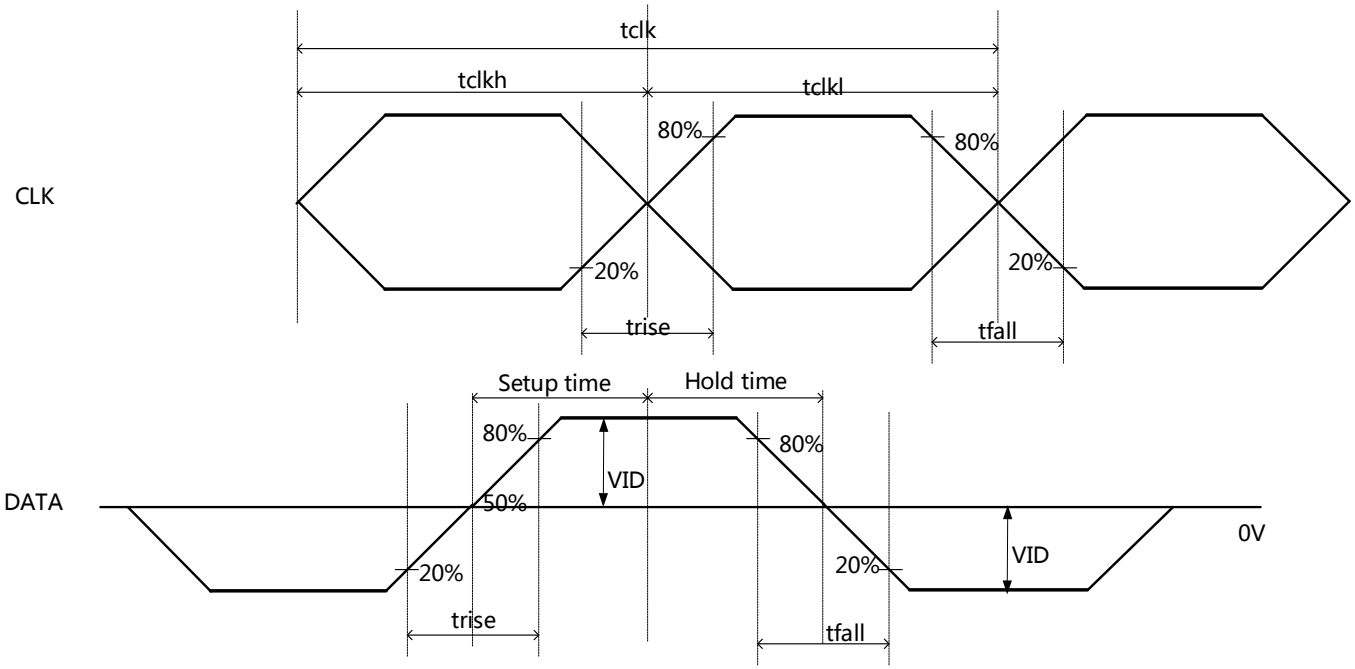
6.0 SIGNAL TIMING SPECIFICATIONS

6.4 miniLVDS Eye Diagram



< Table 10. Eye Diagram information >

Parameter	Symbol	Spec			Unit
		Min	Typ	Max	
Clock Period	tclk	4	-	-	ns
Clock low pulse width	tclkh	0.4tclk	-	0.6tclk	ns
Clock high pulse width	tclkl	0.4tclk	-	0.6tclk	ns
Data setup time	tsetup	0.8	-	-	ns
Data hold time	thold	0.8	-	-	ns
CLK,Data rising time	trise	-	-	0.8	ns
CLK,Data falling time	tfall	-	-	0.8	ns
mini-LVDS different voltage	VID	150	-	600	mv
mini-LVDS Common mode Input Voltage Range(center)	VI	VSS+0.5	1.2	DVDD-1.5	V

Condition:Mini-LVDS CLK MAX Frequency≤250Mhz
The Eye Diagram is the source driver received information.