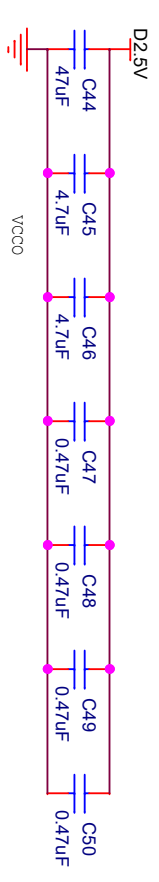
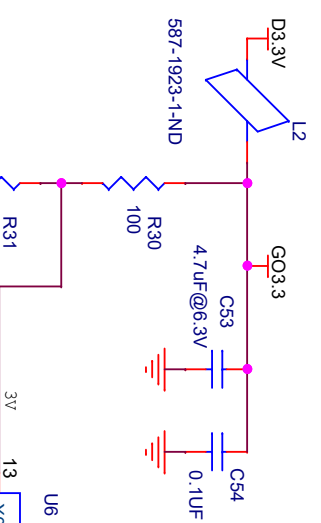
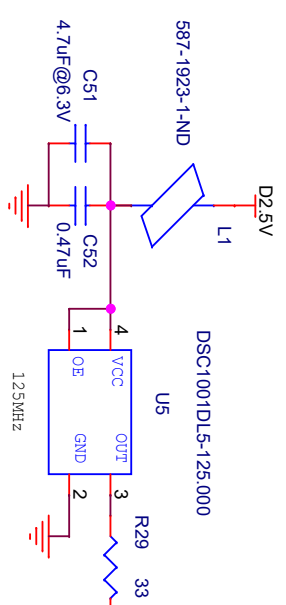
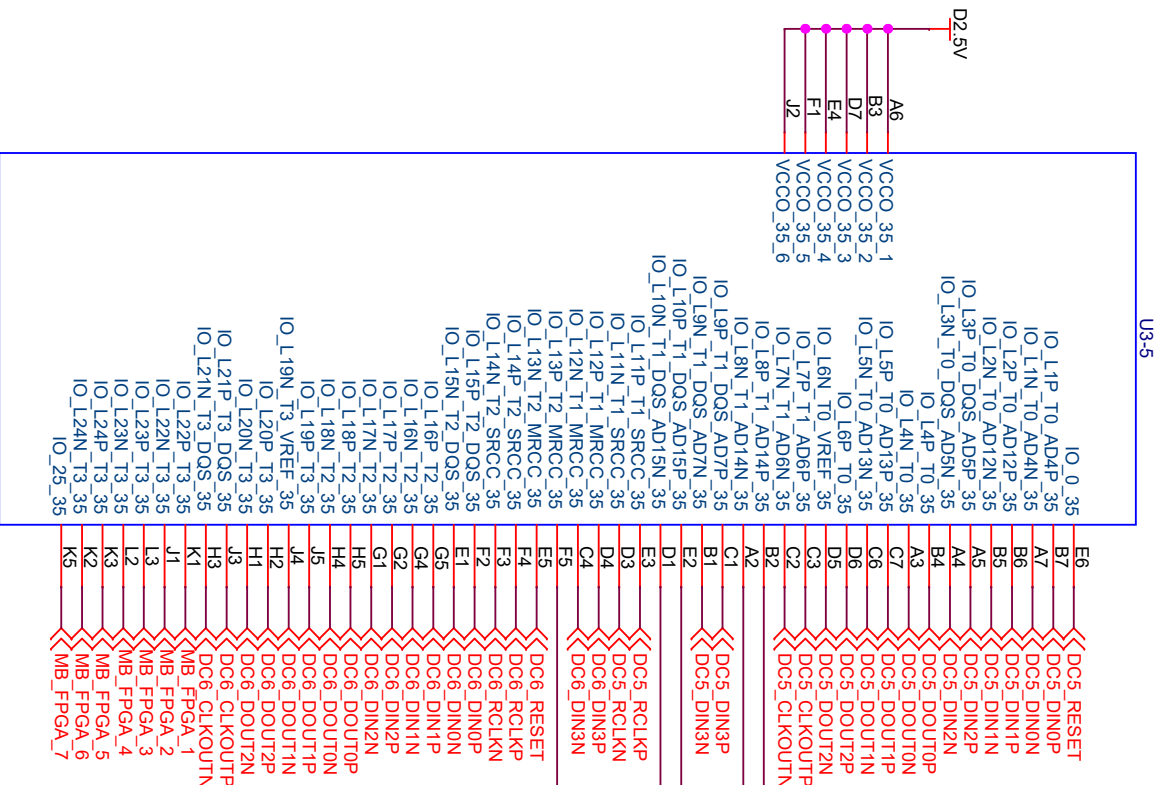
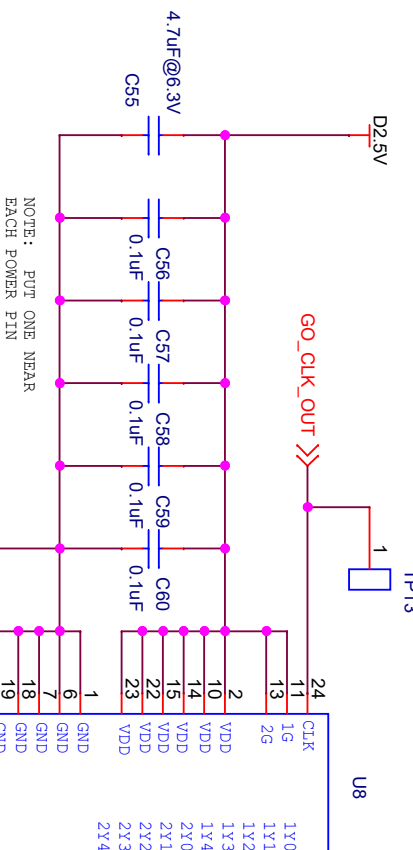
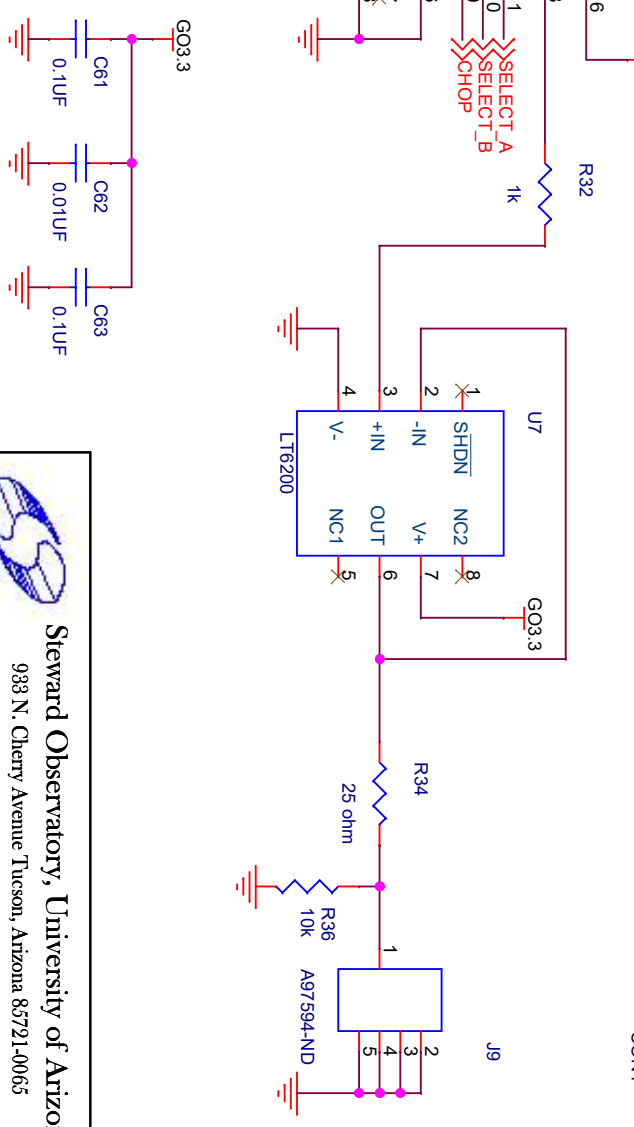
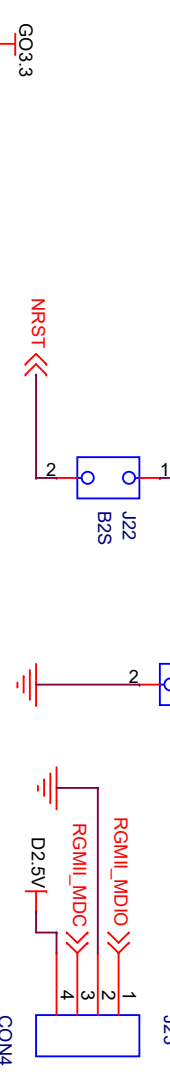
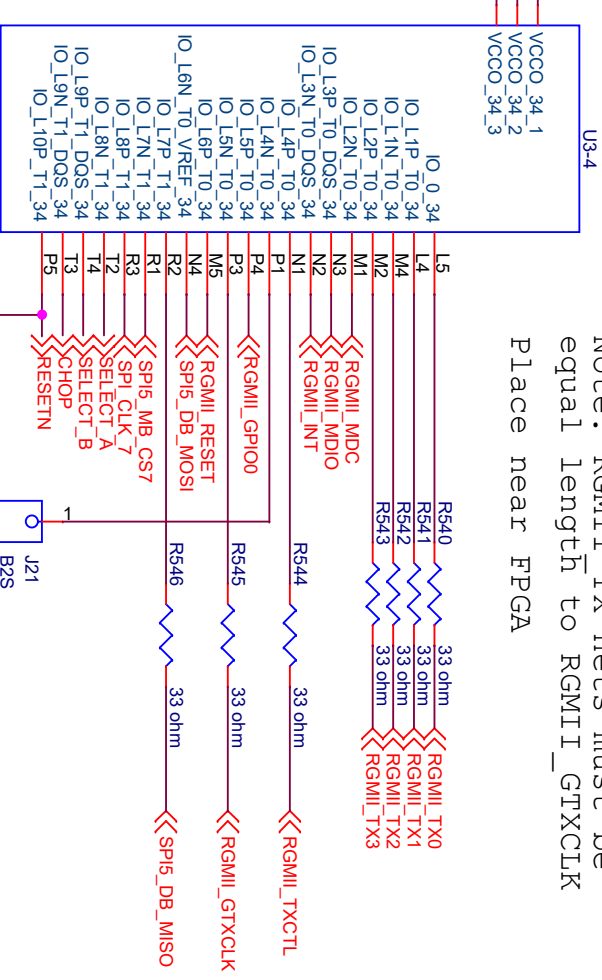


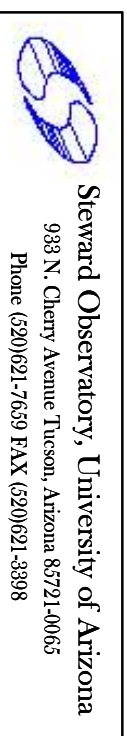
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Rev		0



Note: RGMII_TX nets must be equal length to RGMII_GTXCLK Place near FPGA



NOTE: PUT ONE NEAR EACH POWER PIN

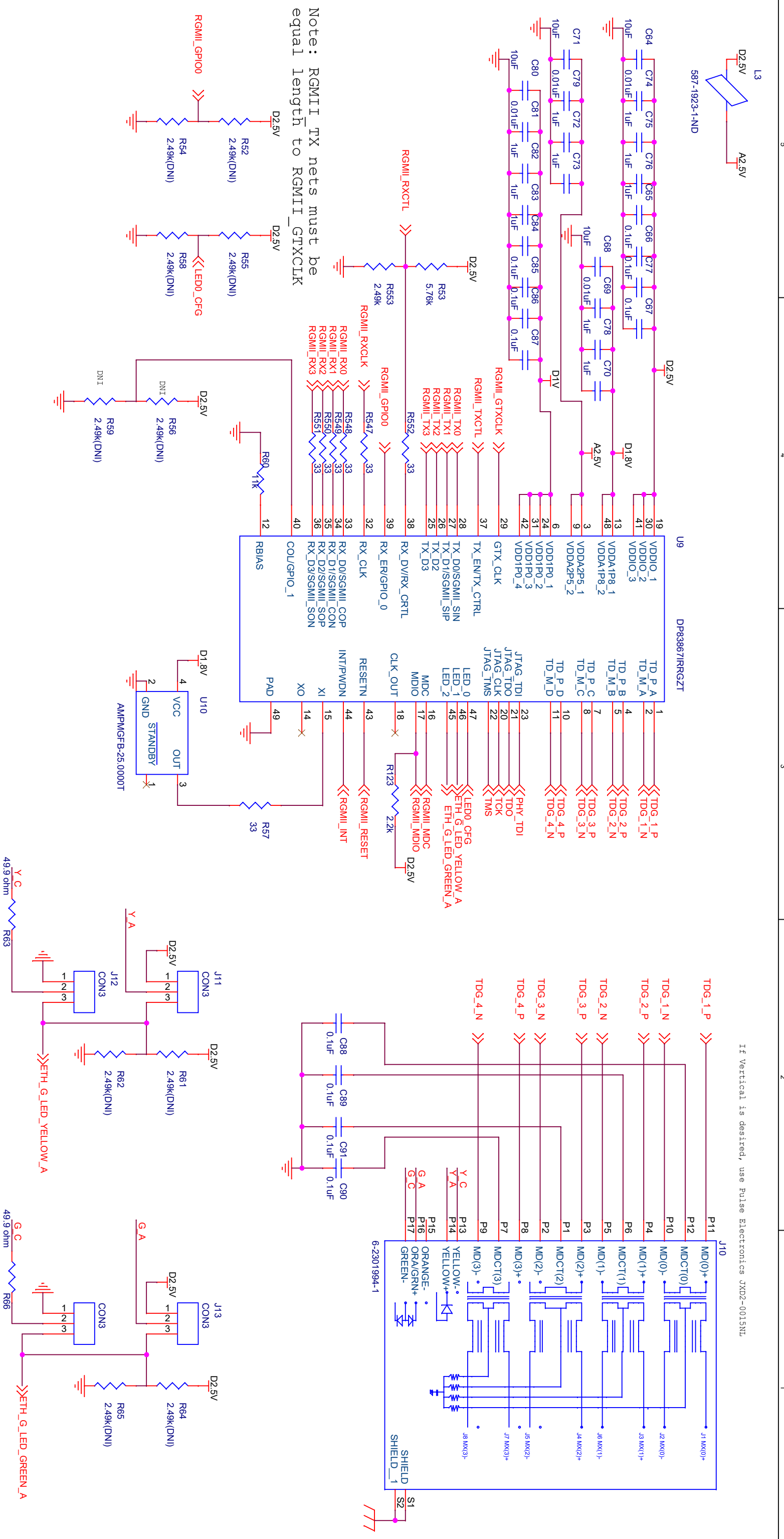


Steward Observatory, University of Arizona
983 N. Cherry Avenue Tucson, Arizona 85721-0065
Phone (520)621-7659 FAX (520)621-3398

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If Vertical is desired, use Pulse Electronics JXD2--0015NL



Note: RGMII TX nets must be equal length to RGMII GTXCLK

Note: Make all RGMII_RX* traces equal length

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B		Sheet	5 of 8
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