

467 = 38F

PHY0

468 = 0



DP83822HF, DP83822IF, DP83822H, DP83822I

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Table 11 describes the DP83822 configuration bootstraps:

Table 11. 4-Level Strap Pins

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
			MODE	FX_EN	PHY_AD0	
COL 00	29	[01]	1	0	0	FX_EN: Enables 100BASE-FX when set to '1' PHY_AD0: PHY Address bit[0] <i>OPEN/1.96K PD</i>
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_D0 00	30	[10]	1 (Default)	1	0	AN_1: See Table 12 below PHY_AD1: PHY Address bit[1] <i>OPEN/OPEN</i>
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1 00	31	[00]	1 (Default)	0	0	EEE_EN: Enables EEE operation when set to '1' PHY_AD2: PHY Address bit [2] <i>OPEN/OPEN</i>
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2 00	32	[00]	1 (Default)	0	0	FLD_EN: Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. PHY_AD3: PHY Address bit[3] <i>OPEN/OPEN</i>
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3 00	1	[10]	1 (Default)	1	0	AN_EN: See Table 12 below PHY_AD4: PHY Address bit[4] <i>OPEN/OPEN</i>
			2	0	0	
			3	0	1	
			4	1	1	
LED_0 11	17	[X1]	1	X	0	AN_0: See Table 12 below <i>OPEN/OPEN</i>
			2	X	0	
			3	X	1	
			4 (Default)	X	1	
CRS 10	27	[01]	1	0	0	LED_CFG: See Table 13 below LED_SPEED: See Table 14 below <i>6.2K-PV/1.96K-PD</i>
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_ER 11	28	[01]	1	0	0	AMDIX_EN: Enables Auto-MDIX when set to '1' RGMII_EN: See Table 15 below SD_EN: Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active LOW, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465). <i>OPEN/OPEN</i>
			2	1	0	
			3	1	1	
			4 (Default)	0	1	

Table 11. 4-Level Strap Pins (continued)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
			MODE	XI_50	RMII_EN	
RX_DV 00	26	[00]	1 (Default)	0	0	XI_50: See Table 15 below RMII_EN: See Table 15 below
			2	1	0	
			3	0	1	
			4	1	1	

Table 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

Table 13. LED_0 Configuration

Strap Mode	LED_CFG[0]	LED_0
4 & 3	1	ON for Good Link OFF for No Link
2 & 1	0	ON for Good Link BLINK for TX/RX Activity

Table 14. LED_1 Configuration

Strap Mode	LED_SPEED	LED_1
4 & 1	0	LED_1 in Tri-State
3 & 2	1	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED

Table 15. MAC Interface Configuration

RGMI_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	Reserved
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	Reserved

467 = F8F
468 = 0x0

PHY I



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Table 11 describes the DP83822 configuration bootstraps:

Table 11. 4-Level Strap Pins

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
			MODE	FX_EN	PHY_AD0	
COL 11	29	[01]	MODE	FX_EN	PHY_AD0	FX_EN: Enables 100BASE-FX when set to '1' PHY_AD0: PHY Address bit[0]
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_D0 00	30	[10]	MODE	AN_1	PHY_AD1	AN_1: See Table 12 below PHY_AD1: PHY Address bit[1]
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1 00	31	[00]	MODE	EEE_EN	PHY_AD2	EEE_EN: Enables EEE operation when set to '1' PHY_AD2: PHY Address bit [2]
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2 00	32	[00]	MODE	FLD_EN	PHY_AD3	FLD_EN: Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. PHY_AD3: PHY Address bit[3]
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3 00	1	[10]	MODE	AN_EN	PHY_AD4	AN_EN: See Table 12 below PHY_AD4: PHY Address bit[4]
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
LED_0 11	17	[X1]	MODE	RESERVED	AN_0	AN_0: See Table 12 below
			1	X	0	
			2	X	0	
			3	X	1	
			4 (Default)	X	1	
CRS 10	27	[01]	MODE	LED_SPEED	LED_CFG	LED_CFG: See Table 13 below LED_SPEED: See Table 14 below
			1	0	0	
			2	1	1	
			3	1	1	
			4 (Default)	0	1	
RX_ER 11	28	[01]	MODE	RGMII_EN	AMDIX_EN (SD_EN)	AMDIX_EN: Enables Auto-MDIX when set to '1' RGMII_EN: See Table 15 below SD_EN: Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active LOW, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465).
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	

Table 11. 4-Level Strap Pins (continued)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
			MODE	XI_50	RMII_EN	
RX_DV 	26	[00]	1 (Default)	0	0	XI_50: See Table 15 below RMII_EN: See Table 15 below
			2	1	0	
			3	0	1	
			4	1	1	

Table 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

Table 13. LED_0 Configuration

Strap Mode	LED_CFG[0]	LED_0
4 & 3	1	ON for Good Link OFF for No Link
2 & 1	0	ON for Good Link BLINK for TX/RX Activity

Table 14. LED_1 Configuration

Strap Mode	LED_SPEED	LED_1
4 & 1	0	LED_1 in Tri-State
3 & 2	1	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED

Table 15. MAC Interface Configuration

RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	Reserved
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	Reserved