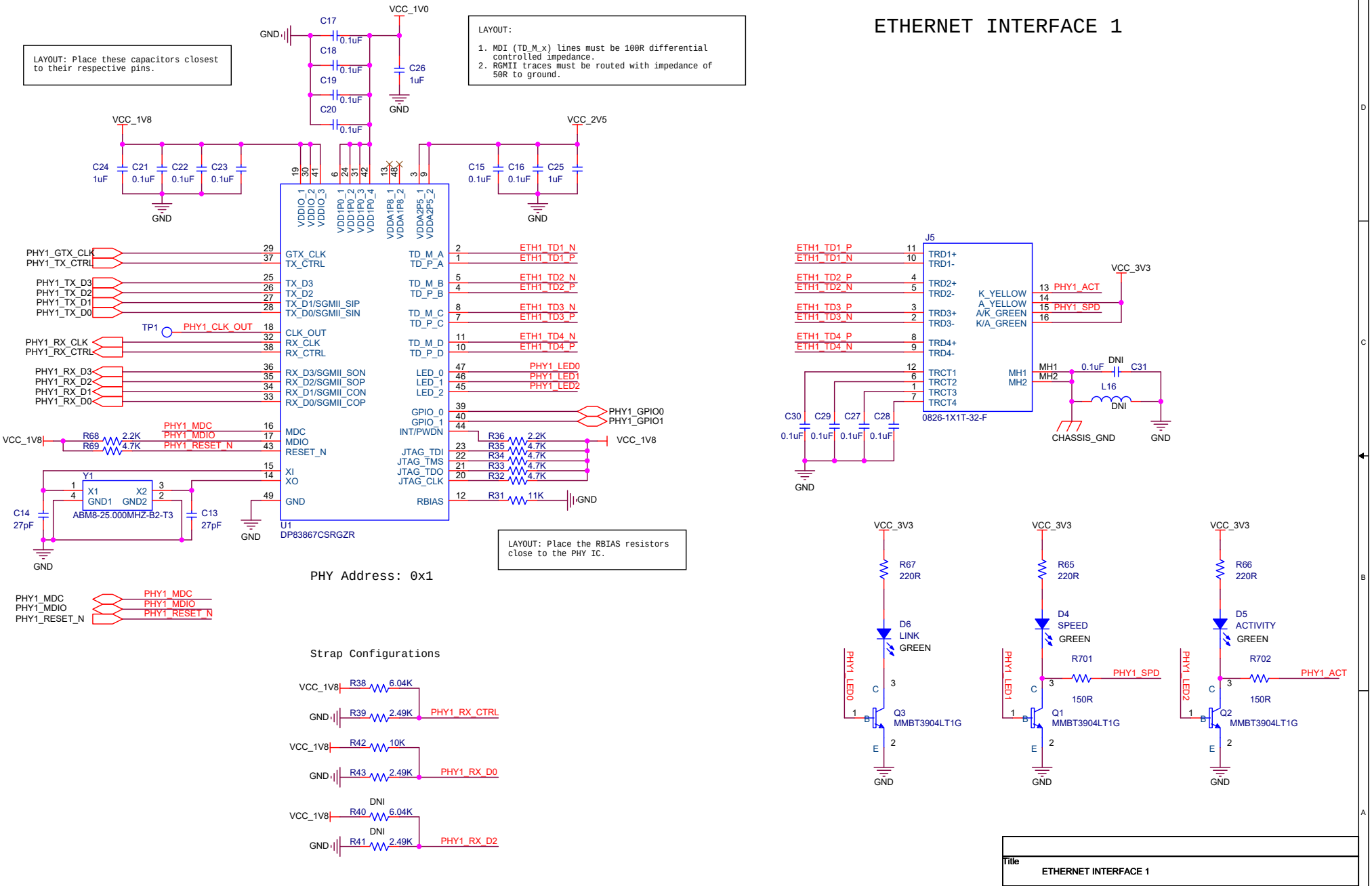
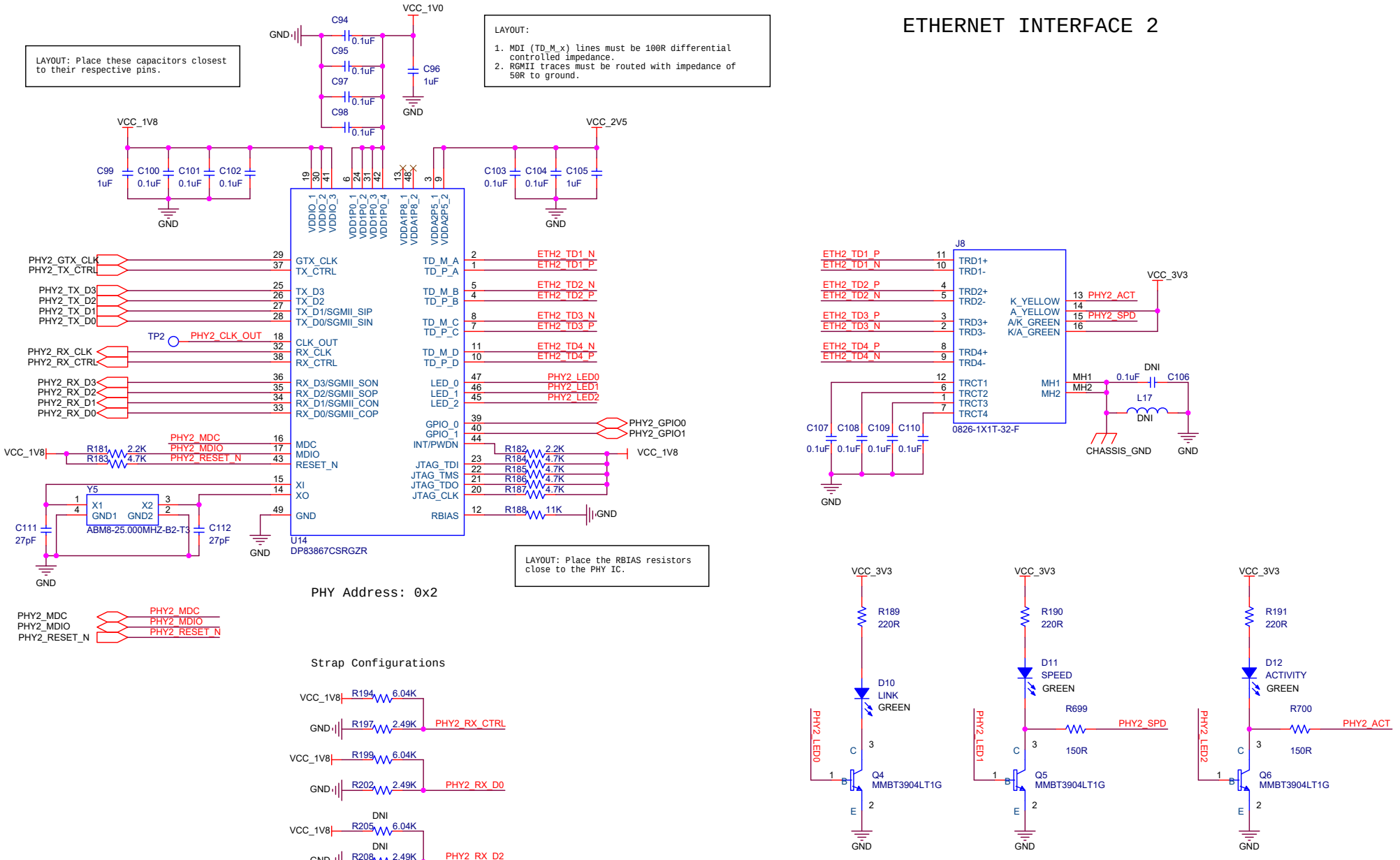
ETHERNET INTERFACE 1



Title	ETHERNET INTERFACE 1		
Size B	Document Number 1.0		Rev 0.4
Date: Thursday, September 25, 2025	Sheet 4 of 34		

ETHERNET INTERFACE 2



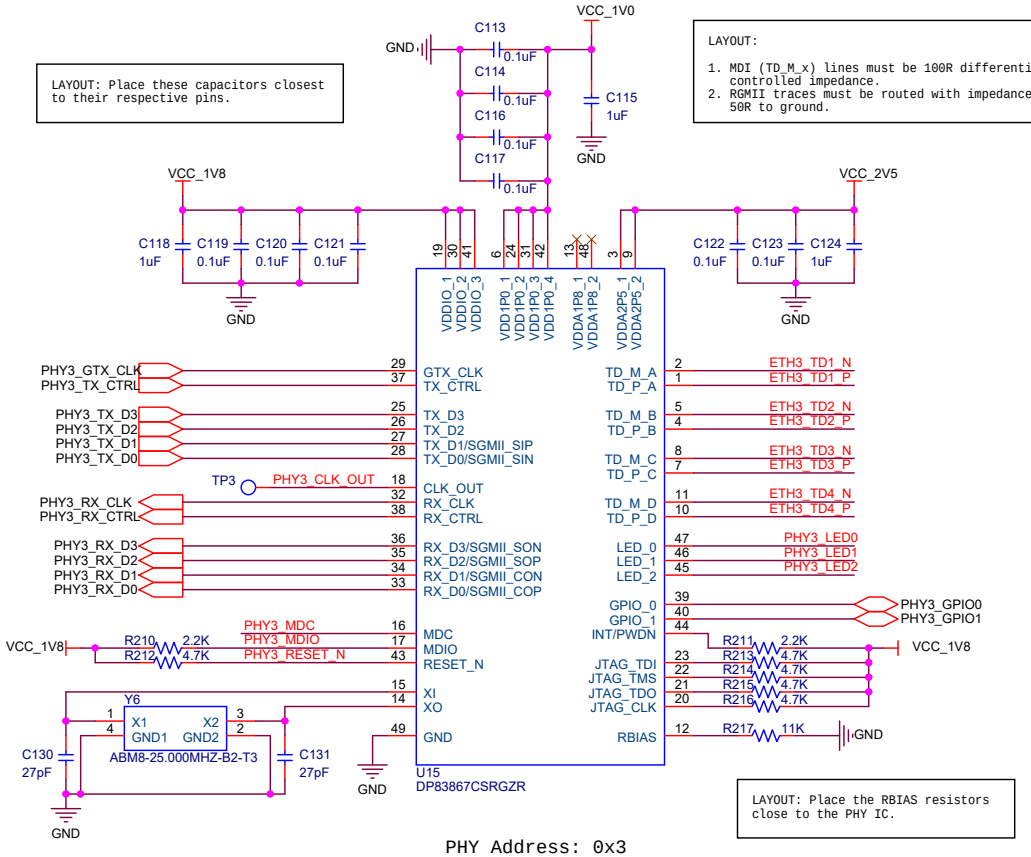
Title	ETHERNET INTERFACE 2	
Size B	Document Number 1.0	Rev 0.4
Date: Thursday, September 25, 2025	Sheet 5 of 34	

ETHERNET INTERFACE 3

LAYOUT: Place these capacitors closest to their respective pins.

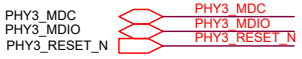
LAYOUT:

1. MDI (TD_M_x) lines must be 100R differential controlled impedance.
2. RGMII traces must be routed with impedance of 50R to ground.

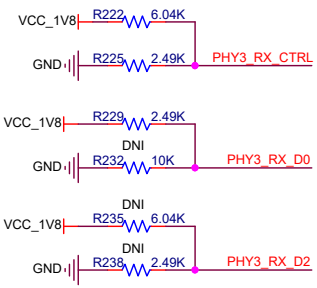


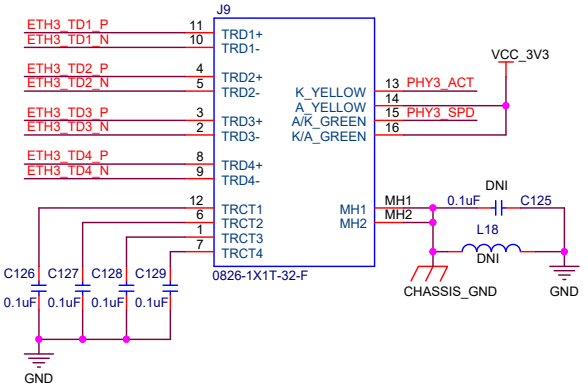
LAYOUT: Place the RBIAS resistors close to the PHY IC.

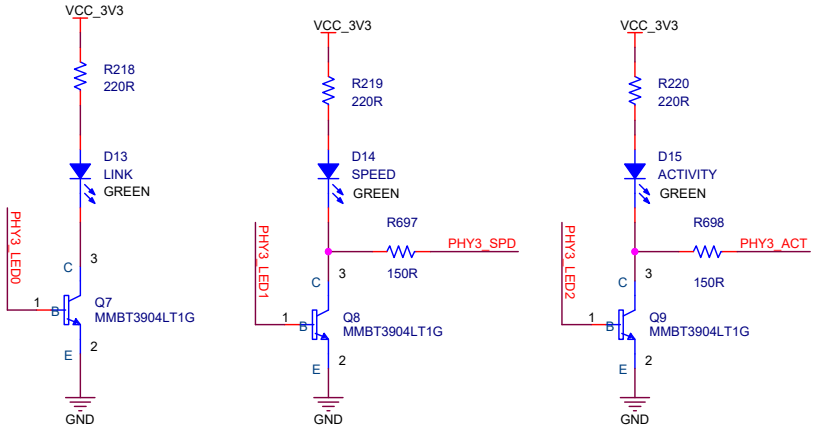
PHY Address: 0x3



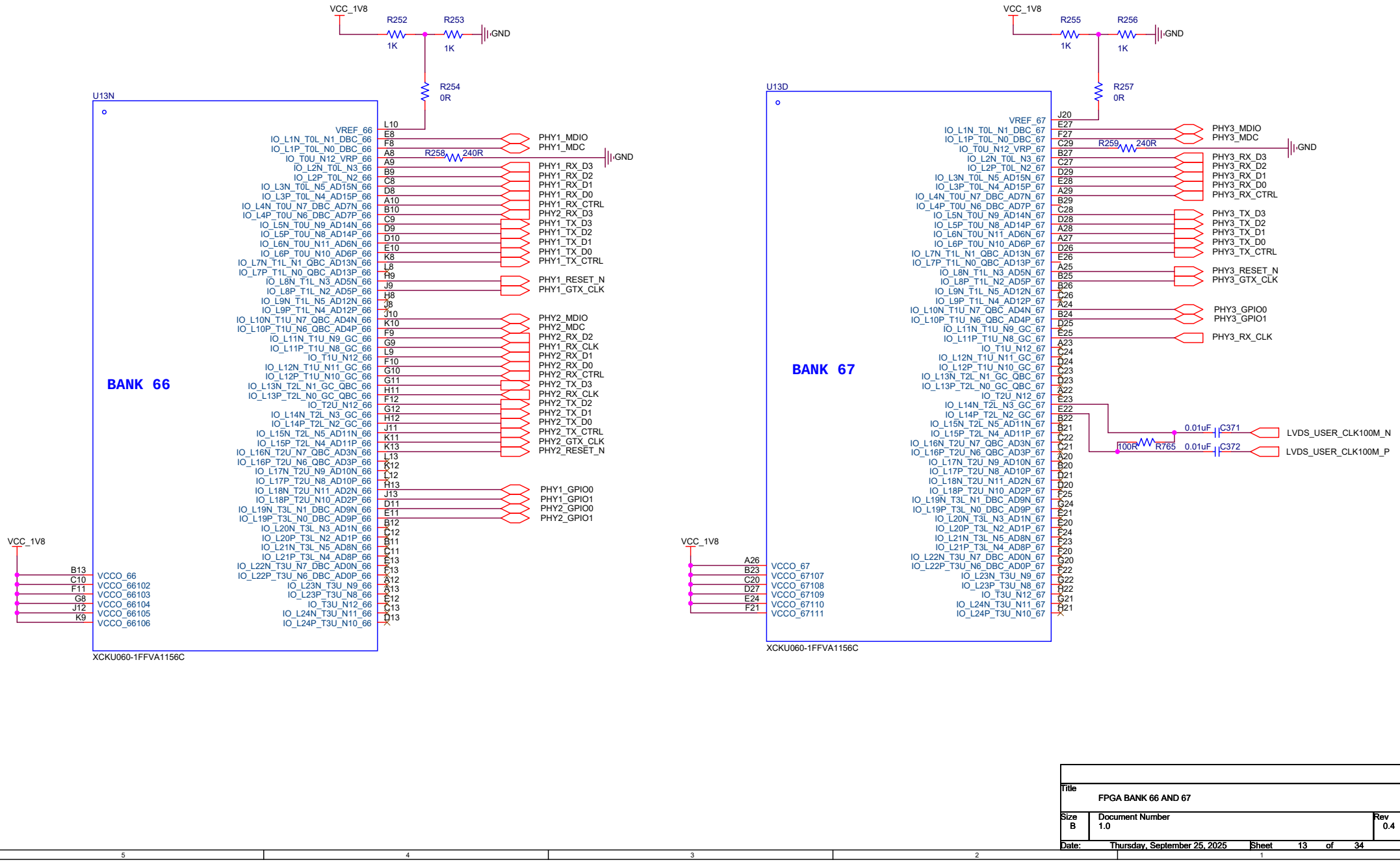
Strap Configurations







Title	ETHERNET INTERFACE 3	
Size B	Document Number 1.0	Rev 0.4
Date: Thursday, September 25, 2025	Sheet 6 of 34	



Title	FPGA BANK 66 AND 67	
Size B	Document Number 1.0	Rev 0.4
Date: Thursday, September 25, 2025	Sheet 13 of 34	