Loss Budget allocation according to 802.3bm

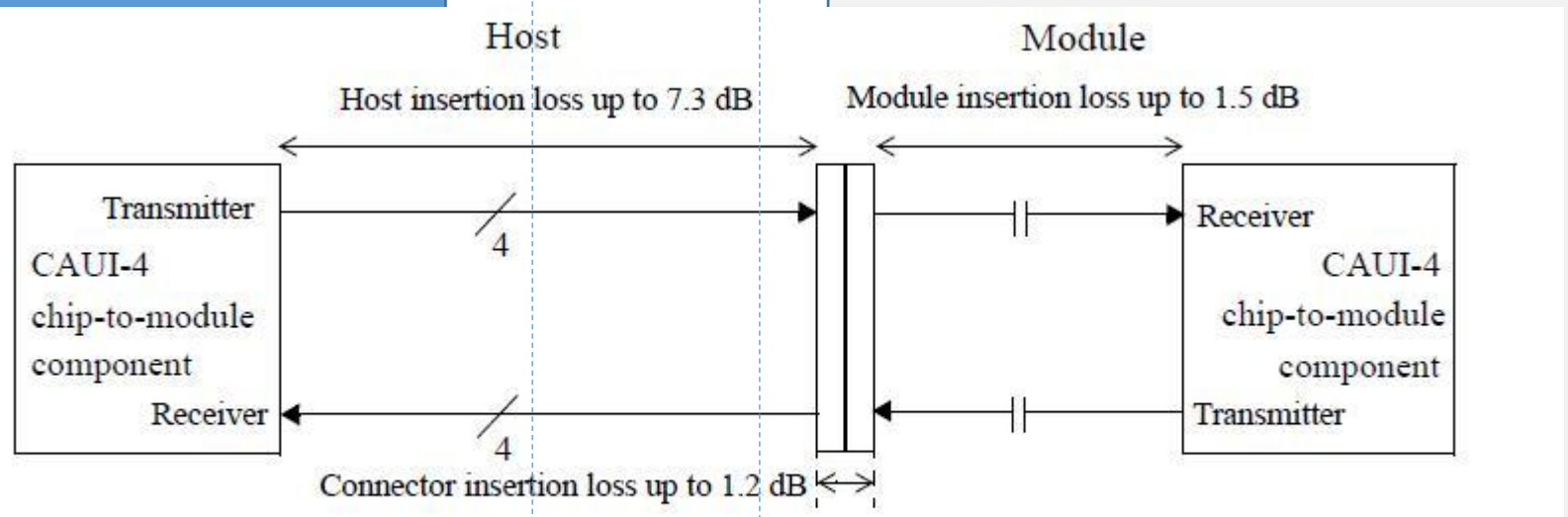


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

FPGA Board with
SERDES 4x25G

QSFP28 Transceiver Module
On mainboard

FireFly Cable used to connect FPGA
Board to Mainboard with QSFP28 port :
because of this cable we are 2 dB out of range of loss budget allocated for CAU-4 interface according to standard 802.3bm

Loss Budget allocation according to 802.3bm

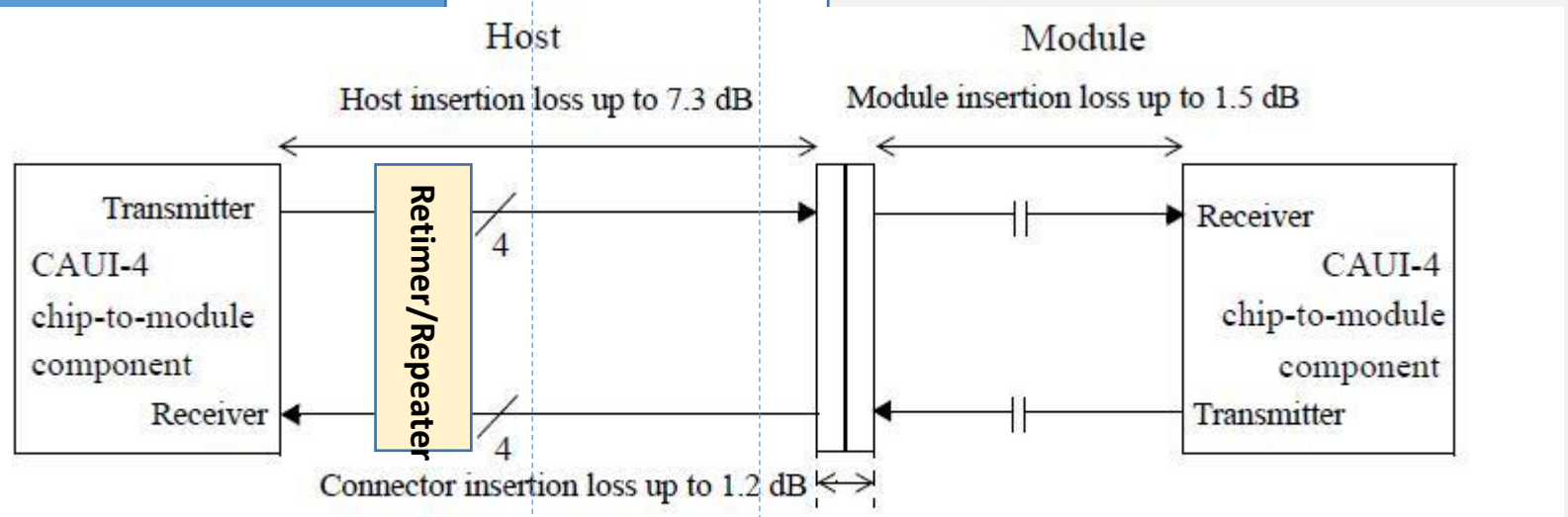


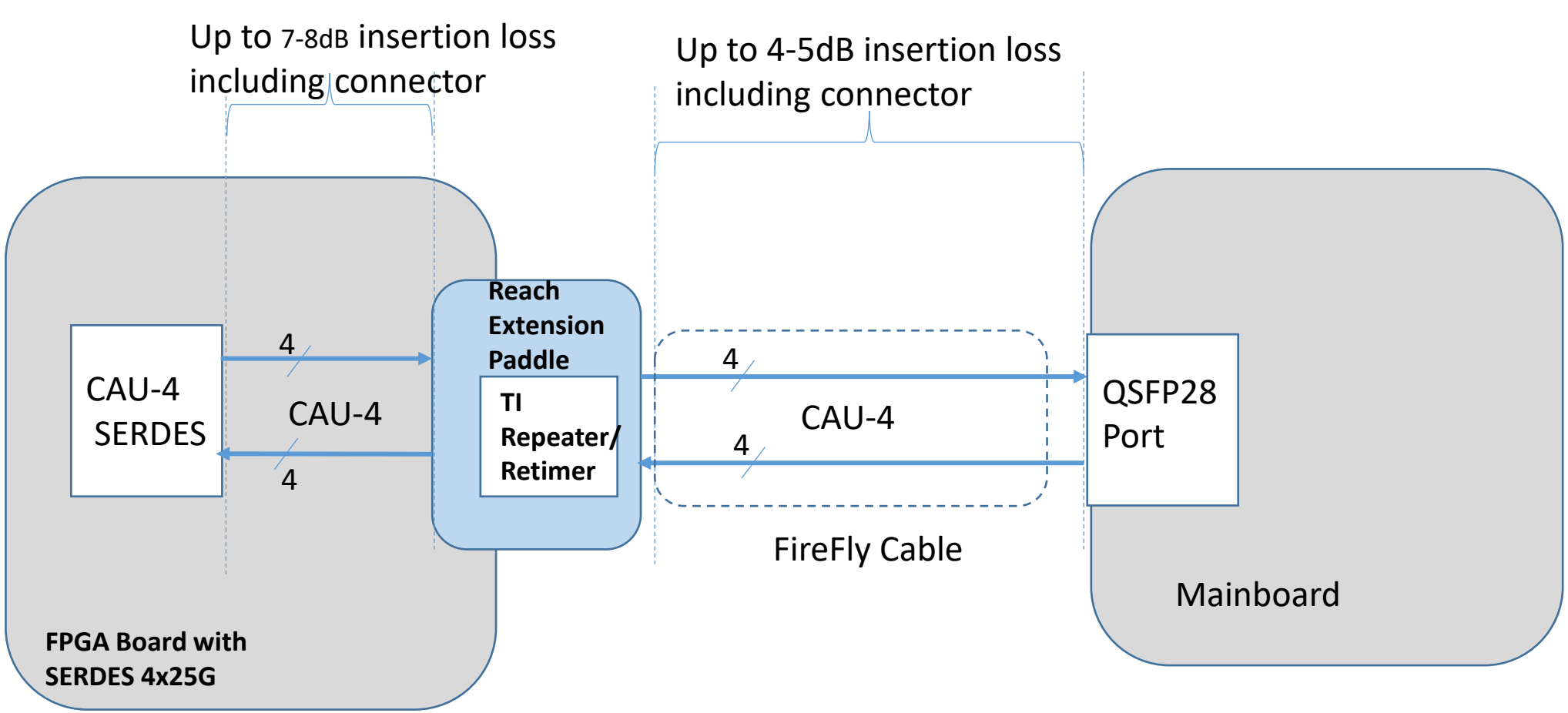
Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

FPGA Board with
SERDES 4x25G

QSFP28 Transceiver Module
On mainboard

FireFly Cable used to connect FPGA
Board to Mainboard with QSFP28 port :
because of this cable we are 2 dB out of range of loss budget allocated for CAU-4 interface according to standard 802.3bm:

Inserted Retimer/Repeater placed between FPGA Board and FireFly cable
Is targeted to resolve excessive loss issue


Up to 7-8dB insertion loss including connector
Up to 4-5dB insertion loss including connector
CAU-4 SERDES
4
CAU-4
4
Reach Extension Paddle
TI Repeater/ Retimer
4
CAU-4
4
QSFP28 Port
FireFly Cable
Mainboard
FPGA Board with SERDES 4x25G