



Test Report

Overall Result: FAIL

Test Configuration Details	
Application	
Name	D9020DPHC MIPI D-PHY Test
Version	3.90.0.0
Device Description	
High Speed Data Rate(Mbps)	800
CTS Version	v1.2
ZID	100 ohm
CLoad	50pF
Fixture Setup	Auto Load Switching
Test Session Details	
Infiniium SW Version	06.50.00906
Infiniium Model Number	MSOV134A
Infiniium Serial Number	MY57220101
Debug Mode Used	No
Compliance Limits	MIPI D-PHY Test Limit v1.2 (official)
Probe (Channel 1)	Model: 1169B Serial: US55390644 Head: N5425A/B Atten: Calibrated (12 NOV 2022 17:02:59), Using Cal Atten (3.2385E+00) Skew: Calibrated (12 NOV 2022 17:03:10), Using Cal Skew
Probe (Channel 2)	Model: 1169B Serial: US55390676 Head: N5425A/B Atten: Calibrated (12 NOV 2022 17:04:06), Using Cal Atten (3.2377E+00) Skew: Calibrated (12 NOV 2022 17:04:18), Using Cal Skew
Probe (Channel 3)	Model: 1169B Serial: US55390699 Head: N5425A/B Atten: Calibrated (12 NOV 2022 18:20:14), Using Cal Atten (3.2203E+00) Skew: Calibrated (12 NOV 2022 18:20:24), Using Cal Skew
Probe (Channel 4)	Model: 1169B Serial: US55390726 Head: N5425A/B Atten: Calibrated (12 NOV 2022 18:13:15), Using Cal Atten (3.1476E+00) Skew: Calibrated (12 NOV 2022 18:13:26), Using Cal Skew
Last Test Date	2022-11-12 21:13:15 UTC +08:00

Summary of Results

Test Statistics	
Failed	2
Passed	31
Total	33

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx)	185.62 mV	35.6 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.3.8 HS Data TX Vcmtx Mismatch	1.19 mV	76.2 %	VALUE < 5.00 mV
✓	0	1	1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF))	6.62 mV	55.9 %	VALUE < 15.00 mV
✓	0	1	1.3.9 HS Data TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	9.07 mV	63.7 %	VALUE < 25.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD0 Pulse)	-185.58 mV	35.1 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.3.4 HS Data TX Differential Voltage(VOD1 Pulse)	185.19 mV	34.8 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.3.5 HS Data TX Differential Voltage Mismatch (Pulse)	400 µV	97.1 %	VALUE < 14.00 mV
✓	0	1	1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse)	280.95 mV	22.0 %	VALUE <= 360.00 mV
✓	0	1	1.4.17 HS Clock Instantaneous (Uinst) (Max)	1.290 ns	89.7 %	VALUE < 12.500 ns
✓	0	1	1.3.3 HS Entry: DATA TX THS- PREPARE+THS- ZERO	225.81 ns	43.4 %	VALUE >= TXTHSPrepareTHSZero_LimitMin s

✗	1	1	1.3.11 HS Data TX 20%-80% Rise Time (tR)[Burst Data]	375 ps	0.0 %	VALUE < DataRiseTime_LimitMax s
✓	0	1	1.3.12 HS Data TX 80%-20% Fall Time (tF)[Burst Data]	373 ps	0.5 %	VALUE < DataFallTime_LimitMax s
✓	0	1	1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF))	10.36 mV	58.6 %	VALUE < 25.00 mV
✓	0	1	1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx)	192.08 mV	42.1 %	150.00 mV <= VALUE <= 250.00 mV
✓	0	1	1.4.8 HS Clock TX Vcmtx Mismatch	4.29 mV	14.2 %	VALUE < 5.00 mV
✓	0	1	1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF))	2.50 mV	83.3 %	VALUE < 15.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse)	-175.60 mV	27.4 %	-270.00 mV <= VALUE <= -140.00 mV
✓	0	1	1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse)	178.70 mV	29.8 %	140.00 mV <= VALUE <= 270.00 mV
✓	0	1	1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse)	3.10 mV	77.9 %	VALUE < 14.00 mV
✓	0	1	1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse)	291.78 mV	19.0 %	VALUE <= 360.00 mV
✓	0	1	1.4.11 HS Clock TX 20%-80% Rise Time (tR)[Continuous Clock, Burst Data]	340 ps	9.3 %	VALUE < CLKRiseTime_LimitMax s
✓	0	1	1.4.12 HS Clock TX 80%-20% Fall Time (tF)[Continuous Clock, Burst Data]	346 ps	7.7 %	VALUE < CLKFallTime_LimitMax s
✓	0	1	1.4.17 HS Clock Instantaneous (Uinst) (Min)	1.212 ns	121E+01 %	VALUE >= Uinst_Min_Limit s
✓	0	1	1.4.18 Clock Lane HS Clock Delta UI (UI variation)	3.21 %	34.0 %	UIVariant_Limit_Min % <= VALUE <= UIVariant_Limit_Max %
✓	0	1	1.3.1 HS Entry: DATA TLPX	59.95 ns	19.9 %	VALUE >= 50.00 ns
✓	0	1	1.3.2 HS Entry: DATA	66.30	44.8 %	THSPPrepare_LimitMin s <= VALUE <=

			TX THS-PREPARE	ns		THSPrepare_LimitMax s
✓	0	1	1.3.13 HS Exit: DATA TX THS-TRAIL	80.67 ns	24.1 %	VALUE >= TXTHSTrail_LimitMin s
✓	0	1	1.3.14 HS Exit: DATA TX TREOT	8.99 ns	74.3 %	VALUE <= 35.00 ns
✓	0	1	1.3.15 HS Exit: DATA TX TEOT	89.66 ns	25.3 %	VALUE <= TXTEOT_LimitMax s
✓	0	1	1.3.16 HS Exit: DATA TX THS-EXIT	9.97388 µs	987E+01 %	VALUE >= 100.00 ns
✓	0	1	1.5.3 HS Clock Rising Edge Alignment to First Payload Bit	Pass	100.0 %	VALUE <= 500.000000000 m
✗	1	1	1.5.4 Data-to-Clock Skew (TSKEW(TX)) (Max,Min)	-170 mUlnst	-6.7 %	MinMaxTSkewTest_LimitMin Ulnst <= VALUE <= MinMaxTSkewTest_LimitMax Ulnst
✓	0	1	1.5.4 Data-to-Clock Skew (TSKEW(TX)) (Mean)	-10 mUlnst	46.7 %	MeanTSkewTest_LimitMin Ulnst <= VALUE <= MeanTSkewTest_LimitMax Ulnst

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✓ 1.3.7 HS Data TX Static Common Mode Voltage(Vcmtx) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.7)

Test Summary: Pass Test Description: HS transmit static common-mode voltage.

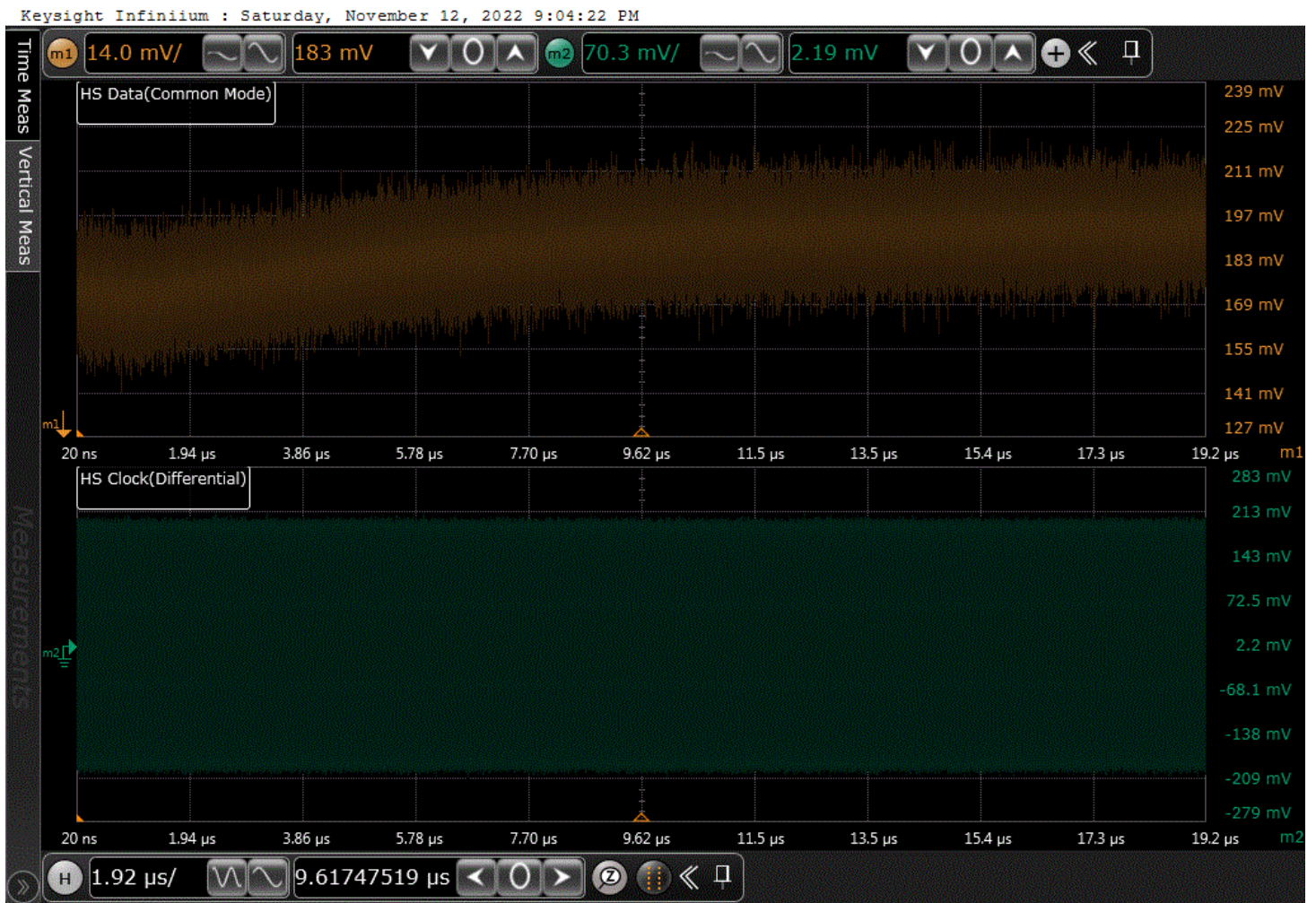
Pass Limits:[150.00 mV to 250.00 mV]811_Vcmtx(Worst)185.62 mV

Result Details:

Result Details

HS Data TX Common Mode Voltage(See image)**Vcmtx(Differential-1)**185.62 mV**Number of Vcmtx(Differential-1) Measured**6.593000 k**Vcmtx(Differential-0)**187.99 mV**Number of Vcmtx(Differential-0) Measured**8.795000 k**ZID**100 ohm**DataLane**Lane1**Number of HS Burst**1 Trial 1

Trial 1: HS Data TX Common Mode Voltage



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✓ 1.3.8 HS Data TX Vcmtx Mismatch Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.8)

Test Summary: Pass Test Description: VCMTX mismatch when output is Differential-1 or Differential-0.

Pass Limits:< 5.00 mV812_Vcmtx Mismatch1.19 mV

Result Details:

Result Details

Vcmtx(Differential-1)185.62 mVVcmtx(Differential-0)187.99 mVZID100

ohmDataLaneLane1Number of HS Burst1

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✓ 1.3.10 HS Data TX Common-Level Variations Above 450MHz (VCMTX(HF)) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.10)

Test Summary: Pass Test Description: Common-level variations above 450MHz.

Pass Limits:< 15.00 mV818_Vcmtx(HF)6.62 mV

Result Details:

Result Details

Common Level Variations(>450Mhz)(See image)ZID100 ohmDataLaneLane1Number of HS Burst1

Trial 1

Trial 1: Common Level Variations(>450Mhz)

Next

Test Summary: Pass Test Description: Common-level variation between 50-450MHz.

Pass Limits:< 25.00 mV819 Vcmtx(LF)9.07 mV

Result Details:

Result Details

Common Level Variations(50-450MHz)(See image)

Trial 1

Trial 1: Common Level Variations(50-450MHz)

The screenshot displays two waveforms on a Tektronix oscilloscope. The top trace, labeled $(Dp+Dn)/2$, shows a noisy signal with a vertical scale of 3.35 mV and a horizontal scale of 131 μ s. The bottom trace, labeled $(Dp+Dn)/2$ - Bandpass filtered at 50MHz -450MHz, shows the same signal after bandpass filtering, with a vertical scale of 1.92 μ s and a horizontal scale of 9.61747519 μ s. A measurement of 17.875 mV is indicated between two points, M3 and M4, on the bottom trace. The oscilloscope interface includes various control buttons and a measurement menu on the right side.

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✓ 1.3.4 HS Data TX Differential Voltage(VOD0 Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.4)

Test Summary: Pass Test Description: HS transmit differential voltage. This test will measure the VOD0 based on the reference data patterns(100000) of differential signal.

Pass Limits:[-270.00 mV to -140.00 mV]8131_Vod0(Mean)-185.58 mV

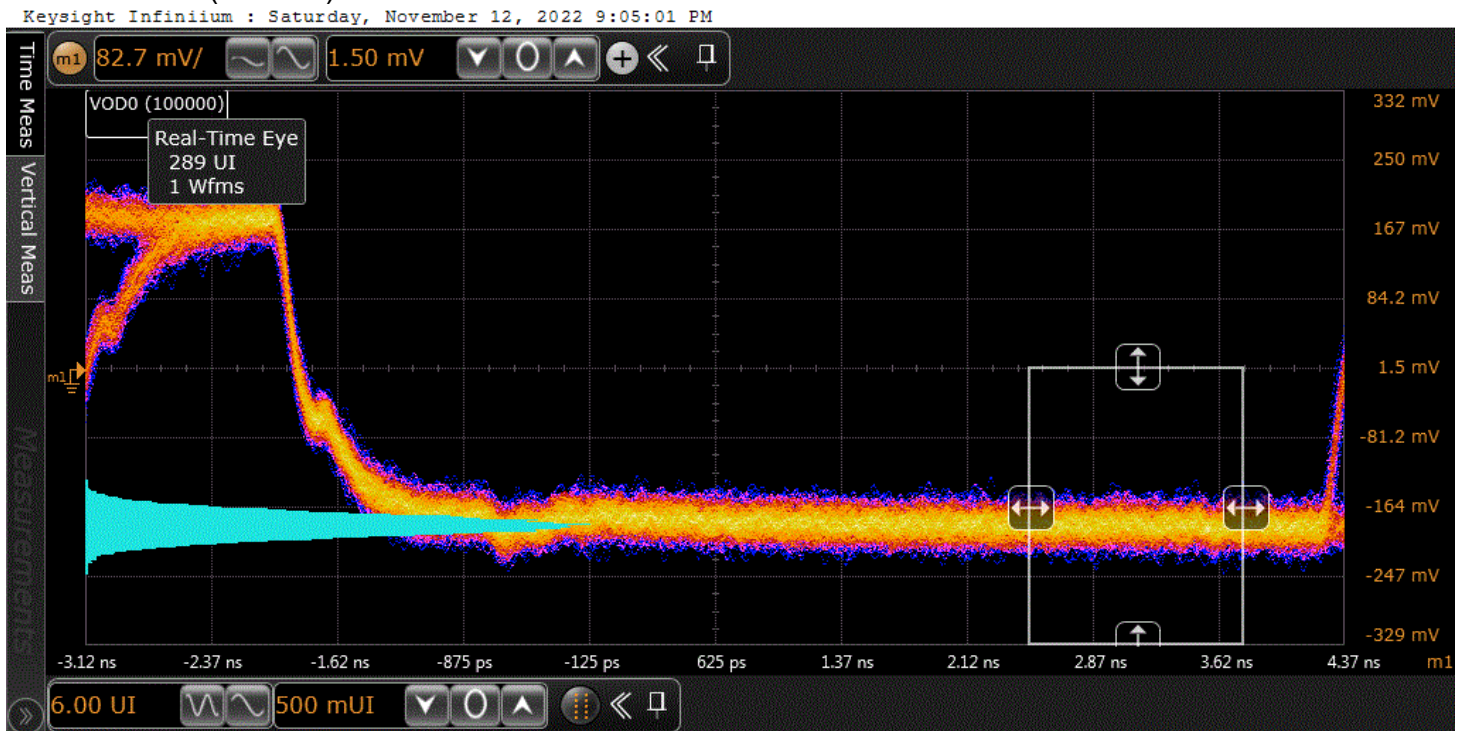
Result Details:

Result Details

VOD0 (100000)(See image)**Vod(Differential-0)**-185.58 mV**Number of measurement**289.000**ZID**100 ohm**DataLane**Lane1**Number of HS Burst**1

Trial 1

Trial 1: VOD0 (100000)



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✓ 1.3.4 HS Data TX Differential Voltage(VOD1 Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.4)

Test Summary: Pass Test Description: HS transmit differential voltage. This test will measure the VOD1 based on the reference data patterns(011111) of differential signal.

Pass Limits:[140.00 mV to 270.00 mV]8132_Vod1(Mean)185.19 mV

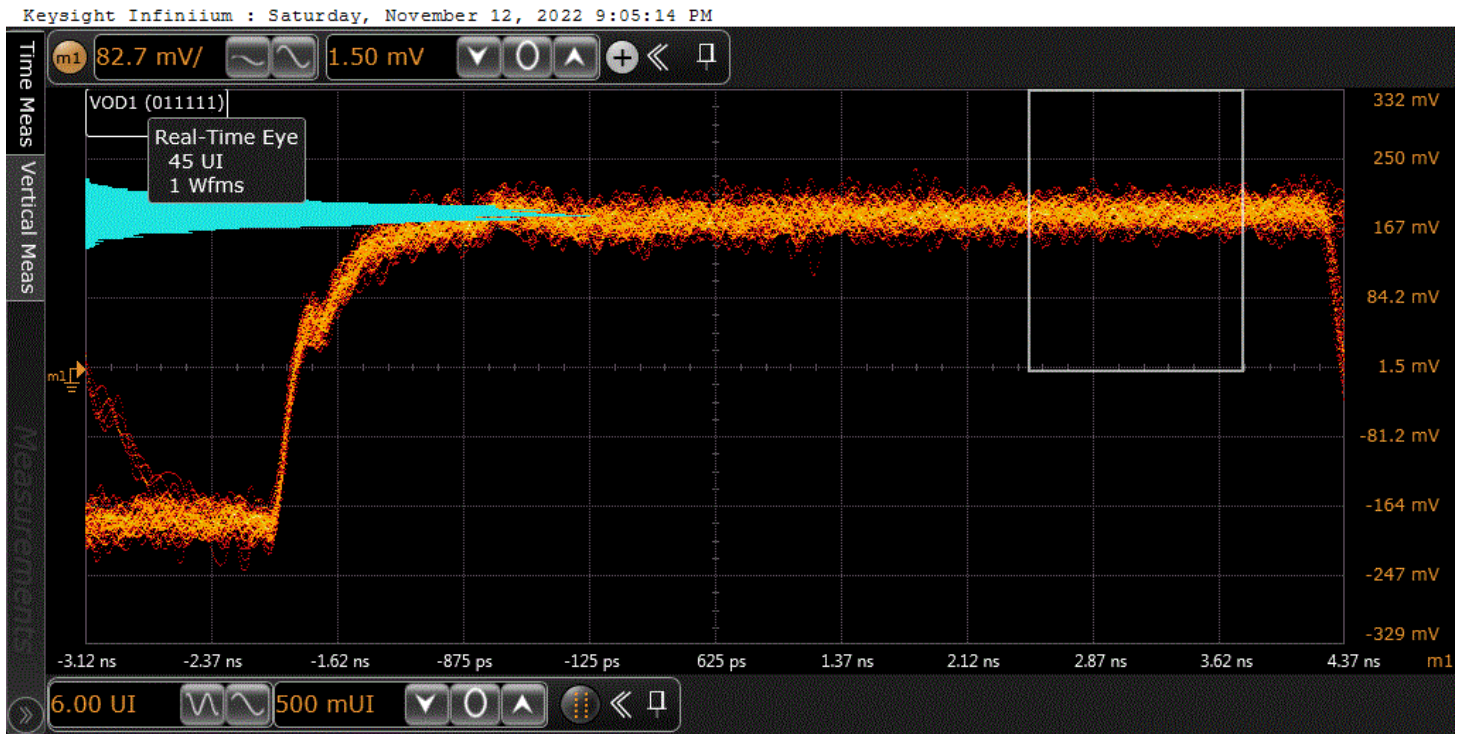
Result Details:

Result Details

VOD1 (011111)(See image)**Vod(Differential-1)**185.19 mV**Number of measurement**45.000**ZID**100 ohm**DataLane**Lane1**Number of HS Burst**1

Trial 1

Trial 1: VOD1 (011111)



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✓ 1.3.5 HS Data TX Differential Voltage Mismatch (Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.5)

Test Summary: Pass Test Description: VOD mismatch when output is Differential-1 or Differential-0.

Pass Limits:< 14.00 mV8141_Vod Mismatch400 μ V

Result Details:

Result Details

Vod(Differential-1)185.19 mV**Vod(Differential-0)**-185.58 mV**ZID**100 ohm**DataLane**Lane1**Number of HS Burst**1

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✓ 1.3.6 HS Data TX Single Ended Output High Voltage(VOHHS Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.3.6)

Test Summary: Pass Test Description: HS Single Ended output high voltage. This test will measure the VOHHS based on the reference pulses(100000) of single-ended Dp and Dn signals.

Pass Limits:<= 360.00 mV8151_Vohhs(Worst)280.95 mV

Result Details:

Result Details

DpVOHHS (011111)(See image)**DnVOHHS (011111)**(See image)**Vohhs(Dp)**280.53

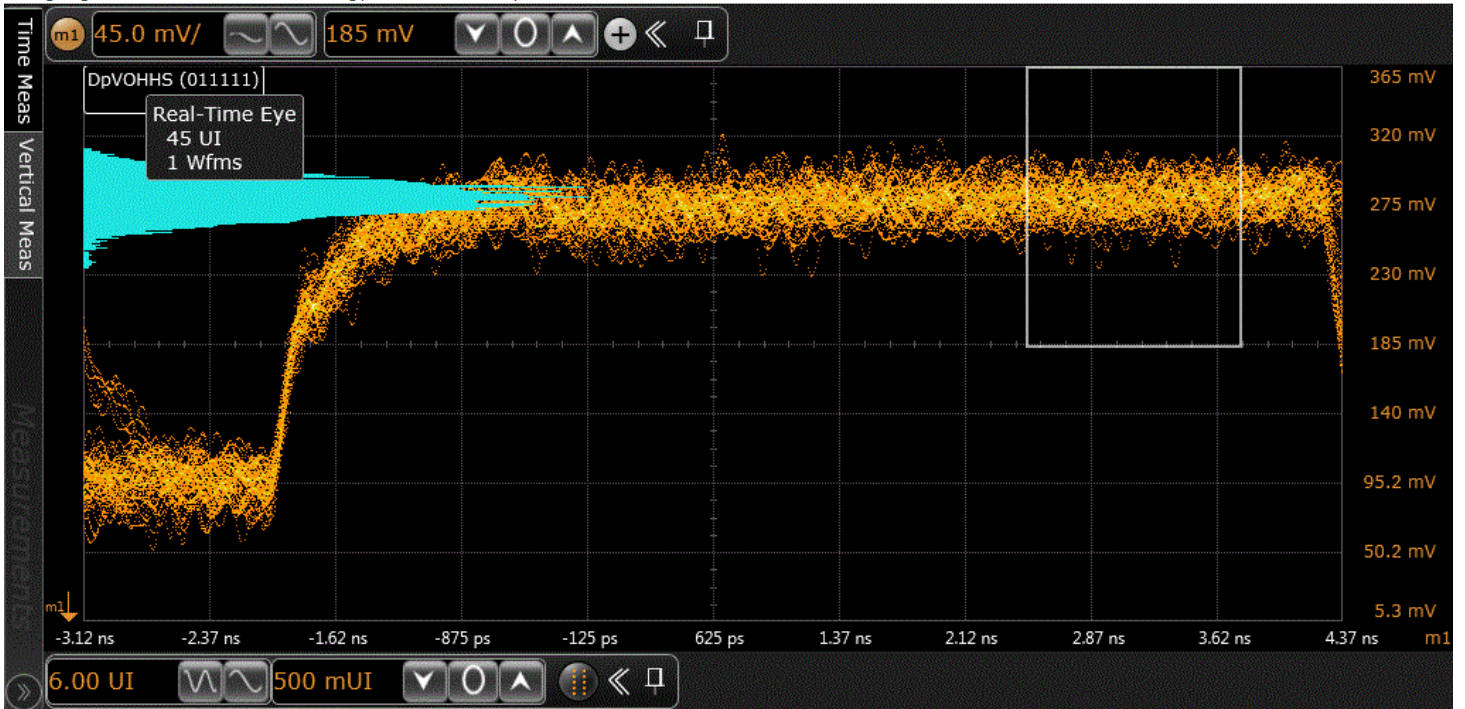
mV**Vohhs(Dn)**280.95 mV**Number of measurement Vohhs(Dp)**45.000**Number of measurement**

Vohhs(Dn)289.000**ZID**100 ohm**DataLane**Lane1**Number of HS Burst**1

Trial 1

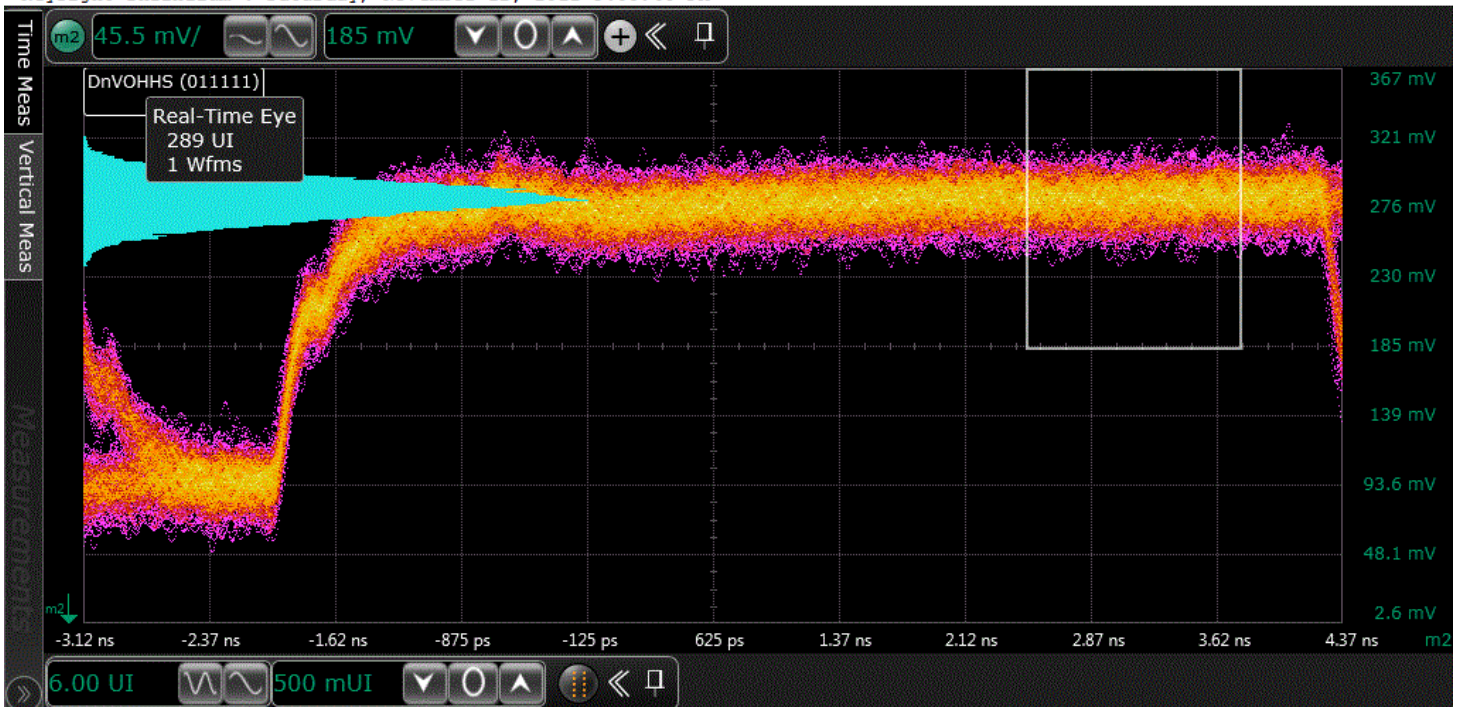
Trial 1: DpVOHHS (011111)

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Trial 1: DnVOHHS (011111)

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✓ 1.4.17 HS Clock Instantaneous (UIinst)(Max) Reference: D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Test Summary: Pass Test Description: Maximum UI instantaneous of HS Clock.

Pass Limits: < 12.500 ns911_UIinst(Max)1.290 ns

Result Details:

Result Details

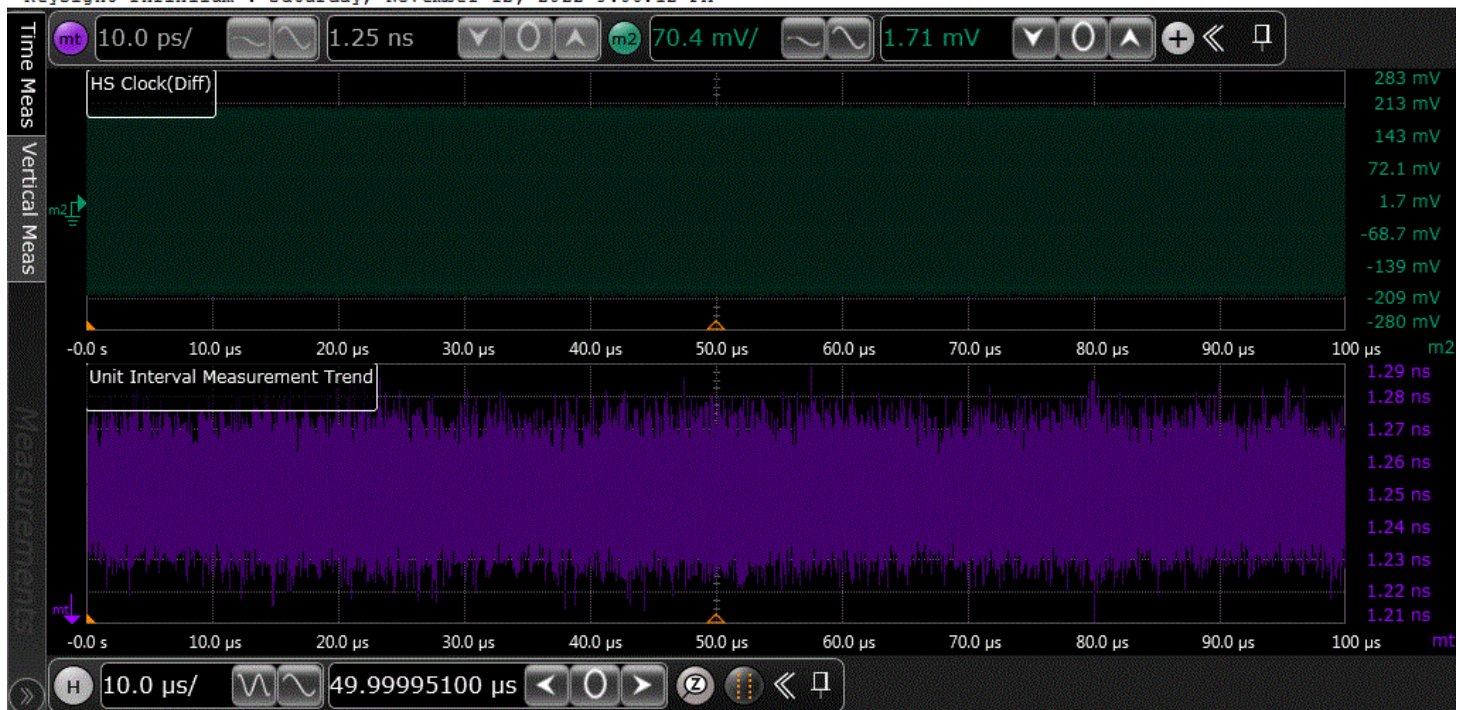
UIInst(See image)UIINST(Max)1.290170 nsUIINST(Mean)1.249993 nsNumber of UI79.999000

kZID100 ohmDataLaneLane1Number of HS Burst1

Trial 1

Trial 1: UIInst

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✓ 1.3.3 HS Entry: DATA TX THS-PREPARE+THS-ZERO Reference: D-PHY Specification v1.2

Section 6.9 Table 14, CTS v1.2(Test 1.3.3)

Test Summary: Pass Test Description: THS-PREPARE+Time to drive HS-0 before Sync sequence.
 TXTHSPrepereTHSZero_LimitMin is based on 145ns+10*UI.

Pass Limits:>= TXTHSPrepereTHSZero_LimitMin s558_THS-PREPARE+THS-ZERO225.81 ns

Result Details:

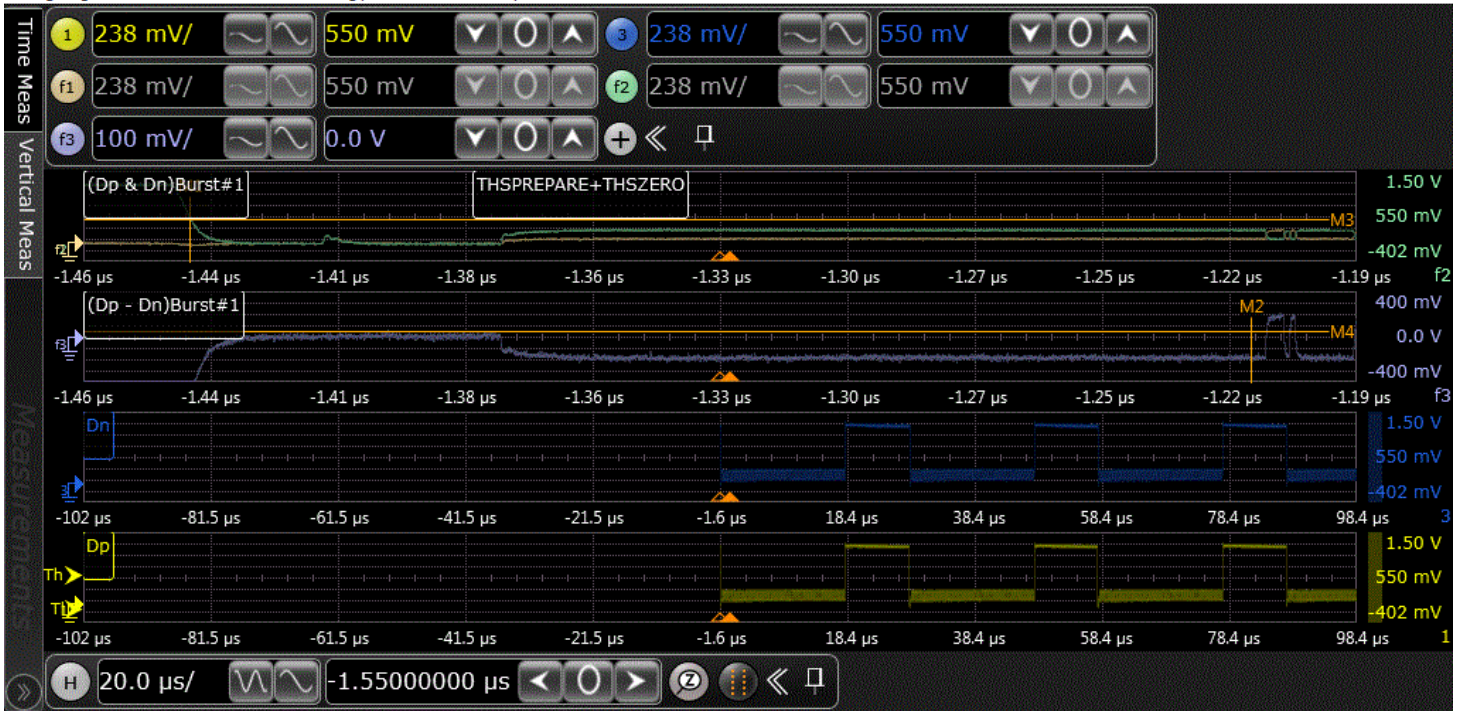
Result Details

THSPREPARE_THSZERO(See image)**UIINST(Mean)**1.249993 ns**VHS_ZERO**-179.13 mV**ZID**100 ohm**DataLaneLane1PassLimit Min (TXTHSPrepereTHSZero_LimitMin)**157.50 ns**Number of HS burst**1

Trial 1

Trial 1: THSPREPARE_THSZERO

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✖ 1.3.11 HS Data TX 20%-80% Rise Time (tR)[Burst Data] Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.3.11)

Test Summary: FAIL **Test Description:** This test is to verify that the 20%-80% rise time of the HS Differential signal is less than the maximum conformance limit(DataRiseTime_LimitMax). For CTS v1.2, the maximum conformance limit(DataRiseTime_LimitMax) is $0.3 \cdot UI$ for Datarate ≤ 1 Gbps, $0.35 \cdot UI$ for Datarate > 1 Gbps and ≤ 1.5 Gbps, $0.4 \cdot UI$ for Datarate > 1.5 Gbps. This test will measure the rise time based on the reference data patterns(000111) of differential signal. This test is applicable for Burst Data signal only. The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for rise time measurement in this test.

Pass Limits: $< \text{DataRiseTime_LimitMax}$ s81101_Rise Time375 ps

Result Details:

Result Details

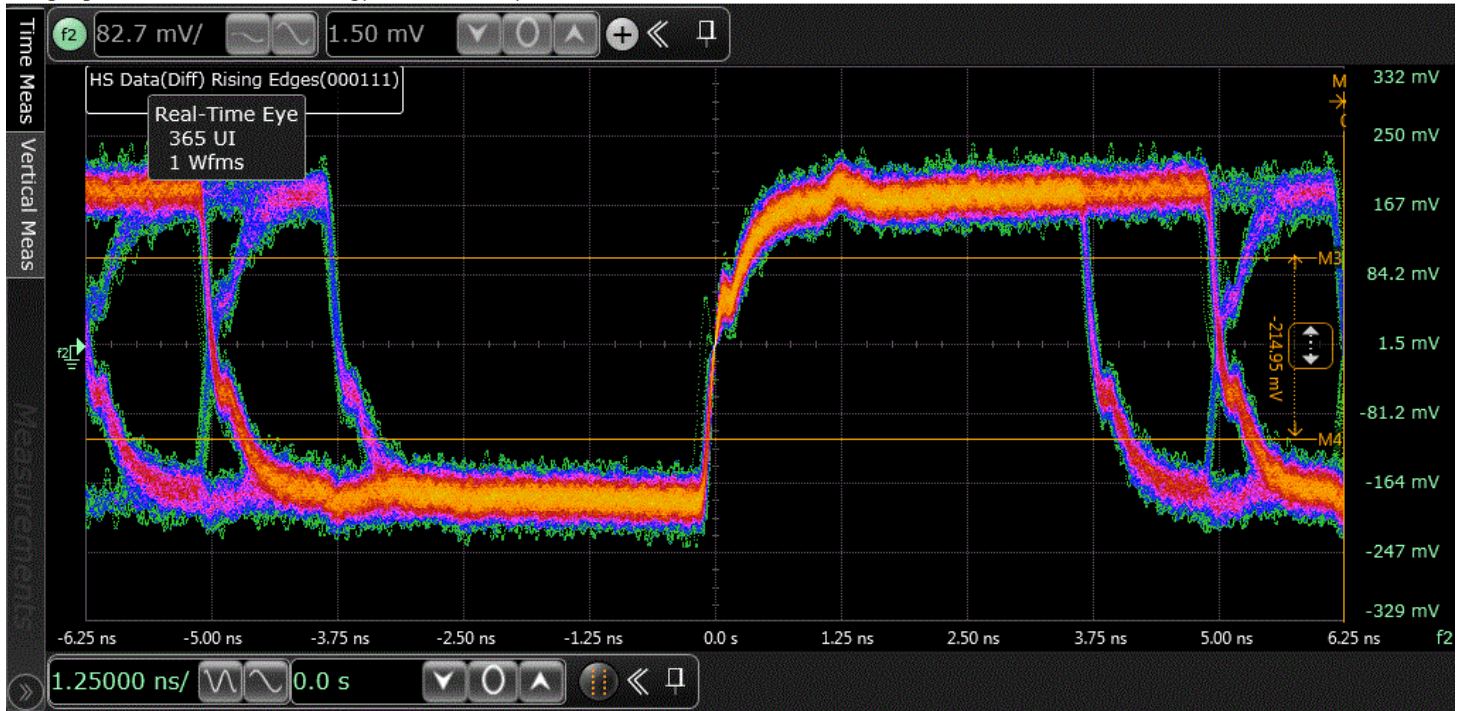
HS TX Risetime(See image)**Transition Time Measurement Lower Threshold(%)**20**Vod(1)**179.13 mV**Vod(0)**-179.13 mV**UIINST(Mean)**1.249993 ns**Number of Measurement**365**ZID**100

ohm**DataLane**Lane1**PassLimit Max (DataRiseTime_LimitMax)**375 ps**Number of HS Burst**1

Trial 1

Trial 1: HS TX Risetime

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✓ 1.3.12 HS Data TX 80%-20% Fall Time (tF)[Burst Data] Reference: D-PHY Specification v1.2
Section 9.1.1 Table 20, CTS v1.2(Test 1.3.12)

Test Summary: Pass **Test Description:** This test is to verify that the 80%-20% fall time of the HS differential signal is less than the maximum conformance limit(DataFallTime_LimitMax). For CTS v1.2, the maximum conformance limit(DataFallTime_LimitMax) is $0.3 \cdot UI$ for Datarate $\leq 1\text{Gbps}$, $0.35 \cdot UI$ for Datarate $> 1\text{Gbps}$ and $\leq 1.5\text{Gbps}$, $0.4 \cdot UI$ for Datarate $> 1.5\text{Gbps}$. This test will measure the fall time based on the reference data patterns(111000) of differential signal. This test is applicable for Burst Data signal only. The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for fall time measurement in this test.

Pass Limits:< DataFallTime_LimitMax s81111_Fall Time373 ps

Result Details:

Result Details

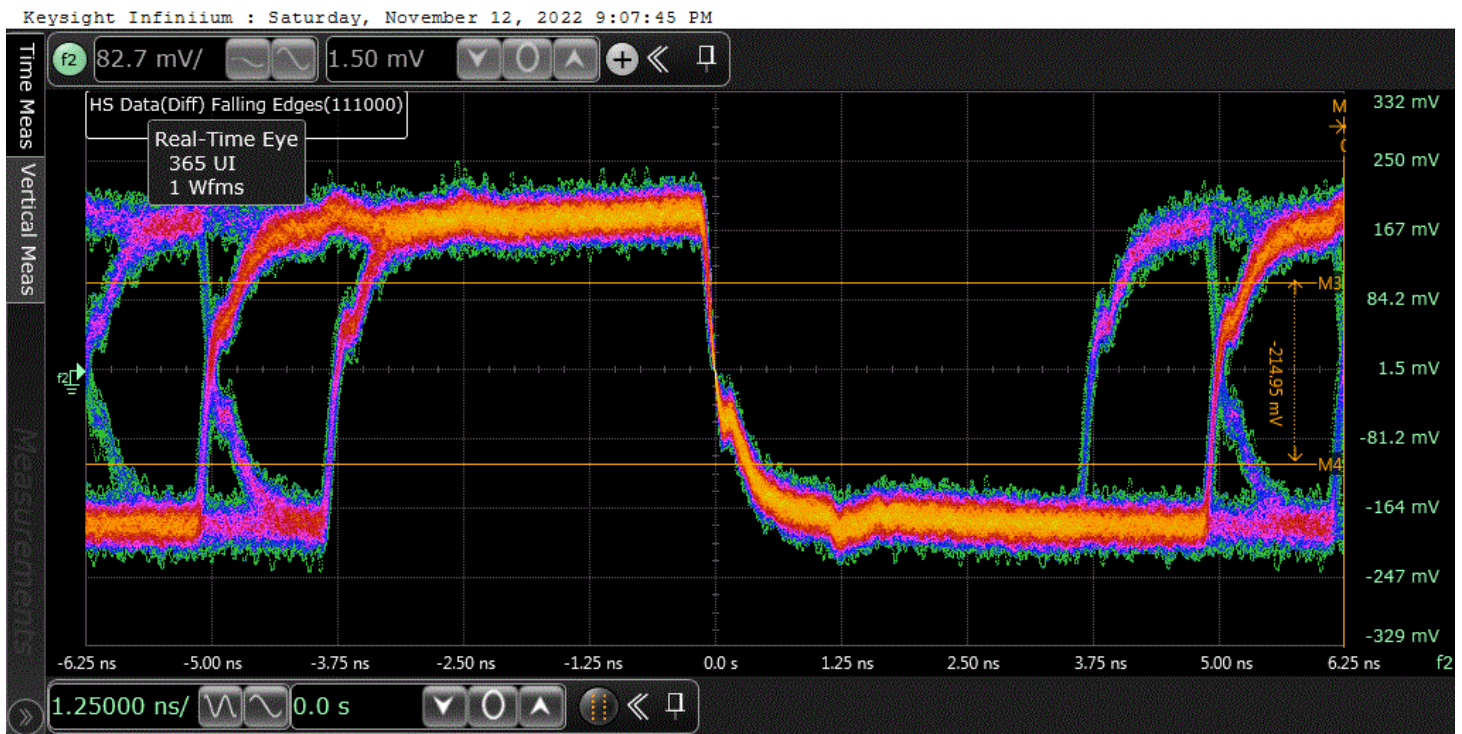
HS TX Falltime(See image)Transition Time Measurement Lower Threshold(%)20Vod(1)179.13

mVVod(0)-179.13 mVUIINST(Mean)1.249993 nsNumber of Measurement365ZID100

ohmDataLaneLane1PassLimit Max (DataFallTime_LimitMax)375 psNumber of HS Burst1

Trial 1

Trial 1: HS TX Falltime



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✓ 1.4.9 HS Clock TX Common-Level Variations Between 50-450MHz (VCMTX(LF)) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.9)

Test Summary: Pass Test Description: Common-level variation between 50-450MHz. This test is only available for CTS v1.2 and CTS v2.0 and v2.1.

Pass Limits: < 25.00 mV 1820_Vcmtx(LF) 10.36 mV

Result Details:

Result Details

Common Level Variations(50-450MHz)(See image) ZID100 ohm Number of HS Burst1

Trial 1

Trial 1: Common Level Variations(50-450MHz)



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✓ 1.4.7 HS Clock TX Static Common Mode Voltage(Vcmtx) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.7)

Test Summary: Pass Test Description: HS transmit static common-mode voltage for Clock.

Pass Limits:[150.00 mV to 250.00 mV]1811_Vcmtx(Worst)192.08 mV

Result Details:

Result Details

HS Clock TX Common Mode Voltage(See image)Vcmtx(Differential-1)200.66 mVNumber of Vcmtx(Differential-1) Measured39.999000 kVcmtx(Differential-0)192.08 mVNumber of Vcmtx(Differential-0) Measured40.000000 kZID100 ohmNumber of HS Burst1

Trial 1

Trial 1: HS Clock TX Common Mode Voltage

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✓ 1.4.8 HS Clock TX Vcmtx Mismatch Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.8)

Test Summary: Pass Test Description: VCMTX mismatch when output is Differential-1 or Differential-0.

Pass Limits:< 5.00 mV1812_Vcmtx Mismatch4.29 mV

Result Details:

Result Details

Vcmtx(Differential-1)200.66 mV**Vcmtx(Differential-0)**192.08 mV**ZID**100 ohm**Number of HS Burst**1

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✓ 1.4.10 HS Clock TX Common-Level Variations Above 450MHz (VCMTX(HF)) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.10)

Test Summary: Pass Test Description: Common-level variations above 450MHz.

Pass Limits:< 15.00 mV1818_Vcmtx(HF)2.50 mV

Result Details:

Result Details

Common Level Variations(>450Mhz)(See image)**ZID100 ohmNumber of HS Burst1**

Trial 1

Trial 1: Common Level Variations(>450Mhz)

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✓ 1.4.4 HS Clock TX Differential Voltage(VOD0 Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)

Test Summary: Pass Test Description: HS clock transmitter differential voltage.

Pass Limits: [-270.00 mV to -140.00 mV]18131_Vod0(Mean)-175.60 mV

Result Details:

Result Details

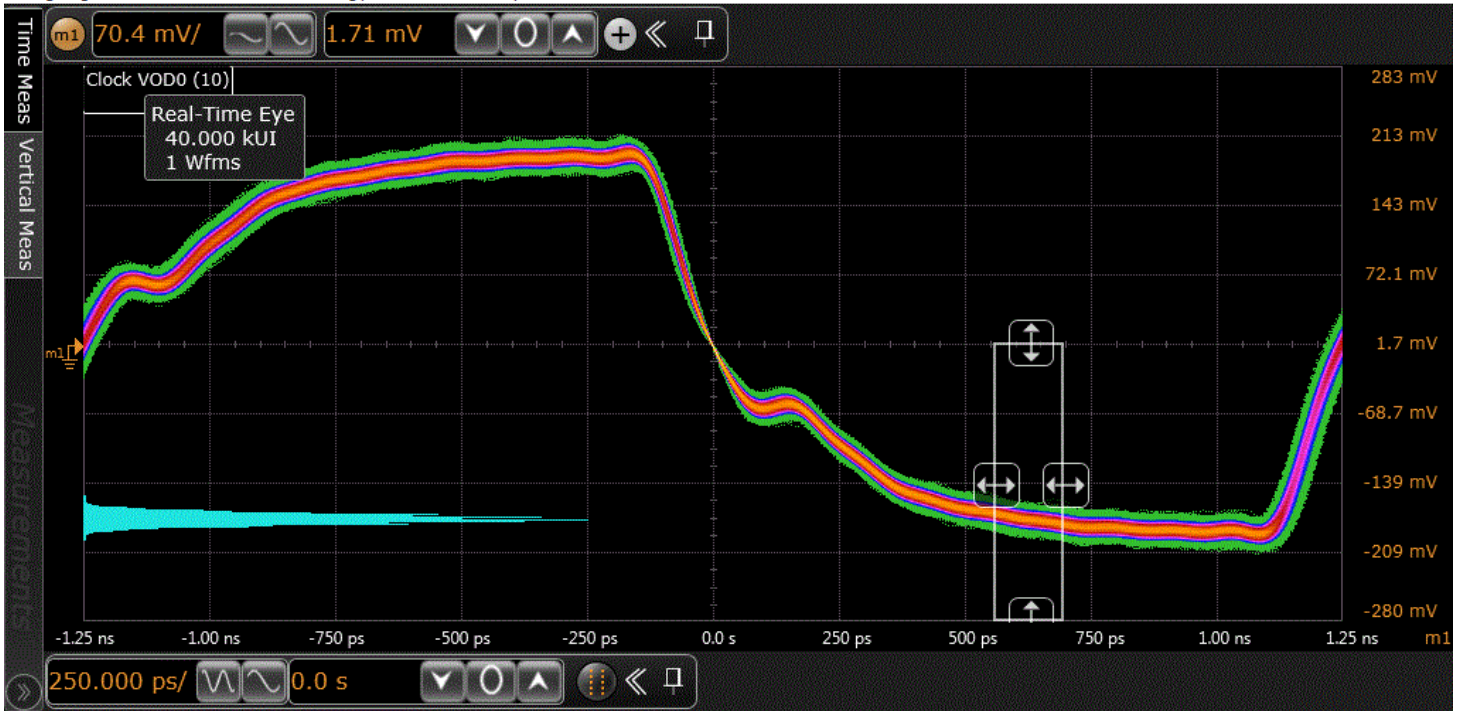
Clock VOD0 (10)(See image)**Vod(Differential-0)-175.60 mVNumber of measurement40.000000**

kZID100 ohmNumber of HS Burst1

Trial 1

Trial 1: Clock VOD0 (10)

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✓ 1.4.4 HS Clock TX Differential Voltage(VOD1 Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.4)

Test Summary: Pass Test Description: HS clock transmitter differential voltage.

Pass Limits:[140.00 mV to 270.00 mV]18132_Vod1(Mean)178.70 mV

Result Details:

Result Details

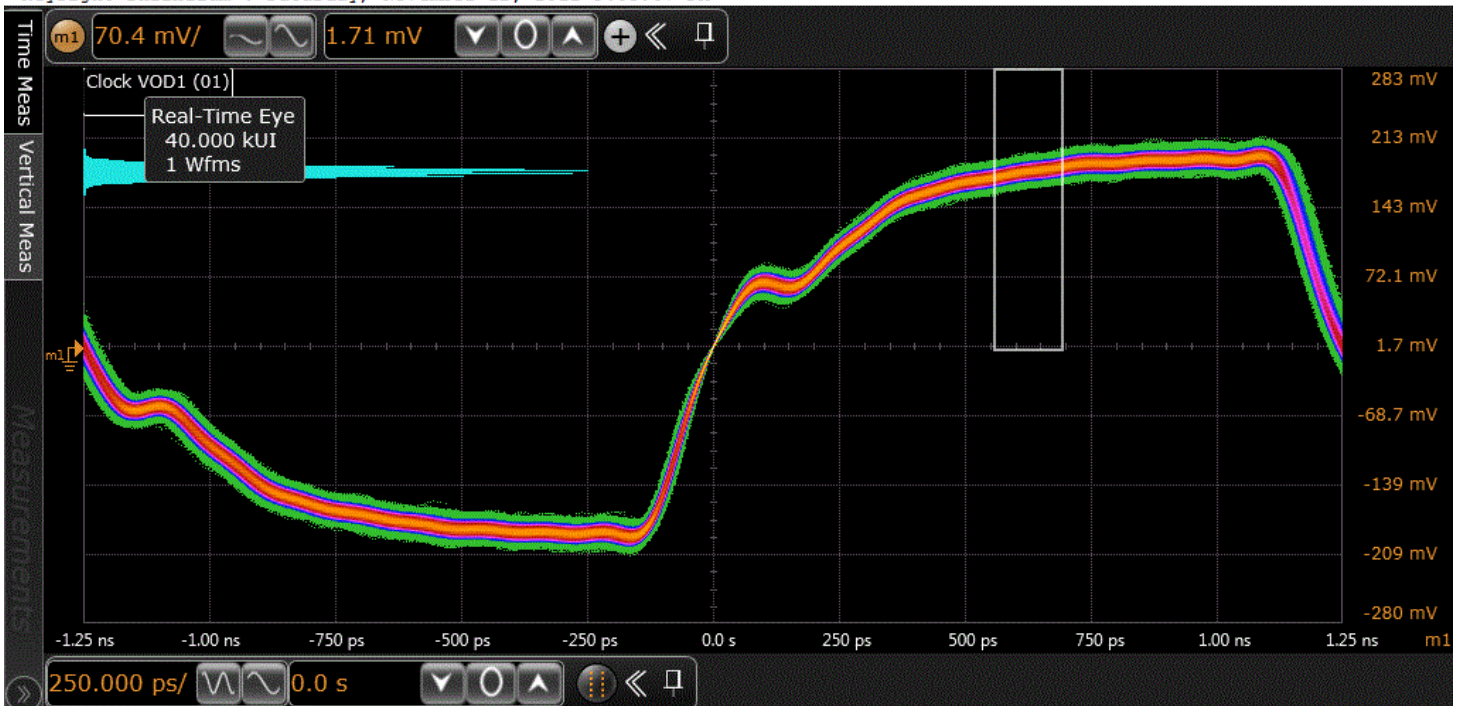
Clock VOD1 (01)(See image)Vod(Differential-1)178.70 mVNumber of measurement40.000000

kZID100 ohmNumber of HS Burst1

Trial 1

Trial 1: Clock VOD1 (01)

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✓ 1.4.5 HS Clock TX Differential Voltage Mismatch (Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.5)

Test Summary: Pass Test Description: VOD mismatch when output is Differential-1 or Differential-0.

Pass Limits:< 14.00 mV18141_Vod Mismatch3.10 mV

Result Details:

Result Details

Vod(Differential-1)178.70 mV**Vod(Differential-0)**-175.60 mV**ZID**100 ohm**Number of HS Burst**1

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✓ 1.4.6 HS Clock TX Single Ended Output High Voltage(VOHHS Pulse) Reference: D-PHY Specification v1.2 Section 9.1.1 Table 19, CTS v1.2(Test 1.4.6)

Test Summary: Pass Test Description: HS Single Ended output high voltage.

Pass Limits:<= 360.00 mV18151_Vohhs(Worst)291.78 mV

Result Details:

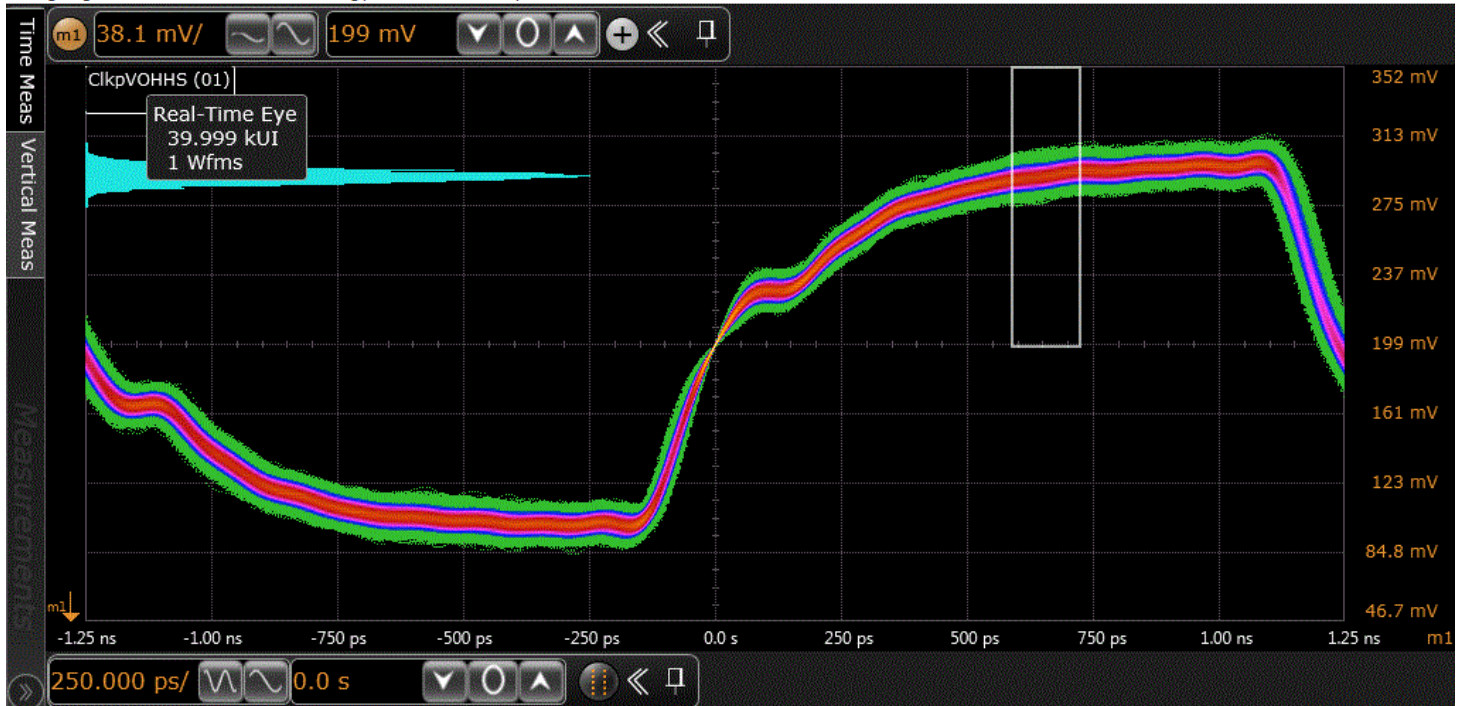
Result Details

ClkpVOHHS (01)(See image)**ClknVOHHS (01)**(See image)**Vohhs(Clkp)**291.78 mV**Vohhs(Clkn)**283.35 mV**Number of measurement Vohhs(Clkp)**39.999000 k**Number of measurement Vohhs(Clkn)**40.000000 k**ZID**100 ohm**Number of HS Burst**1

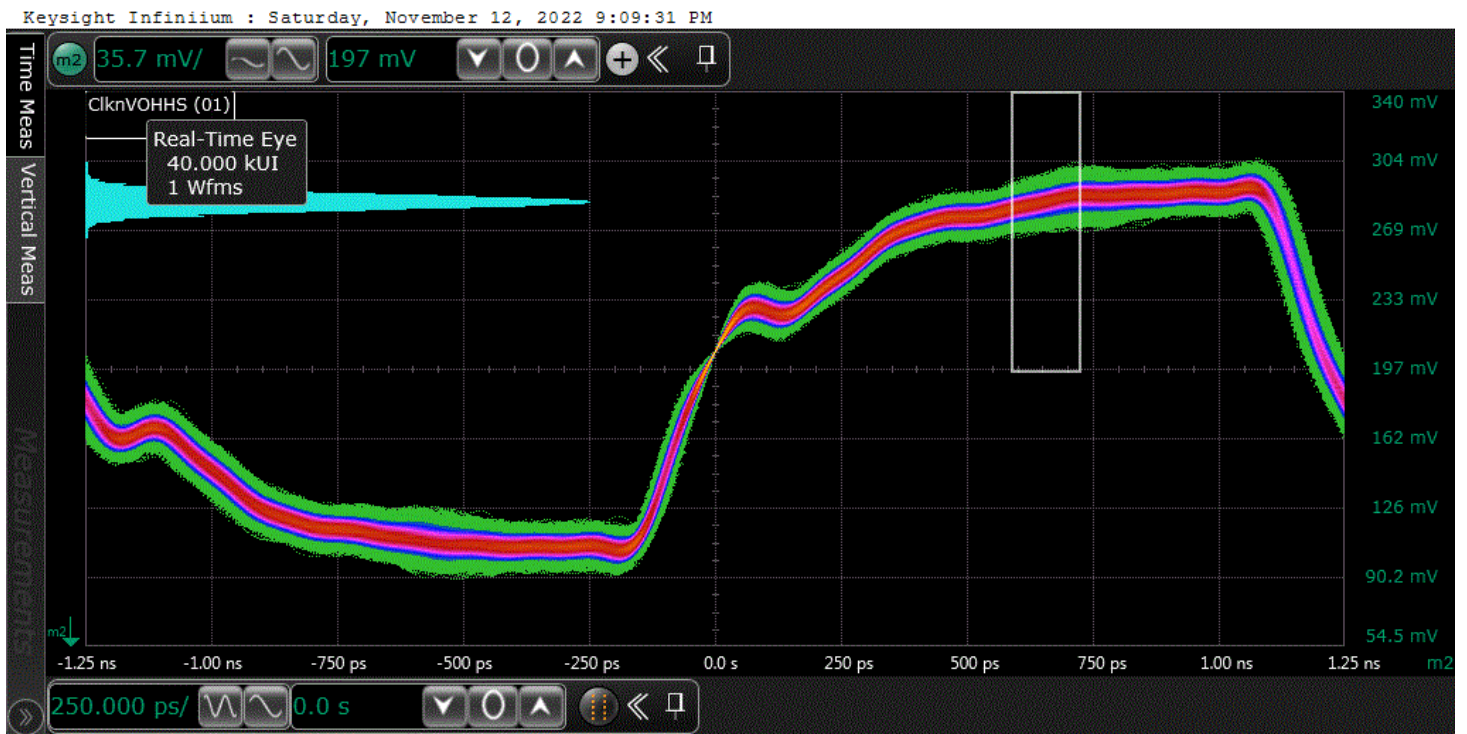
Trial 1

Trial 1: ClkpVOHHS (01)

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Trial 1: ClknVOHHS (01)



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✓ 1.4.11 HS Clock TX 20%-80% Rise Time (tR)[Continuous Clock, Burst Data] Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.11)

Test Summary: Pass **Test Description:** This test is to verify that the 20%-80% rise time of the HS differential signal is less than the maximum conformance limit(CLKRiseTime_LimitMax). For CTS v1.2, the maximum conformance limit(CLKRiseTime_LimitMax) is $0.3 \cdot UI$ for Datarate ≤ 1 Gbps, $0.35 \cdot UI$ for Datarate > 1 Gbps and ≤ 1.5 Gbps, $0.4 \cdot UI$ for Datarate > 1.5 Gbps. This test is applicable for Continuous Clock and Burst Data signal only. The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for rise time measurement in this test.

Pass Limits: $< CLKRiseTime_LimitMax$ s181102_Rise Time340 ps

Result Details:

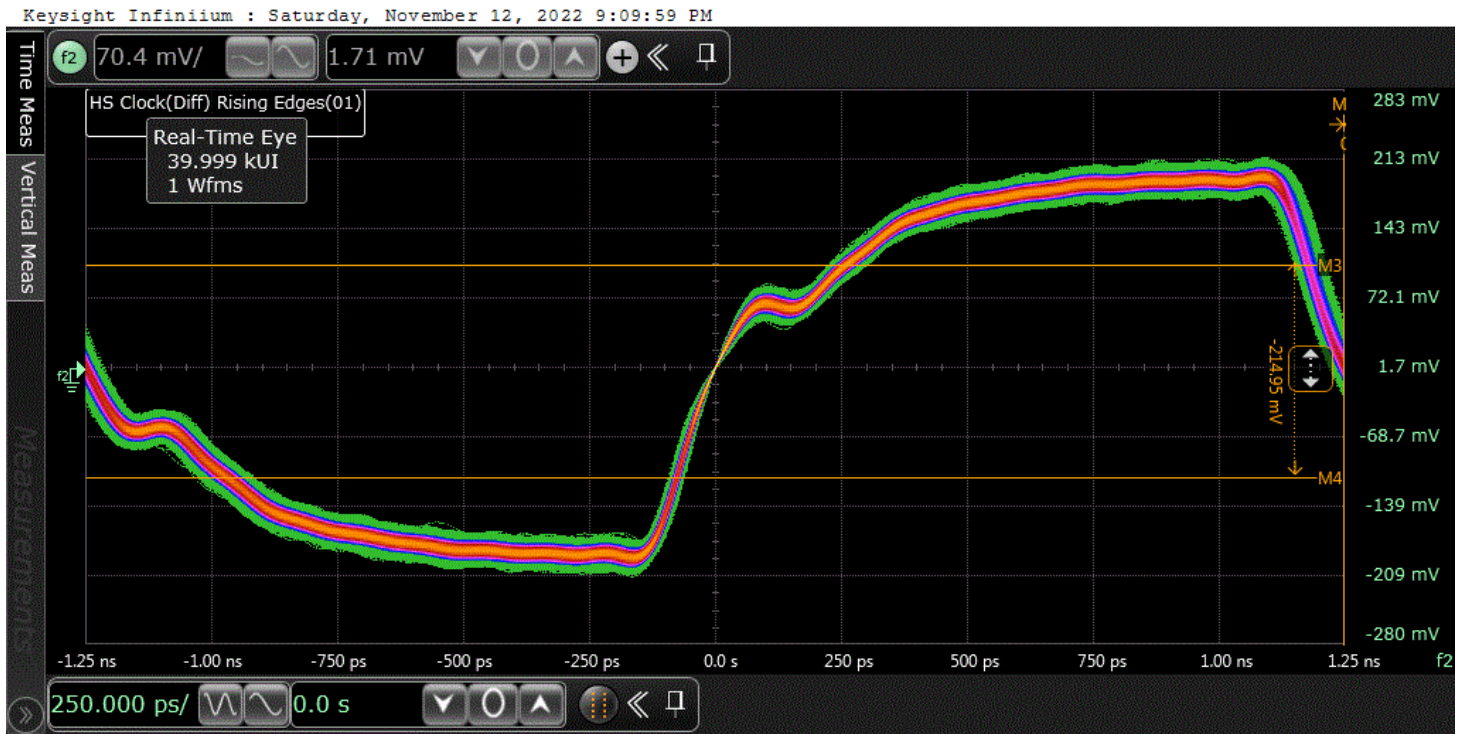
Result Details

HS Clock TX Risetime(See image)Transition Time Measurement Lower

Threshold(%)20Vod(1)179.13 mVVod(0)-179.13 mVUIINST(Mean)1.249993 nsNumber of Measurement39.999 kZID100 ohmPassLimit Max (CLKRiseTime_LimitMax)375 psNumber of HS Burst1

Trial 1

Trial 1: HS Clock TX Risetime



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✓ 1.4.12 HS Clock TX 80%-20% Fall Time (tF)[Continuous Clock, Burst Data] Reference: D-PHY Specification v1.2 Section 9.1.1 Table 20, CTS v1.2(Test 1.4.12)

Test Summary: Pass **Test Description:** This test is to verify that the 80%-20% fall time of the HS differential signal is less than the maximum conformance limit(CLKFallTime_LimitMax). For CTS v1.2, the maximum conformance limit(CLKFallTime_LimitMax) is $0.3 \cdot UI$ for Datarate ≤ 1 Gbps, $0.35 \cdot UI$ for Datarate > 1 Gbps and ≤ 1.5 Gbps, $0.4 \cdot UI$ for Datarate > 1.5 Gbps. This test is applicable for Continuous Clock and Burst Data signal only. The VHS_ZERO level measured from Data Lane will be used to calculate 20/80% reference voltage for fall time measurement in this test.

Pass Limits: < CLKFallTime_LimitMax s181112_Fall Time346 ps

Result Details:

Result Details

HS Clock TX Falltime(See image)Transition Time Measurement Lower

Threshold(%)20Vod(1)179.13 mVVod(0)-179.13 mVUIINST(Mean)1.249993 nsNumber of Measurement40.000 kZID100 ohmPassLimit Max (CLKFallTime_LimitMax)375 psNumber of HS Burst1

Trial 1

Trial 1: HS Clock TX Falltime

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✓ 1.4.17 HS Clock Instantaneous (U_{inst})(Min) Reference: D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.17)

Test Summary: Pass Test Description: Minimum UI instantaneous (Min) of HS Clock.

Pass Limits: $\geq$ U_{inst_Min_Limit} s914_U_{inst}(Min)1.212 ns

Result Details:

Result Details

UIINST(Min)1.211870 ns**UIINST(Mean)**1.249993 ns**Number of UI**79.999000 k**ZID**100

ohm**DataLane**Lane1**PassLimit Min (U_{inst_Min_Limit})**0.000000000000 s**Number of HS Burst**1

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✓ 1.4.18 Clock Lane HS Clock Delta UI (UI variation) Reference: D-PHY Specification v1.2 Section 10.1 Table 29, CTS v1.2(Test 1.4.18)

Test Summary: Pass Test Description: This test is to verify that the Clock lane HS Clock Delta UI is in between the minimum conformance limit(U_{Variant_Limit_Min}) and the maximum conformance limit(U_{Variant_Limit_Max}). For CTS v1.1, U_{Variant_Limit_Min} is -10% and U_{Variant_Limit_Max} is 10% for Datarate $\leq$ 1Gbps, U_{Variant_Limit_Min} is -5% and U_{Variant_Limit_Max} is 5% for Datarate $>$ 1Gbps. For CTS v1.2, U_{Variant_Limit_Min} is -10% and U_{Variant_Limit_Max} is 10% for Datarate $\leq$ 1Gbps, U_{Variant_Limit_Min} is -5% and U_{Variant_Limit_Max} is 5% for Datarate $>$ 1Gbps and $\leq$ 1.5Gbps .

Pass Limits:[U_{Variant_Limit_Min} % to U_{Variant_Limit_Max} %]1911_U_{Variant}(Min)3.21 %

Result Details:

Result Details

UIINST(Min)1.211870 ns**UIINST(Max)**1.290170 ns**UIINST(Mean)**1.249993 ns**Number of**

UI79.999000 k**DataLane**Lane1**UIVariant_min**-3.050 %**UIVariant_max**3.214 %**ZID**100 ohm**PassLimit**

Min (UIVariant_Limit_Min)-10.00 %**PassLimit Max (UIVariant_Limit_Max)**10.00 %**Number of HS Burst**1

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✓ 1.3.1 HS Entry: DATA TLPX Reference: D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.1)

Test Summary: Pass Test Description: Length of any Low-Power state period.

Pass Limits: ≥ 50.00 ns511_TLPX59.95 ns

Result Details:

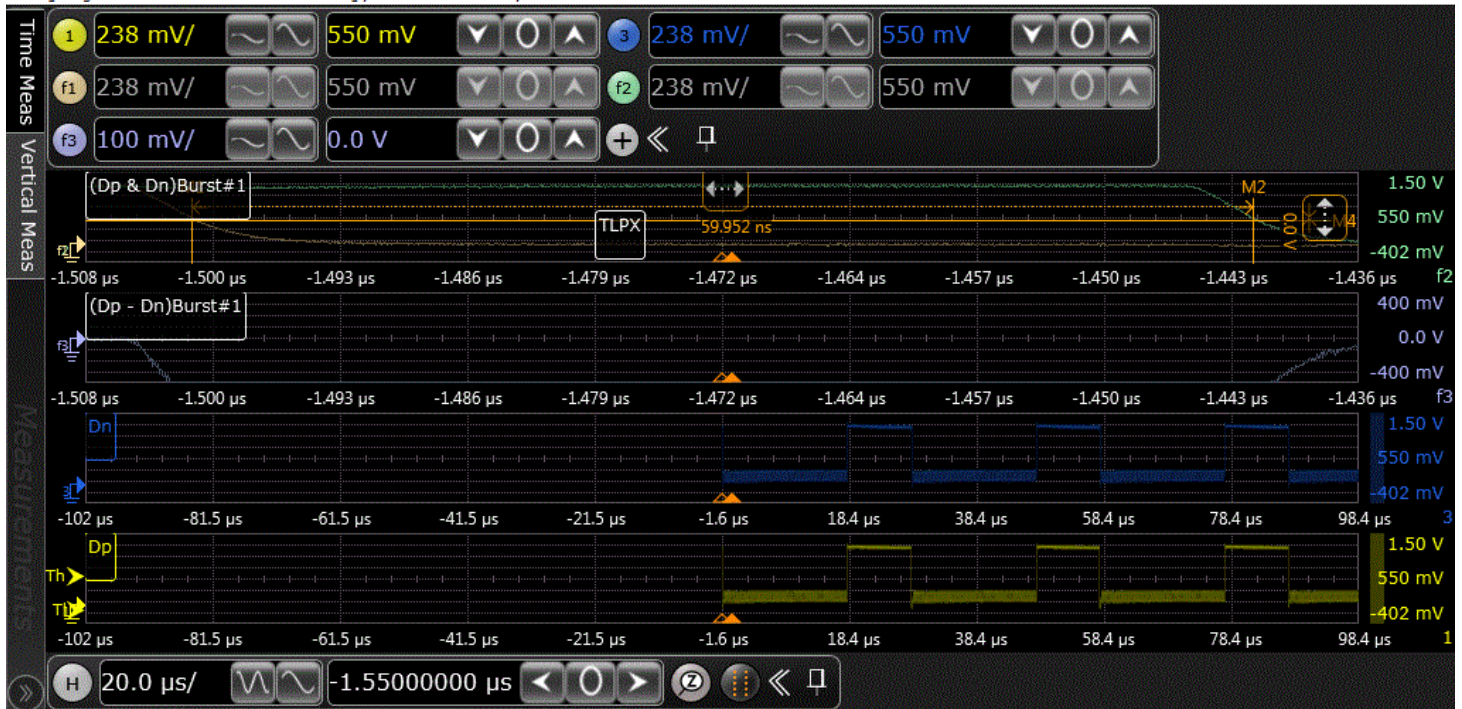
Result Details

TLPX(See image)**ZID**100 ohm**DataLane**Lane1**Number of HS burst**1

Trial 1

Trial 1: TLPX

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✓ 1.3.2 HS Entry: DATA TX THS-PREPARE Reference: D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.2)

Test Summary: Pass Test Description: Time to drive LP-00 to prepare for HS Transmission.

THSPrepare_LimitMin is based on $40\text{ns} + 4 \cdot \text{UI}$. THSPrepare_LimitMax is based on $85\text{ns} + 6 \cdot \text{UI}$.

Pass Limits:[THSPrepare_LimitMin s to THSPrepare_LimitMax s]557_THS-PREPARE66.30 ns

Result Details:

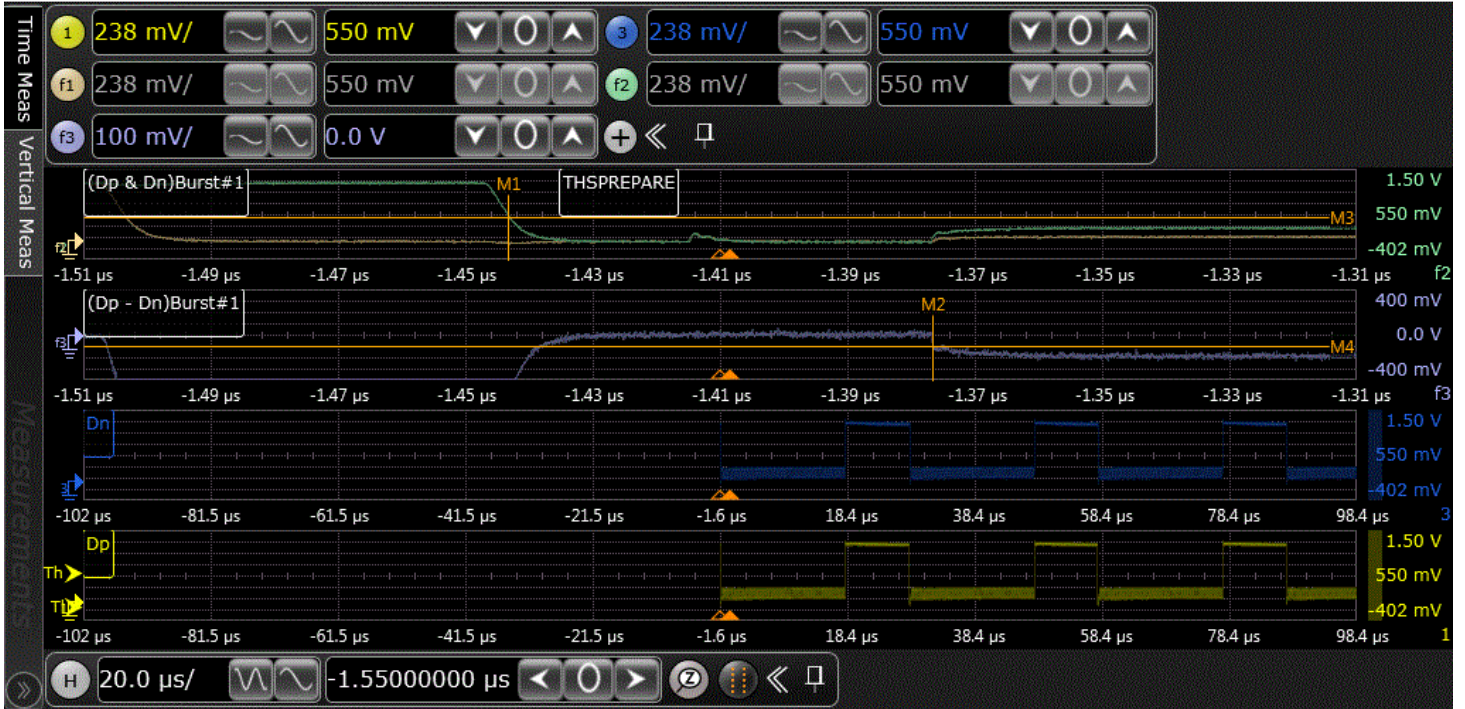
Result Details

THSPREPARE(See image)**UIINST(Mean)**1.249993 ns**ZID**100 ohm**DataLane**Lane1**PassLimit Min (THSPrepare_LimitMin)**45.00 ns**PassLimit Max (THSPrepare_LimitMax)**92.50 ns**Number of HS burst**1

Trial 1

Trial 1: THSPREPARE

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✓ 1.3.13 HS Exit: DATA TX THS-TRAIL Reference: D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.13)

Test Summary: Pass **Test Description:** Time to drive flipped differential state after last payload data bit of a HS transmission burst. TXTHSTrail_LimitMin is based on $60\text{ns} + n \cdot 4 \cdot \text{UI}$. The THS-SKIP parameter is useful to avoid glitch problem during THS-TRAIL measurement. Any transition on the Data Lane in THS-SKIP time interval will be ignored when finding last payload data bit of HS transmission burst. The default value of THS-SKIP is set to 0s to prevent invalid THS-TRAIL measurement.

Pass Limits: $\geq$ TXTHSTrail_LimitMin s546_THS-TRAIL80.67 ns

Result Details:

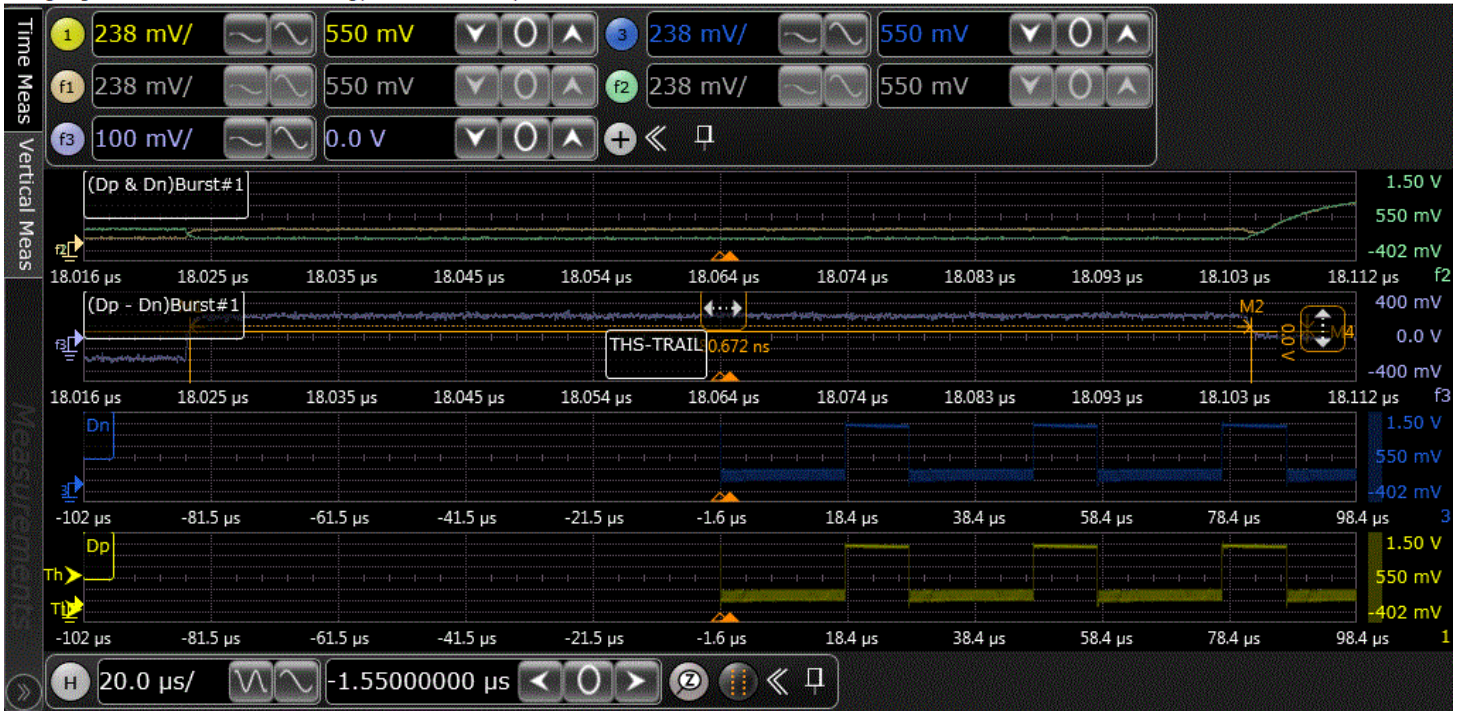
Result Details

THSTRAIL(See image)**THS-SKIP(s)**0.00000000000000 s**ZID**100 ohm**DataLane**Lane1**PassLimit Min**
(TXTHSTrail_LimitMin)65.00 ns**Number of HS burst**1

Trial 1

Trial 1: THSTRAIL

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✓ 1.3.14 HS Exit: DATA TX TREOT Reference: D-PHY Specification v1.2 Section 9.1.2 Table 22, CTS v1.2(Test 1.3.14)

Test Summary: Pass Test Description: 30%-85% rise time and fall time

Pass Limits: ≤ 35.00 ns 549_TREOT 8.99 ns

Result Details:

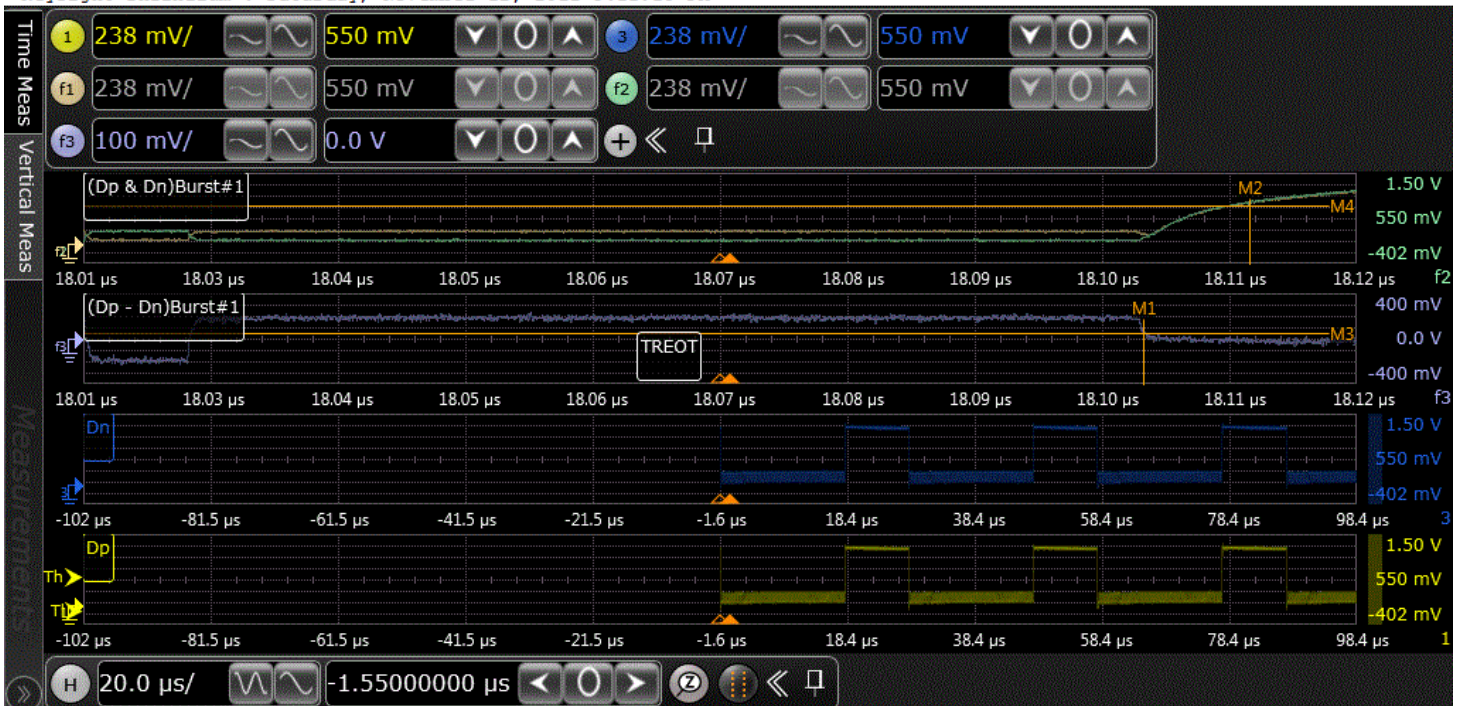
Result Details

TREOT(See image) ZID100 ohm Data Lane Lane1 Number of HS burst1

Trial 1

Trial 1: TREOT

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✓ 1.3.15 HS Exit: DATA TX TEOT Reference: D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.15)

Test Summary: Pass Test Description: Time from start of THS-TRAIL period to start of LP-11 state. TXTEOT_LimitMax is based on $105\text{ns} + n \cdot 12 \cdot \text{UI}$.

Pass Limits: $\leq \text{TXTEOT_LimitMax}$ s547_TEOT89.66 ns

Result Details:

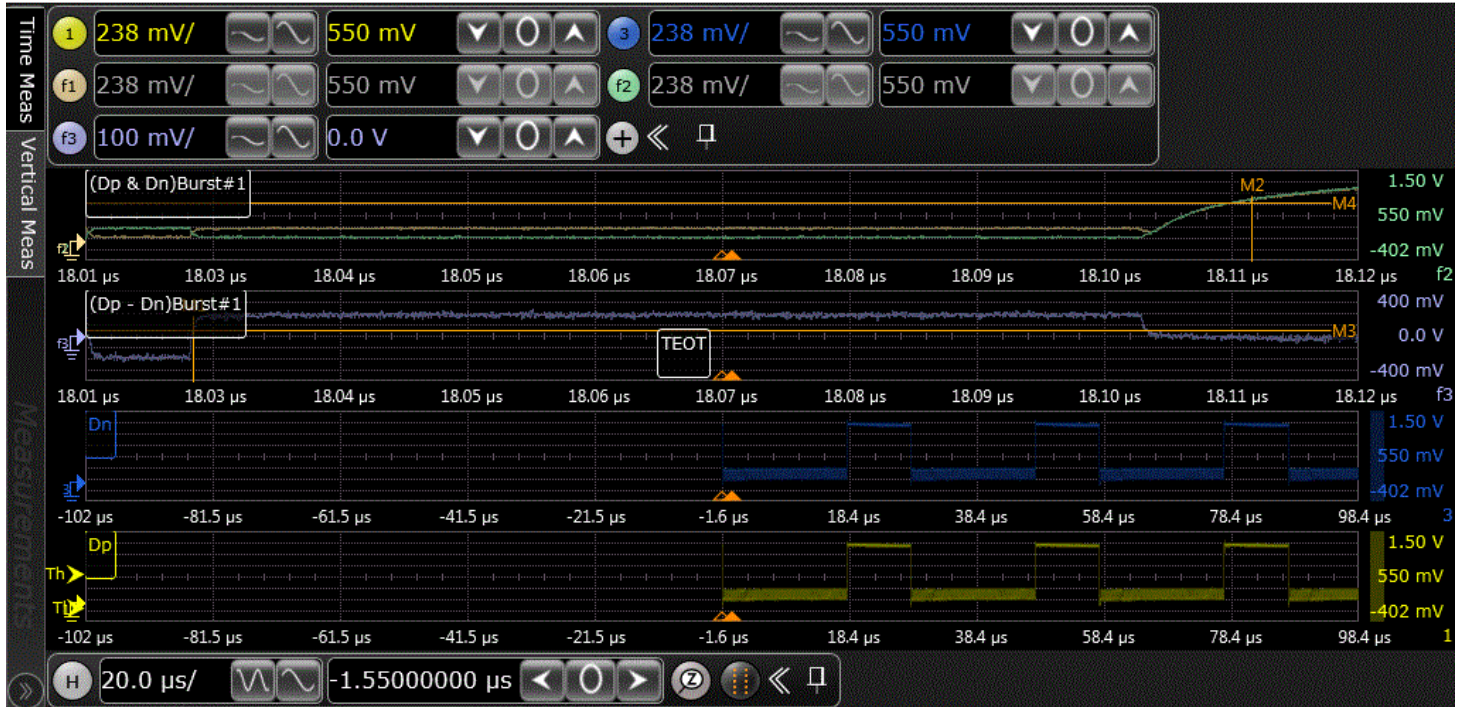
Result Details

TEOT(See image)UIINST(Mean)1.249993 nsZID100 ohmDataLaneLane1PassLimit Max (TXTEOT_LimitMax)120.00 nsNumber of HS burst1

Trial 1

Trial 1: TEOT

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✓ 1.3.16 HS Exit: DATA TX THS-EXIT Reference: D-PHY Specification v1.2 Section 6.9 Table 14, CTS v1.2(Test 1.3.16)

Test Summary: Pass Test Description: Time to drive LP-11 after HS burst.

Pass Limits: ≥ 100.00 ns548_THS-EXIT9.97388 μs

Result Details:

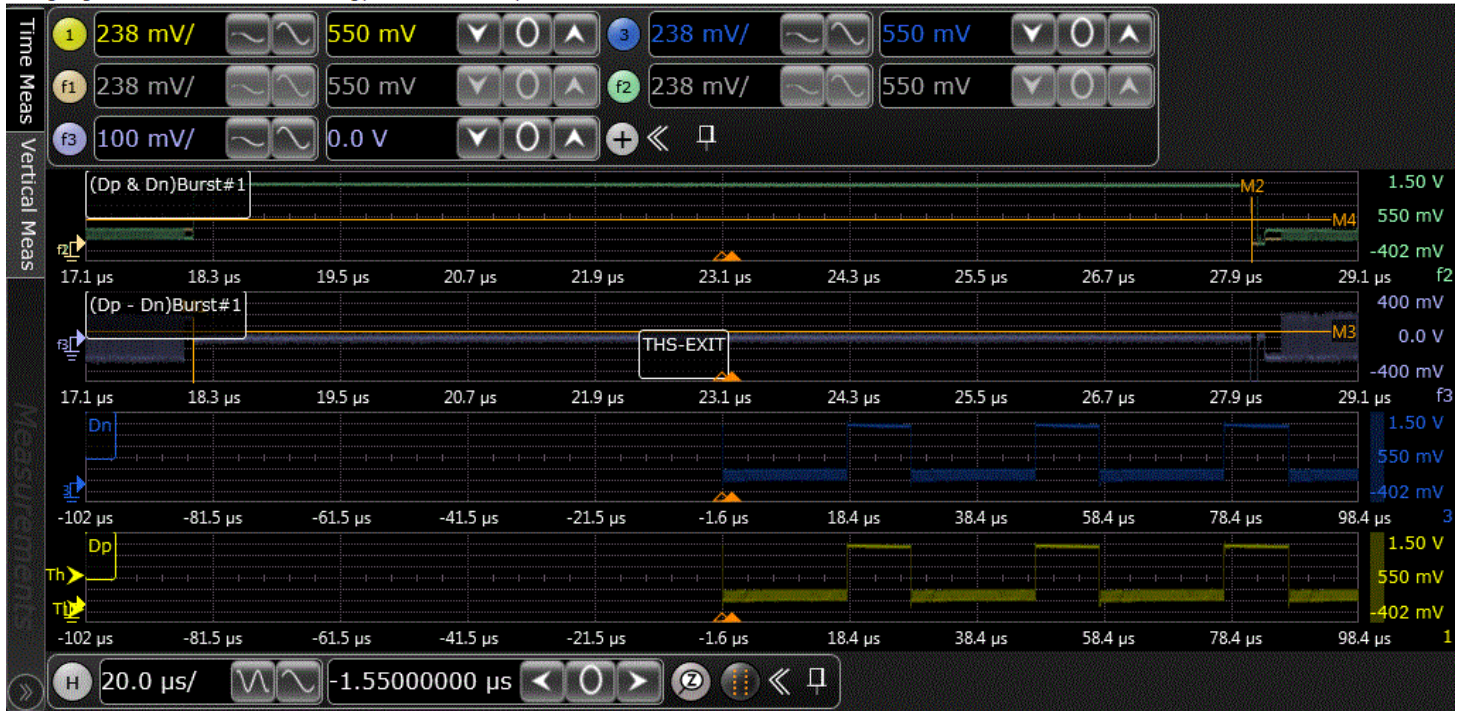
Result Details

THSEXIT(See image)ZID100 ohmDataLaneLane1Number of HS burst1

Trial 1

Trial 1: THSEXIT

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✓ 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit Reference: D-PHY Specification v1.2 Section 10.2, CTS v1.2(Test 1.5.3)

Test Summary: Pass **Test Description:** Test will pass when there is a rising edge during the first payload bit. "First Payload Bit Alignment" will be set to "PASS" ONLY when a rising edge is detected during the first payload bit.

Pass Limits: <= 500.000000000 m912_First Payload Bit AlignmentPass

Result Details:

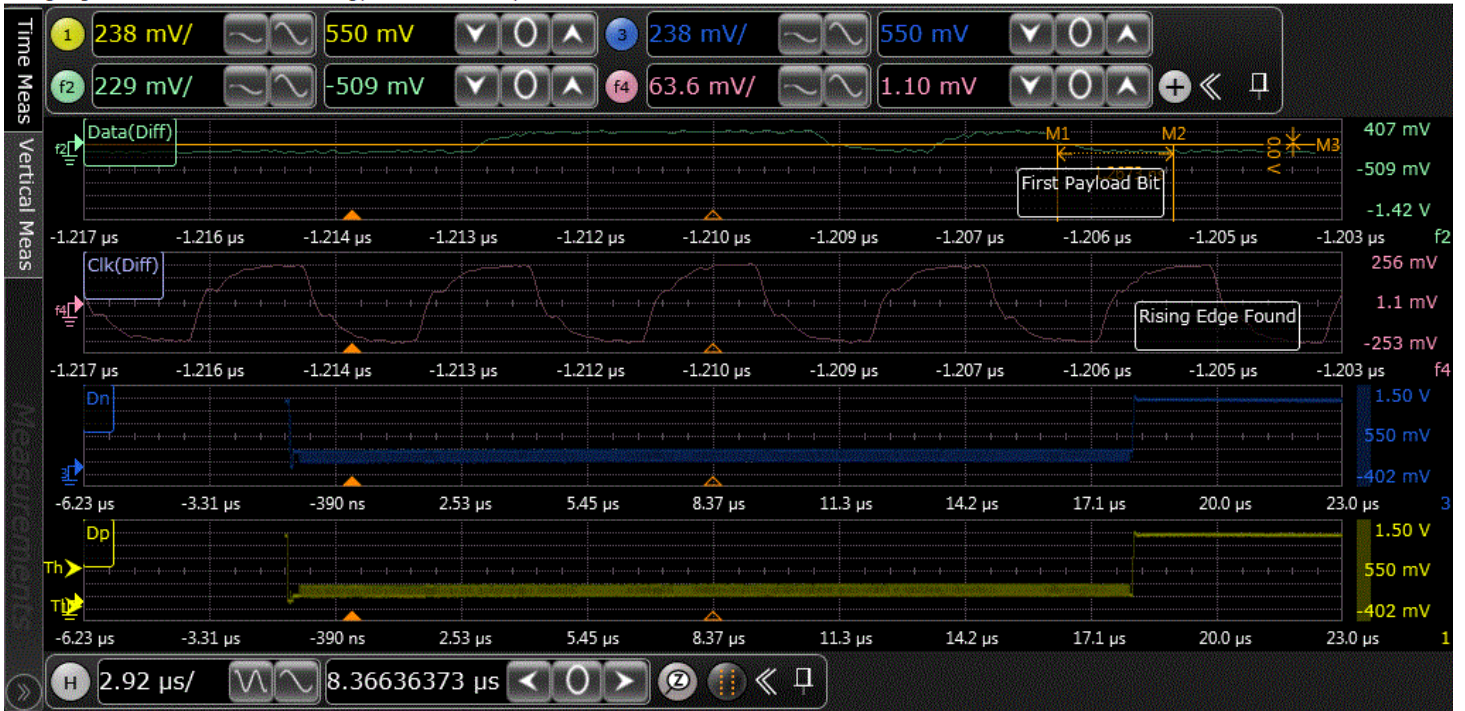
Result Details

First Payload Bit Clock Alignment(See image)ZID100 ohmDataLaneLane1Number of HS Burst1

Trial 1

Trial 1: First Payload Bit Clock Alignment

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✖ 1.5.4 Data-to-Clock Skew (TSKEW(TX))(Max,Min) Reference: D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Test Summary: FAIL Test Description: Data to Clock Skew [measured at transmitter].

Pass Limits:[MinMaxTSkewTest_LimitMin Ulinst to MinMaxTSkewTest_LimitMax

Ulinst]913_Tskew(Worst)-170 mUlinst

Result Details:

Result Details

LeftCrossing(See image)UIINST(Mean)1.2500 nsTSkew(Min)-212.9 psTSkew(Max)52.7 psNo Of

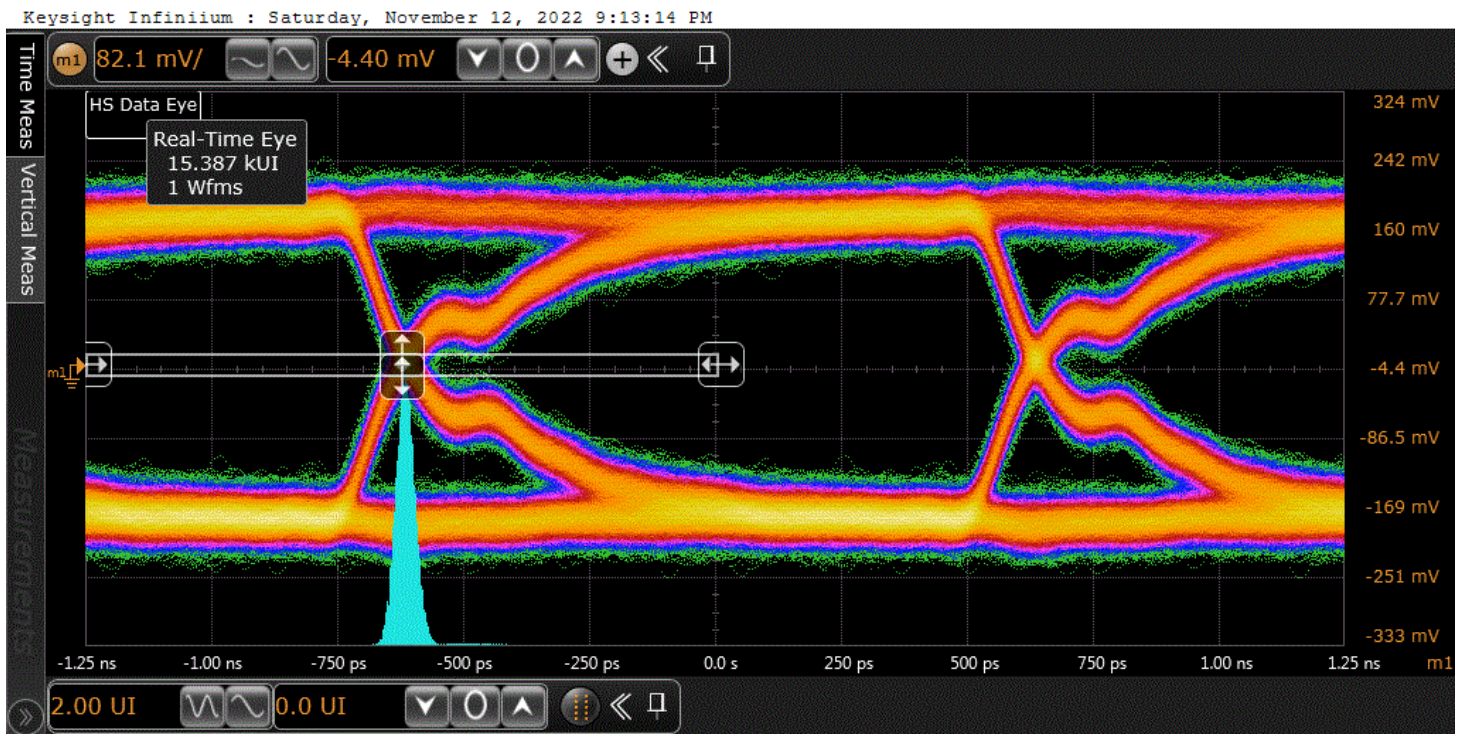
Measurement15.387000 kZID100 ohmDataLaneLane1PassLimit Min

(MinMaxTSkewTest_LimitMin)-150 mUlinstPassLimit Max (MinMaxTSkewTest_LimitMax)150

mUlinstNumber of HS Burst1

Trial 1

Trial 1: LeftCrossing



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✓ 1.5.4 Data-to-Clock Skew (TSKEW(TX))(Mean) Reference: D-PHY Specification v1.2 Section 10.2.1 Table 30, CTS v1.2(Test 1.5.4)

Test Summary: Pass Test Description: Data to Clock Skew [measured at transmitter].

Pass Limits:[MeanTSkewTest_LimitMin UIinst to MeanTSkewTest_LimitMax

UIinst]9131_Tskew(Mean)-10 mUIinst

Result Details:

Result Details

UIINST(Mean)1.2500 nsTSkew(Mean)-13.0 psNo Of Measurement15.387000 kZID100

ohmDataLaneLane1PassLimit Min (MeanTSkewTest_LimitMin)-150 mUIinstPassLimit Max (MeanTSkewTest_LimitMax)150 mUIinstNumber of HS Burst1

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