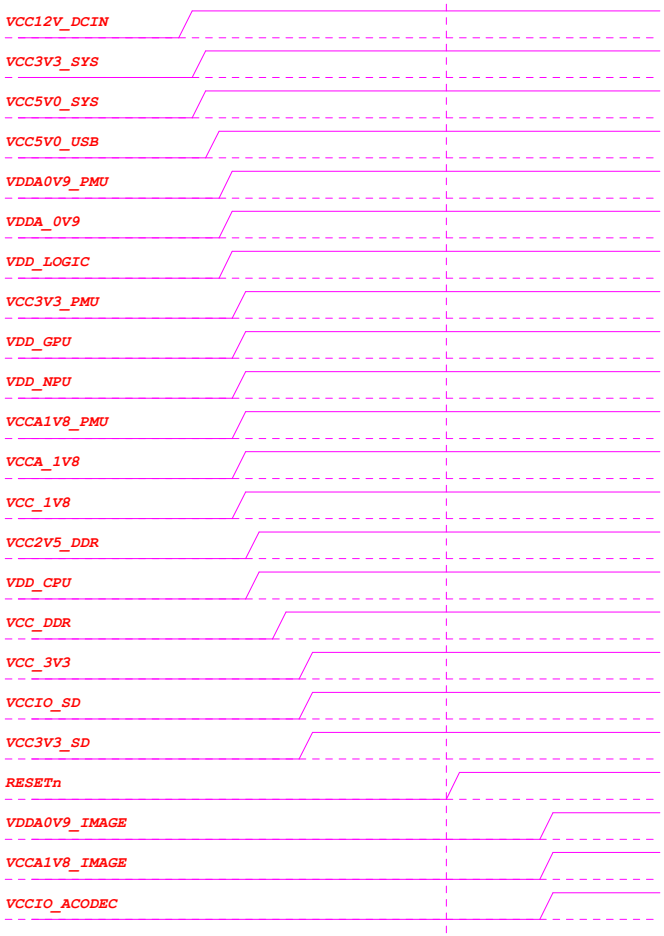
# Power Sequence




| Power Supply | PMIC Channel | Supply limit | Power Name | Time Slot | Default Voltage | Default ON/OFF | Sleep ON/OFF | Peak Current | Sleep Current |
|---|---|---|---|---|---|---|---|---|---|
| VCC3V3_SYS | RK809_BUCK1 | 2.5A | VDD_LOGIC | Slot:1 | 0.9V | ON | OFF | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK2 | 2.5A | VDD_GPU | Slot:2 | 0.9V | ON | OFF | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK3 | 1.5A | VCC_DDR | Slot:3 | ADJ FB=0.8V | ON | ON | TBD | TBD |
| VCC3V3_SYS | RK809_BUCK4 | 1.5A | VDD_NPU | N/A | 0.9V | OFF | OFF | TBD | TBD |
| VCC3V3_SYS | RK809_LDO1 | 0.4A | VDDA0V9_IMAGE | N/A | 0.9V | OFF | OFF | TBD | TBD |
| | RK809_LDO2 | 0.4A | VDDA_0V9 | Slot:1 | 0.9V | ON | OFF | TBD | TBD |
| | RK809_LDO3 | 0.1A | VDDA0V9_PMU | Slot:1 | 0.9V | ON | ON | TBD | TBD |
| VCC3V3_SYS | RK809_LDO4 | 0.4A | VCCIO_ACODEC | N/A | 3.3V | OFF | OFF | TBD | TBD |
| | RK809_LDO5 | 0.4A | VCCIO_SD | Slot:4 | 3.3V | ON | OFF | TBD | TBD |
| | RK809_LDO6 | 0.4A | VCC3V3_PMU | Slot:2 | 3.3V | ON | ON | TBD | TBD |
| VCC3V3_SYS | RK809_LDO7 | 0.4A | VCCA_1V8 | Slot:2 | 1.8V | ON | OFF | TBD | TBD |
| | RK809_LDO8 | 0.4A | VCCA1V8_PMU | Slot:2 | 1.8V | ON | ON | TBD | TBD |
| | RK809_LDO9 | 0.4A | VCCA1V8_IMAGE | N/A | 1.8V | OFF | OFF | TBD | TBD |
| VCC3V3_SYS | RK809_SW2 100mohm | 2.1A | VCC3V3_SD | Slot:4 | 3.3V | ON | OFF | TBD | TBD |
| VCC3V3_SYS | RK809_SW1 90mohm | 2.1A | VCC_3V3 | Slot:4 | 3.3V | ON | OFF | TBD | TBD |
| | RK809_BUCK5 | 2.5A | VCC_1V8 | Slot:2 | 1.8V | ON | OFF | TBD | TBD |
| | RK809_RESETn | | | Slot:4+5 | | | | | |
| VCC12V_DCIN | EXT BUCK | 3.0A | VCC3V3_SYS | Slot:0 | 3.3V | ON | ON | TBD | TBD |
| VCC12V_DCIN | EXT BUCK | 3.0A | VCC5V0_SYS | Slot:0 | 5.0V | ON | OFF | TBD | TBD |
| VCC5V0_SYS | EXT BUCK | 6.0A | VDD_CPU | Slot:2A | 1.025V | ON | OFF | TBD | TBD |
| VCC3V3_SYS | EXT LDO | 0.3A | VCC2V5_DDR | Slot:2A | 2.5V | ON | ON | TBD | TBD |
| | | | | | | | | | |

# IO Power Domain Map

# Updates must be Revision accordingly!

| IO Domain | Pin Num | Support IO Voltage 3.3V | Support IO Voltage 1.8V | Actual assigned IO Domain Voltage Supply Power Net Name | Power Source | Voltage | Notes |
|---|---|---|---|---|---|---|---|
| PMUIO1 | Pin Y20 | ✓ | ✗ | VCC3V3_PMU | VCC3V3_PMU | 3.3V | |
| PMUIO2 | Pin W19 | ✓ | ✓ | VCC3V3_PMU | VCC3V3_PMU | 3.3V | |
| VCCIO1 | Pin H17 | ✓ | ✓ | VCCIO_ACODEC | VCCIO_ACODEC | 3.3V | |
| VCCIO2 | Pin H18 | ✓ | ✓ | VCCIO_FLASH | VCC_1V8 | 1.8V | PIN "FLASH_VOL_SEL" must be logic High<br>if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low |
| VCCIO3 | Pin L22 | ✓ | ✓ | VCCIO_SD | VCCIO_SD | 3.3V | |
| VCCIO4 | Pin J21 | ✓ | ✓ | VCCIO4 | VCC_1V8 | 1.8V | |
| VCCIO5 | Pin V10<br>Pin V11 | ✓ | ✓ | VCCIO5 | VCC_3V3 | 3.3V | |
| VCCIO6 | Pin R9<br>Pin U9 | ✓ | ✓ | VCCIO6 | VCC_1V8 | 1.8V | |
| VCCIO7 | Pin V12 | ✓ | ✓ | VCCIO7 | VCC_3V3 | 3.3V | |

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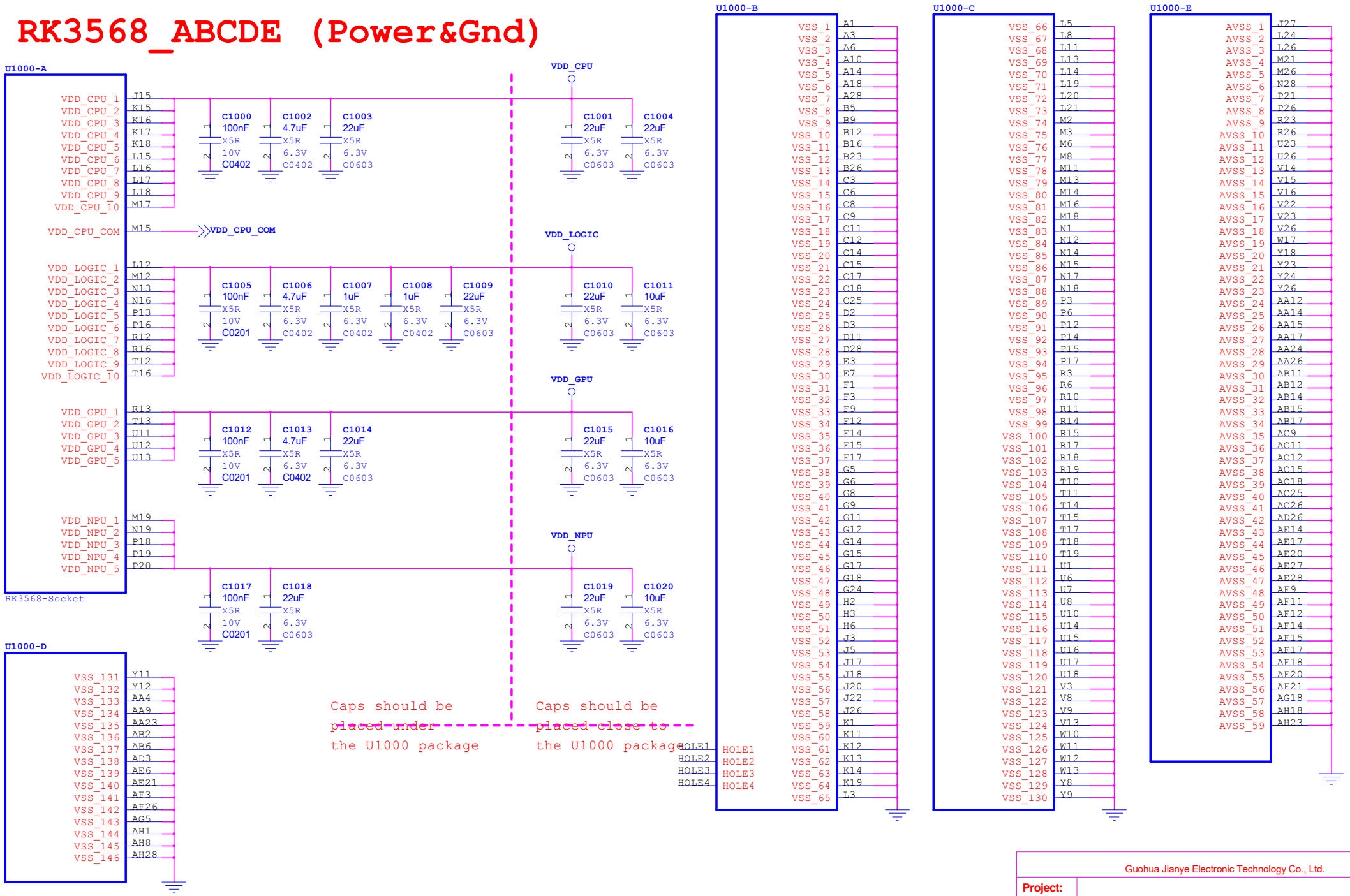
# RK3568_ABCDE (Power&Gnd)

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# RK3568_F (DDR PHY)








**Note:**

Caps should be placed under the U1000 package

| | | | |
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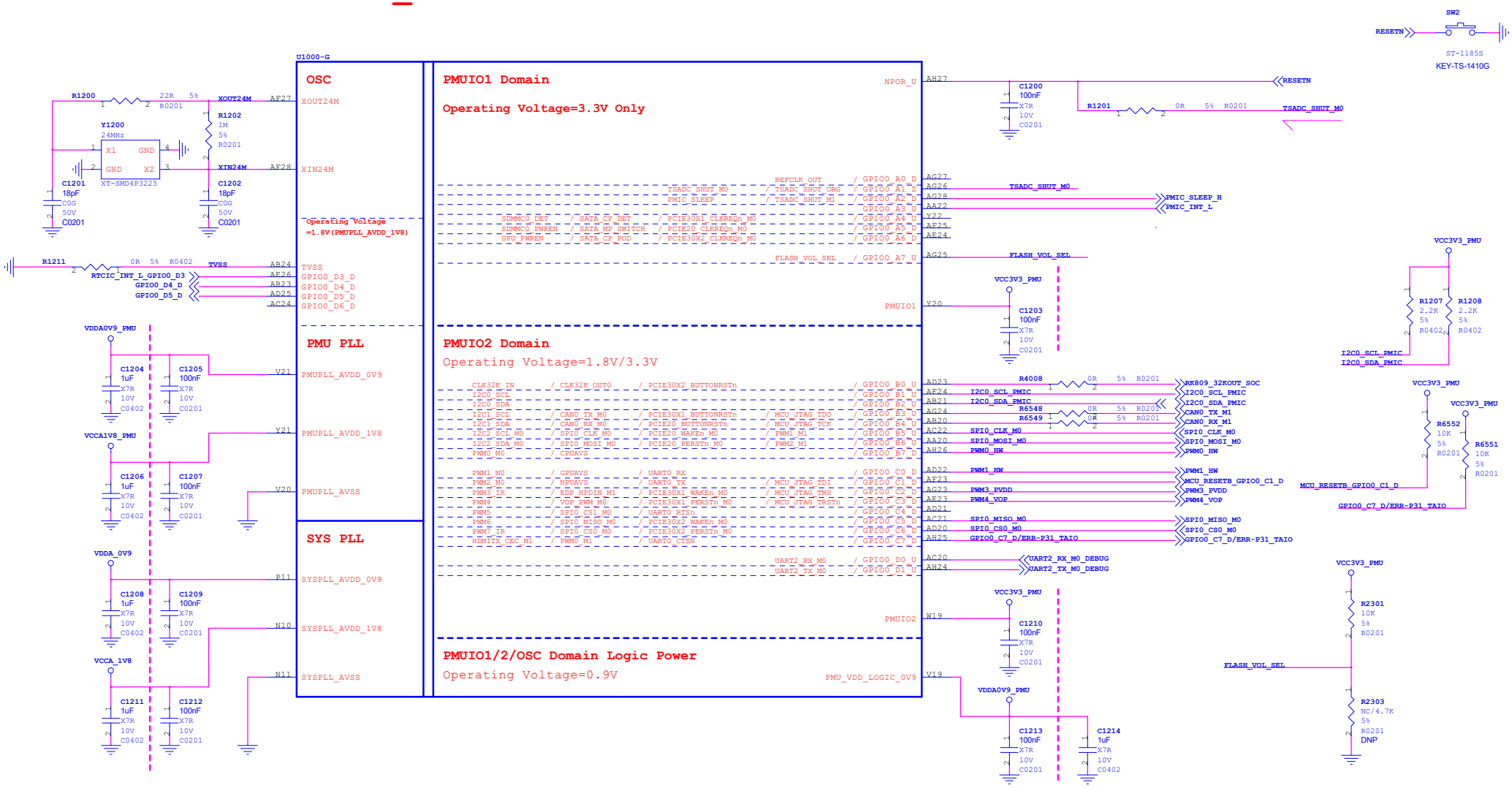
# RK3568_G(OSC/PLL/PMUIO1/2)




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

| | | | | |
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# RK3568_I(VCCIO2 Domain)

U1000-I

**VCCIO2 Domain**

Operating Voltage=1.8V/3.3V

EMMC_D0 / FLASH_D0 / GPIO1_B4_U
EMMC_D1 / FLASH_D1 / GPIO1_B5_U
EMMC_D2 / FLASH_D2 / GPIO1_B6_U
EMMC_D3 / FLASH_D3 / GPIO1_B7_U
EMMC_D4 / FLASH_D4 / GPIO1_C0_U
EMMC_D5 / FLASH_D5 / GPIO1_C1_U
EMMC_D6 / FLASH_D6 / GPIO1_C2_U
EMMC_D7 / FLASH_D7 / GPIO1_C3_U

EMMC_CMD / FLASH_WRn / GPIO1_C4_U

EMMC_CLKOUT / FLASH_DQS / GPIO1_C5_D

EMMC_DATA_STROBE / FSPI_CS1n / FLASH_CLE / GPIO1_C6_D

EMMC_RSTn / FSPI_D2 / FLASH_WPn / GPIO1_C7_D
FSPI_CLK / FLASH_ALE / GPIO1_D0_D
FSPI_D0 / FLASH_RDY / GPIO1_D1_U
FSPI_D1 / FLASH_RDn / GPIO1_D2_U
~~Default is determined by FLASH~~ FSPI_CS0n / FLASH_CS0n / GPIO1_D3_U
FLASH_VOL_SEL/GPIO1_A0_D: FSPI_D3 / FLASH_CS1n / GPIO1_D4_U
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2

A24 EMMC_D0/FLASH_D0
C21 EMMC_D1/FLASH_D1
B24 EMMC_D2/FLASH_D2
D21 EMMC_D3/FLASH_D3
A25 EMMC_D4/FLASH_D4
E21 EMMC_D5/FLASH_D5
E22 EMMC_D6/FLASH_D6
B25 EMMC_D7/FLASH_D7
B22 EMMC_CMD
A23 EMMC_CLK — R1310 22R R0201 — TP2204 TP_0.7 — EMMC_CLKOUT
A26 EMMC_DATA_STROBE
P20 FSPI_D2 — R1311 NC/22R R0201 — EMMC_RSTN
A22
C24
D23
C23
A27
H18

EMMC_D0/FLASH_D0 — TP2202 TP_0.7
TP2203 TP_0.7

VCCIO_FLASH
C1300 100nF X7R 10V C0201

# RK3568_J(VCCIO3 Domain)

U1000-J

**VCCIO3 Domain**

Operating Voltage=1.8V/3.3V

SDMMC0_D0 / UART2_TX_M1 / UART6_TX_M1 / PWM8_M1 / GPIO1_D5_U
SDMMC0_D1 / UART2_RX_M1 / UART6_RX_M1 / PWM9_M1 / GPIO1_D6_U
SDMMC0_D2 / ARMJTAG_TCK / UART5_CTSn_M0 / GPIO1_D7_U
SDMMC0_D3 / ARMJTAG_TMS / UART5_RTSn_M0 / GPIO2_A0_U

SDMMC0_CMD / PWM10_M1 / UART5_RX_M0 / CAN0_TX_M1 / GPIO2_A1_U

SDMMC0_CLK / TEST_CLKOUT / UART5_TX_M0 / CAN0_RX_M1 / GPIO2_A2_D

VCCIO3

J25
J24
H26
J23
H27
H28 — R6427 22R R0201 — SDMMC0_CLK/MCU_EXCLK
L22

VCCIO_SD
C1301 100nF X7R 10V C0201

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

VCC_3V3 — R2300 NC/0R 5% R0402
VCC_1V8 — R2302 0R 5% R0402

U2300 SGM2033/PT5108E23E-18/NC SOT_23_5
IN, GND, EN, OUT, BP

VCC_3V3 — C2300 NC/1uF X5R 6.3V C0402 DNP
R2304 NC/10K R0402
C2302 DNP C0402
C2303 DNP C0402
VCCIO_FLASH — C2301 NC/4.7uF X5R 6.3V C0603

AEC-Q100

U4000-B
EMMC_B153_2L
BGA153_13RX11R5X0R9_2L

AEC-Q100

VCCIO_FLASH

R4003 10K 5% R0201 — EMMC_D0/FLASH_D0 A3, EMMC_D1/FLASH_D1 A4, EMMC_D2/FLASH_D2 A5, EMMC_D3/FLASH_D3 B2, EMMC_D4/FLASH_D4 B3, EMMC_D5/FLASH_D5 B4, EMMC_D6/FLASH_D6 B5, EMMC_D7/FLASH_D7 B6
R4004 10K 5% R0201 — EMMC_CMD M5
EMMC_CLKOUT M6
R4005 10K 5% R0201 — EMMC_RSTN K5
C4009 2.2uF X7R C0201 10V — VDDI C2
EMMC_DATA_STROBE H5
R4006 NC/47K R0201 5% DNP
VSF1 E9, VSF2 E10, VSF3 F10, VSF4 K10

U4000-A
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
CMD
CLK
RST_N
VDDI
DATA_STROBE
VSF1 VSF2 VSF3 VSF4
VCCQ1 VCCQ2 VCCQ3 VCCQ4 VCCQ5 (C6, M4, N4, P3, P5)
VCC1 VCC2 VCC3 VCC4 (E6, F5, J10, K9)
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 (T5, A6, C4, E7, G5, H10)
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 (K8, N2, N5, P4, P6)

C4001 C4002 C4003 C4004 100nF X7R 10V C0402
C4005 4.7uF X7R 10V C0603
VCC_3V3
C4006 C4007 100nF X7R 10V C0402
C4008 4.7uF X7R 10V C0603

KLMBG2JETD-B041
SDINBDA6-32G-XI1

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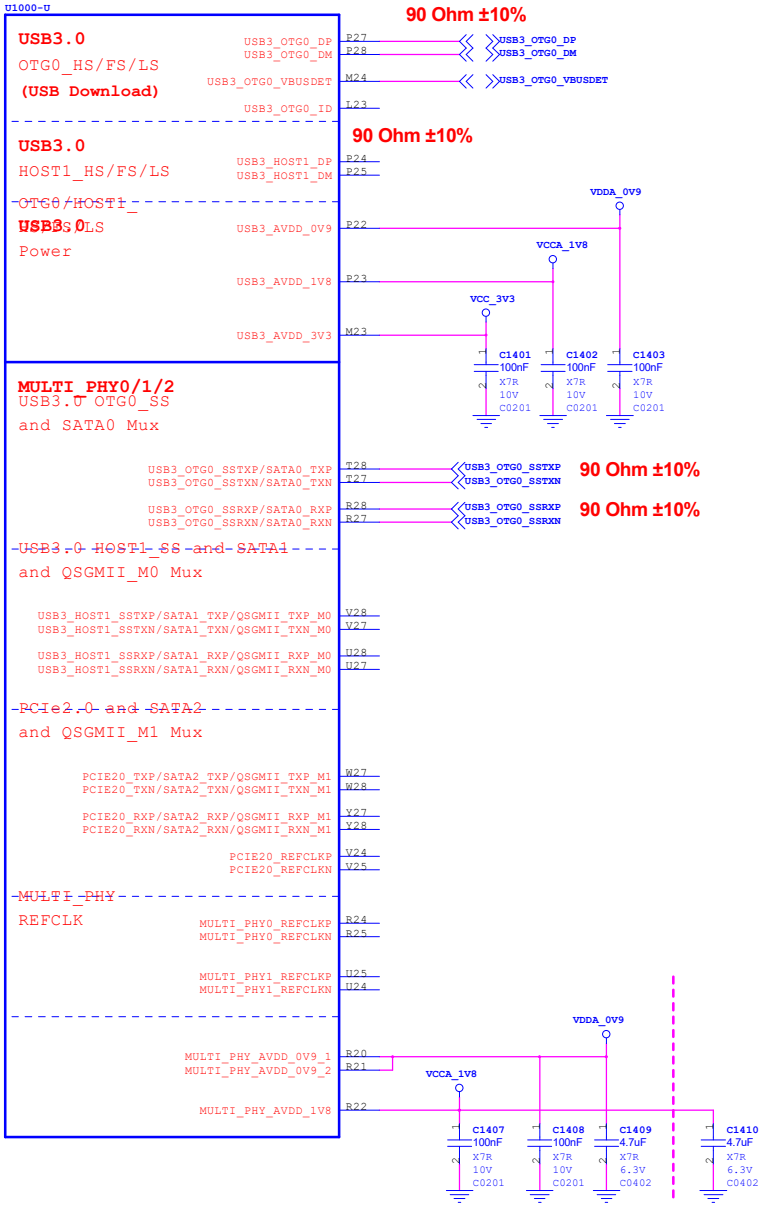
| Date: | Friday, June 2, 2023 | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: 11 of 99 |

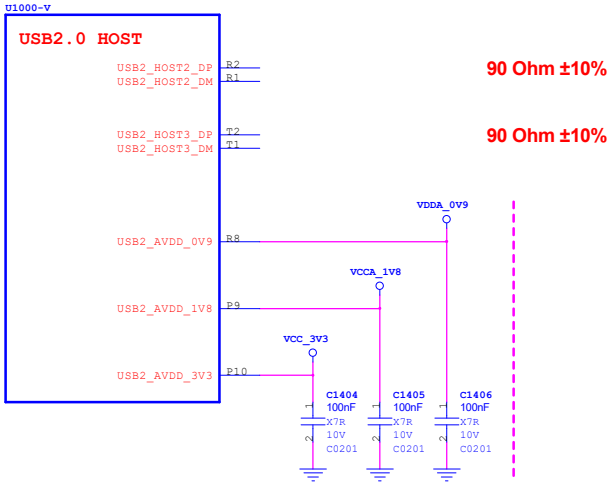
# RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



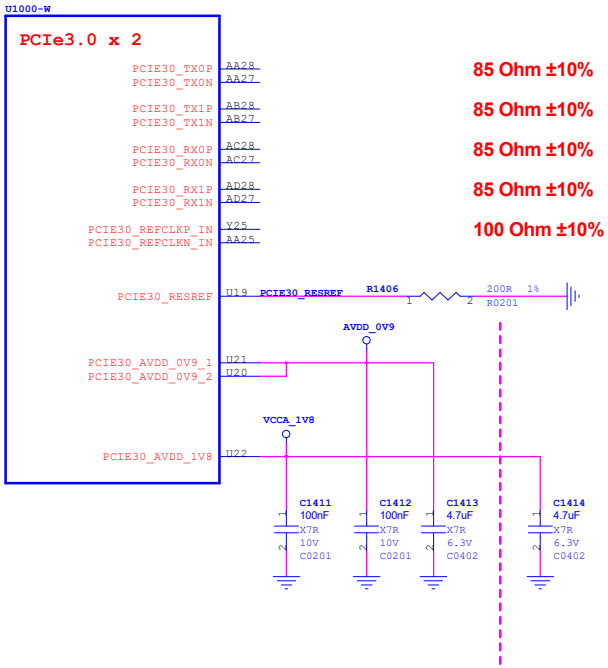

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

# RK3568_V(USB2.0 HOST)




# RK3568_W(PCIe3.0 x2)

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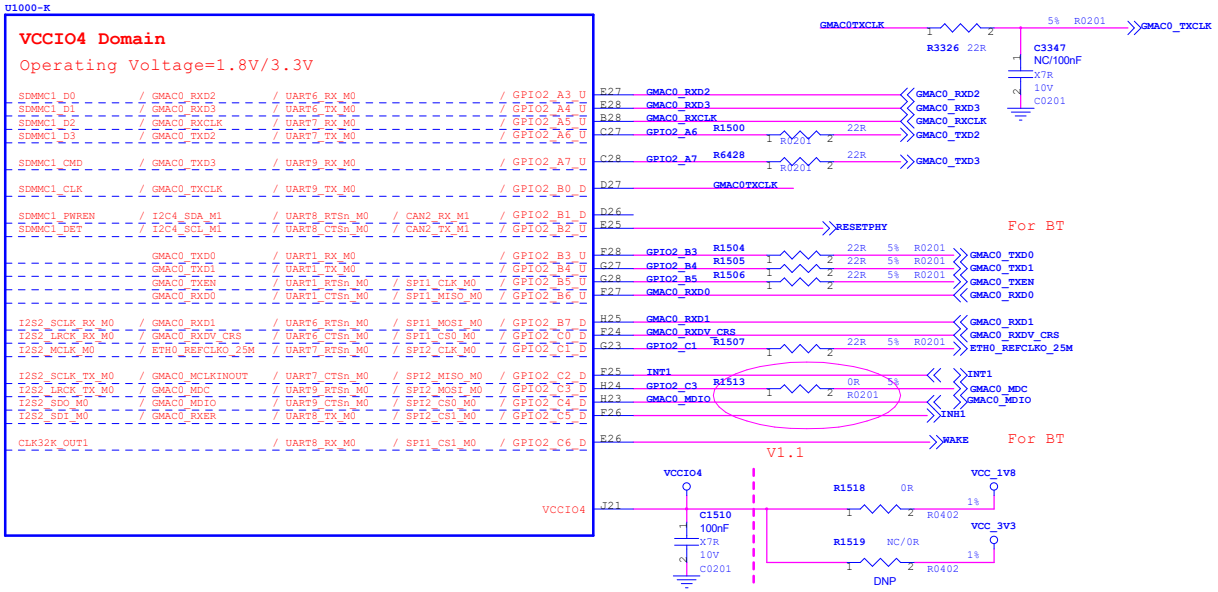
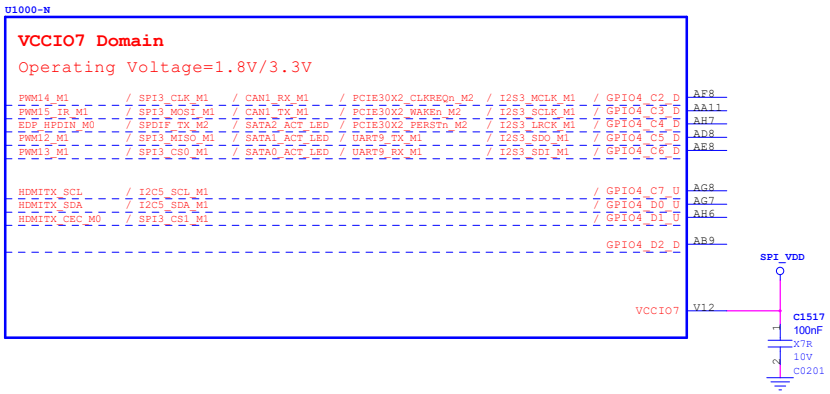
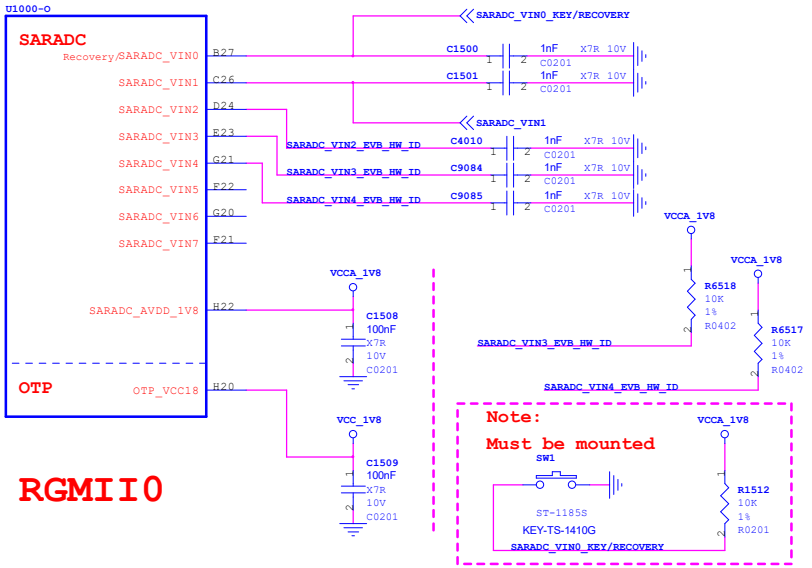
# RK3568_K(VCCIO4 Domain)




# RK3568_N(VCCIO7 Domain)

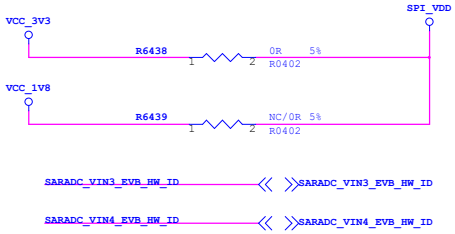



# RK3568_O(SARADC/OTP)

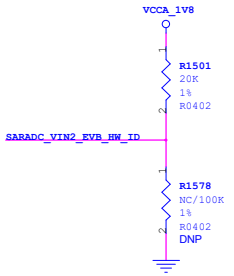



# RGMII0

# SPI VDD




| SARADC_VIN1_EVB_HW_ID | Rup | Rdown | ADC | |
|---|---|---|---|---|
| EVB1 | 10K | DNP | 1023 | 1.8V |
| EVB2 | 20K | 100K | 852 | 1.5V |
| EVB3 | 18K | 36K | 681 | 1.2V |
| EVB4 | 51K | 51K | 512 | 0.9V |
| EVB5 | 36K | 18K | 340 | 0.6V |
| EVB6 | 100K | 20K | 170 | 0.3V |
| EVB7 | DNP | 10K | 0 | 0V |
| EVB8 | | | | |




**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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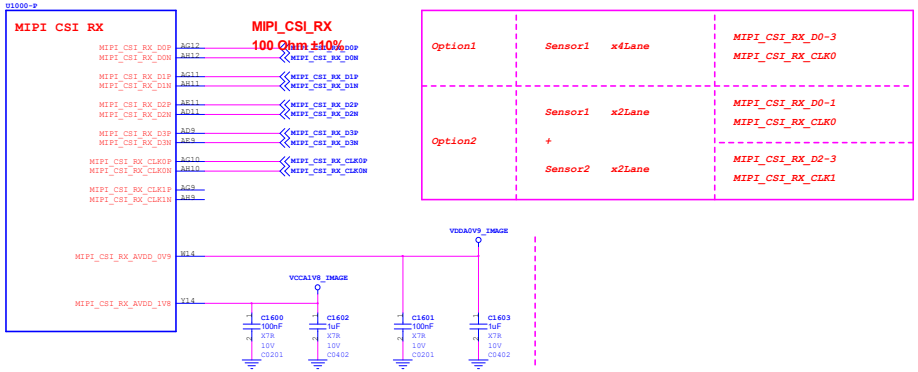
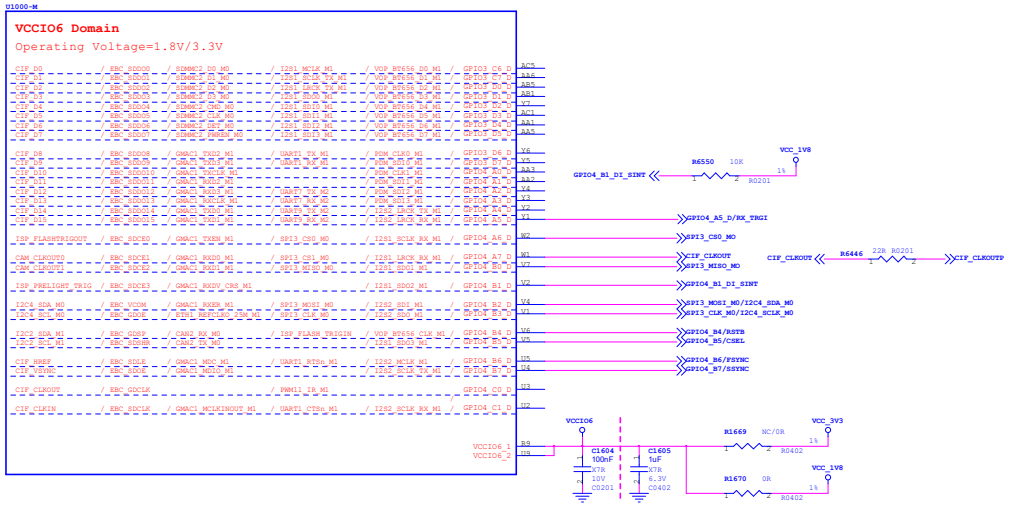
# RK3568_P(MIPI_CSI_RX)




| | | |
|---|---|---|
| Option1 | Sensor1 x4Lane | MIPI_CSI_RX_D0-3<br>MIPI_CSI_RX_CLK0 |
| Option2 | Sensor1 x2Lane<br>+<br>Sensor2 x2Lane | MIPI_CSI_RX_D0-1<br>MIPI_CSI_RX_CLK0<br>MIPI_CSI_RX_D2-3<br>MIPI_CSI_RX_CLK1 |

# RK3568_M(VCCIO6 Domain)




| Mode | 16bit | 12bit | 10bit | 8bit |
|---|---|---|---|---|
| CIF_D0 | D0 | -- | -- | -- |
| CIF_D1 | D1 | -- | -- | -- |
| CIF_D2 | D2 | -- | -- | -- |
| CIF_D3 | D3 | -- | -- | -- |
| CIF_D4 | D4 | D0 | -- | -- |
| CIF_D5 | D5 | D1 | -- | -- |
| CIF_D6 | D6 | D2 | D0 | -- |
| CIF_D7 | D7 | D3 | D1 | -- |
| CIF_D8 | D8 | D4 | D2 | D0 |
| CIF_D9 | D9 | D5 | D3 | D1 |
| CIF_D10 | D10 | D6 | D4 | D2 |
| CIF_D11 | D11 | D7 | D5 | D3 |
| CIF_D12 | D12 | D8 | D6 | D4 |
| CIF_D13 | D13 | D9 | D7 | D5 |
| CIF_D14 | D14 | D10 | D8 | D6 |
| CIF_D15 | D15 | D11 | D9 | D7 |

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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| Project: | | | |
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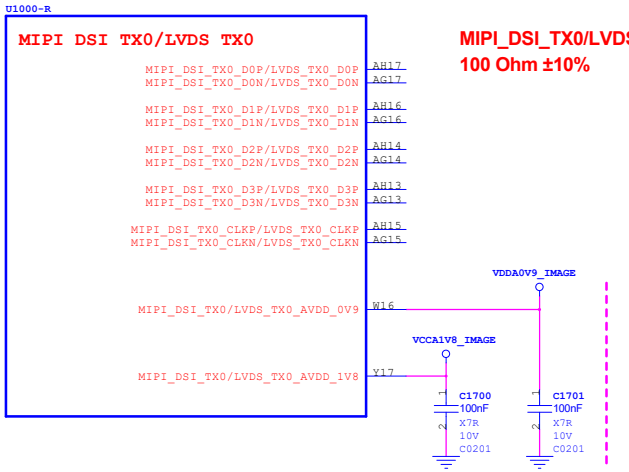
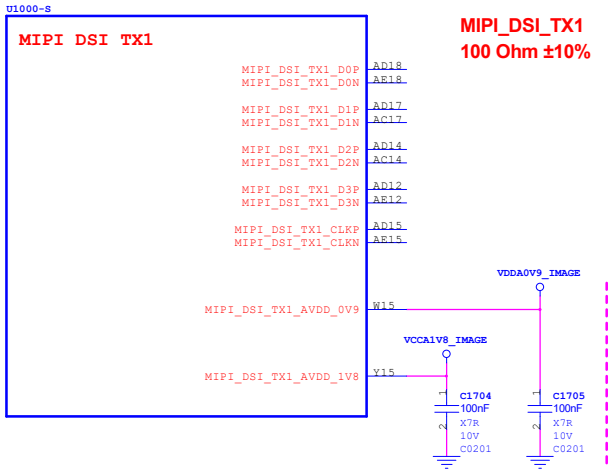
| Date: | Friday, June 2, 2023 | Rev: | |
| Designed by: <designer> | Reviewed by: <Checker> | Sheet: | 11 of 99 |

# RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



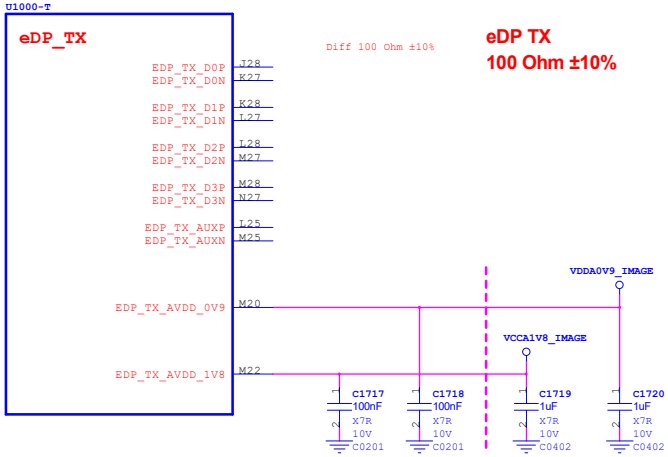

MIPI_DSI_TX0/LVDS_TX0
100 Ohm ±10%

# RK3568_S(MIPI_DSI_TX1)




MIPI_DSI_TX1
100 Ohm ±10%

# RK3568_T(eDP TX)

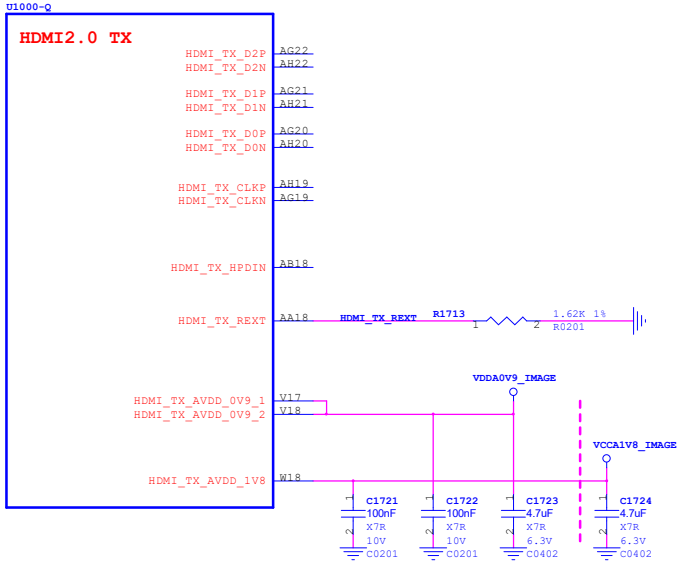



eDP TX
100 Ohm ±10%

**Note:**

Caps of between dashed green lines and U1000
~~should be placed under the U1000 package.~~
Other caps should be placed close to the U1000 package

# RK3568_Q(HDMI2.0 TX)




| Guohua Jianye Electronic Technology Co., Ltd. | | | | |
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| Project: | | | | |
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| Date: | Friday, June 2, 2023 | | Rev: | |
| Designed by: | <designer> | Reviewed by: <Checker> | Sheet: | 11 of 99 |

# RK3568_L(VCCIO5 Domain)

U1000-L

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

| | | | | | | |
|---|---|---|---|---|---|---|
| LCDC_D0 | VOP_BT656_D0_M0 | SPI0_MISO_M1 | PCIE20_CLKREQn_M1 | I2S1_MCLK_M2 | GPIO2_D0_D | AG6 |
| LCDC_D1 | VOP_BT656_D1_M0 | SPI0_MOSI_M1 | PCIE20_WAKEn_M1 | I2S1_SCLK_TX_M2 | GPIO2_D1_D | AD7 |
| LCDC_D2 | VOP_BT656_D2_M0 | SPI0_CS0_M1 | PCIE30X1_CLKREQn_M1 | I2S1_LRCK_TX_M2 | GPIO2_D2_D | AC8 |
| LCDC_D3 | VOP_BT656_D3_M0 | SPI0_CLK_M1 | PCIE30X1_WAKEn_M1 | I2S1_SDI0_M2 | GPIO2_D3_D | AC7 |
| LCDC_D4 | VOP_BT656_D4_M0 | SPI2_CS1_M1 | PCIE30X2_CLKREQn_M1 | I2S1_SDI1_M2 | GPIO2_D4_D | AF5 |
| LCDC_D5 | VOP_BT656_D5_M0 | SPI2_CS0_M1 | PCIE30X2_WAKEn_M1 | I2S1_SDI2_M2 | GPIO2_D5_D | AF6 |
| LCDC_D6 | VOP_BT656_D6_M0 | SPI2_MOSI_M1 | PCIE30X2_PERSTn_M1 | I2S1_SDI3_M2 | GPIO2_D6_D | AD6 |
| LCDC_D7 | VOP_BT656_D7_M0 | SPI2_MISO_M1 | UART8_TX_M1 | I2S1_SDO0_M2 | GPIO2_D7_D | AH5 |
| LCDC_CLK | VOP_BT656_CLK_M0 | SPI2_CLK_M1 | UART8_RX_M1 | I2S1_SDO1_M2 | GPIO3_A0_D | AH4 |
| LCDC_D8 | VOP_BT1120_D0 | SPI1_CS0_M1 | PCIE30X1_PERSTn_M1 | SDMMC2_D0_M1 | GPIO3_A1_D | AB8 |
| LCDC_D9 | VOP_BT1120_D1 | GMAC1_TXD2_M0 | I2S3_MCLK_M0 | SDMMC2_D1_M1 | GPIO3_A2_D | AE5 |
| LCDC_D10 | VOP_BT1120_D2 | GMAC1_TXD3_M0 | I2S3_SCLK_M0 | SDMMC2_D2_M1 | GPIO3_A3_D | AG4 |
| LCDC_D11 | VOP_BT1120_D3 | GMAC1_RXD2_M0 | I2S3_LRCK_M0 | SDMMC2_D3_M1 | GPIO3_A4_D | AF4 |
| LCDC_D12 | VOP_BT1120_D4 | GMAC1_RXD3_M0 | I2S3_SDO_M0 | SDMMC2_CMD_M1 | GPIO3_A5_D | AH3 |
| LCDC_D13 | VOP_BT1120_CLK | GMAC1_TXCLK_M0 | I2S3_SDI_M0 | SDMMC2_CLK_M1 | GPIO3_A6_D | AG3 |
| LCDC_D14 | VOP_BT1120_D5 | GMAC1_RXCLK_M0 | | SDMMC2_DET_M1 | GPIO3_A7_D | AH2 |
| LCDC_D15 | VOP_BT1120_D6 | ETH1_REFCLKO_25M_M0 | | SDMMC2_PWREN_M1 | GPIO3_B0_D | AG2 |
| LCDC_D16 | VOP_BT1120_D7 | GMAC1_RXD0_M0 | UART4_RX_M1 | PWM8_M0 | GPIO3_B1_D | AG1 |
| LCDC_D17 | VOP_BT1120_D8 | GMAC1_RXD1_M0 | UART4_TX_M1 | PWM9_M0 | GPIO3_B2_D | AF2 |
| LCDC_D18 | VOP_BT1120_D9 | GMAC1_RXDV_CRS_M0 | I2C5_SCL_M0 | PDM_SDI0_M2 | GPIO3_B3_D | AF1 |
| LCDC_D19 | VOP_BT1120_D10 | GMAC1_RXER_M0 | I2C5_SDA_M0 | PDM_SDI1_M2 | GPIO3_B4_D | AE1 |
| LCDC_D20 | VOP_BT1120_D11 | GMAC1_TXD0_M0 | I2C3_SCL_M1 | PWM10_M0 | GPIO3_B5_D | AE2 |
| LCDC_D21 | VOP_BT1120_D12 | GMAC1_TXD1_M0 | I2C3_SDA_M1 | PWM11_IR_M0 | GPIO3_B6_D | AE3 |
| LCDC_D22 | PWM12_M0 | GMAC1_TXEN_M0 | UART3_TX_M1 | PDM_SDI2_M2 | GPIO3_B7_D | AD4 |
| LCDC_D23 | PWM13_M0 | GMAC1_MCLKINOUT_M0 | UART3_RX_M1 | PDM_SDI3_M2 | GPIO3_C0_D | AD2 |
| LCDC_HSYNC | VOP_BT1120_D13 | SPI1_MOSI_M1 | PCIE20_PERSTn_M1 | I2S1_SDO2_M2 | GPIO3_C1_D | AD1 |
| LCDC_VSYNC | VOP_BT1120_D14 | SPI1_MISO_M1 | UART5_TX_M1 | I2S1_SDO3_M2 | GPIO3_C2_D | AA7 |
| LCDC_DEN | VOP_BT1120_D15 | SPI1_CLK_M1 | UART5_RX_M1 | I2S1_SCLK_RX_M2 | GPIO3_C3_D | AC4 |
| PWM14_M0 | VOP_PWM_M1 | GMAC1_MDC_M0 | UART7_TX_M1 | PDM_CLK1_M2 | GPIO3_C4_D | AC3 |
| PWM15_IR_M0 | SPDIF_TX_M1 | GMAC1_MDIO_M0 | UART7_RX_M1 | I2S1_LRCK_RX_M2 | GPIO3_C5_D | AC2 |

AG6 GPIO_D0_D
AD7 GPIO_D1_D
AC8 GPIO_D2_D
AF5 SPI2_CS1_M1
AF6 SPI2_CS0_M1
AD6 SPI2_MOSI_M1
AH5 SPI2_MISO_M1
AH4 SPI2_CLK_M1
AB8 GPIO3_A1_D
AE5 GPIO3_A2_D
AG4 TYPEC0_INT
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AD1 UART5_TX_M1
AA7 UART5_RX_M1
AC3 UART7_TX_M1
AC2 UART7_RX_M1

VCCIO5_1 V10
VCCIO5_2 V11

VCC_3V3
C1800
100nF
X5R
10V
C0201

VCC_3V3
R1802 2.2K 5% R0201
R1803 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

for PCIE WIFI

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

**Note:**

*If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!*

*If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormally.*

*The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO5 will be damaged!*

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| Project: | | | | |
| File: | | | | |
| Date: | Friday, June 2, 2023 | | Rev: | |
| Designed by: | <designer> | Reviewed by: <Checker> | Sheet: | 11 of 99 |

# RK3568_H(VCCIO1 Domain)

U1000-H

## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

| | | | | | |
|---|---|---|---|---|---|
| I2C3_SDA_M0 | / UART3_RX_M0 | / CAN1_RX_M0 | / AUDIOPWM_LOUT_P | / ACODEC_ADC_DATA | / GPIO1_A0_U |
| I2C3_SCL_M0 | / UART3_TX_M0 | / CAN1_TX_M0 | / AUDIOPWM_LOUT_N | / ACODEC_ADC_CLK | / GPIO1_A1_U |
| I2S1_MCLK_M0 | / UART3_RTSn_M0 | / SCR_CLK | / PCIE30X1_PERSTn_M2 | | / GPIO1_A2_D |
| I2S1_SCLK_TX_M0 | / UART3_CTSn_M0 | / SCR_IO | / PCIE30X1_WAKEn_M2 | / ACODEC_DAC_CLK | / GPIO1_A3_D |
| I2S1_SCLK_RX_M0 | / UART4_RX_M0 | / PDM_CLK1_M0 | | / SPDIF_TX_M0 | / GPIO1_A4_D |
| I2S1_LRCK_TX_M0 | / UART4_RTSn_M0 | / SCR_RST | / PCIE30X1_CLKREQn_M2 | / ACODEC_DAC_SYNC | / GPIO1_A5_D |
| I2S1_LRCK_RX_M0 | / UART4_TX_M0 | / PDM_CLK0_M0 | | / AUDIOPWM_ROUT_P | / GPIO1_A6_D |
| I2S1_SDO0_M0 | / UART4_CTSn_M0 | / SCR_DET | | / AUDIOPWM_ROUT_N / ACODEC_DAC_DATAL | / GPIO1_A7_D |
| I2S1_SDO1_M0 | / I2S1_SDI3_M0 | / PDM_SDI3_M0 | / PCIE20_CLKREQn_M2 | / ACODEC_DAC_DATAR | / GPIO1_B0_D |
| I2S1_SDO2_M0 | / I2S1_SDI2_M0 | / PDM_SDI2_M0 | / PCIE20_WAKEn_M2 | / ACODEC_ADC_SYNC | / GPIO1_B1_D |
| I2S1_SDO3_M0 | / I2S1_SDI1_M0 | / PDM_SDI1_M0 | / PCIE20_PERSTn_M2 | | / GPIO1_B2_D |
| | I2S1_SDI0_M0 | / PDM_SDI0_M0 | | | / GPIO1_B3_D |

VCCIO1

D18 — I2C3_SDA_M0
E18 — I2C3_SCL_M0

A19 — I2S1_MCLK_M0 — R1902 22R R0201 — I2S1_MCLK_M0_RK809

B19 — I2S1_SCLK_TX_M0 — R1903 22R R0201 — I2S1_SCLK_TX_M0_RK809

F18

A20 — I2S1_LRCK_TX_M0 — R1905 22R R0201 — I2S1_LRCK_TX_M0_RK809

C20 — I2S1_LRCK_RX_M0/PDM_CLK0_M0 — R1906 22R R0201 — PDM_CLK0_M0_RK809

B20 — I2S1_SDO0_M0_RK809 — I2S1_SDO0_M0_RK809

D20

E20

A21

B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17 — C1900 100nF X7R 10V C0201

VCCIO_ACODEC

R6554 2.2K 5% R0201 — I2C3_SDA_M0

R6553 2.2K 5% R0201 — I2C3_SCL_M0

Default:RK809+PDM MIC
S1900=ON
S1901=OFF

**Note:**

Caps of between dashed green lines and U1000 should be placed under the U1000 package

| | | | | | |
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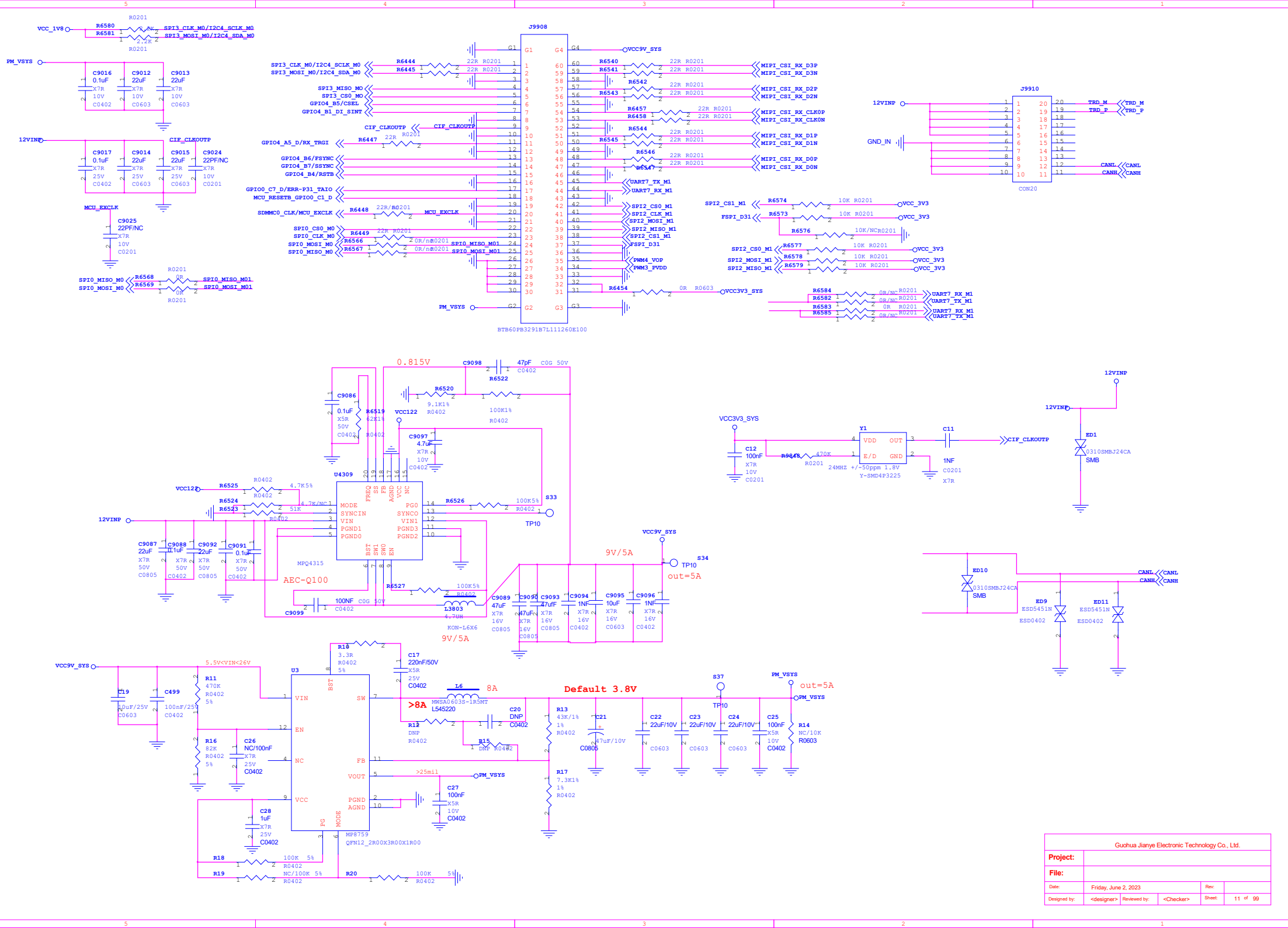
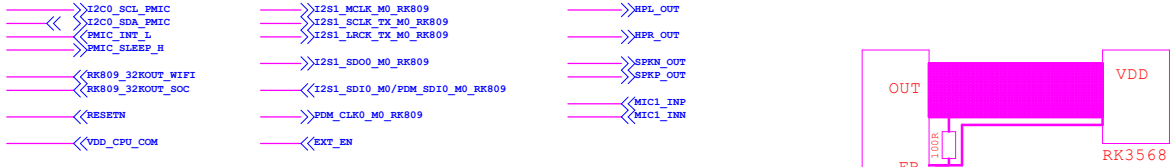
| Project: | | | | | |
| File: | | | | | |
| Date: | Friday, June 2, 2023 | | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: | 11 of 99 |

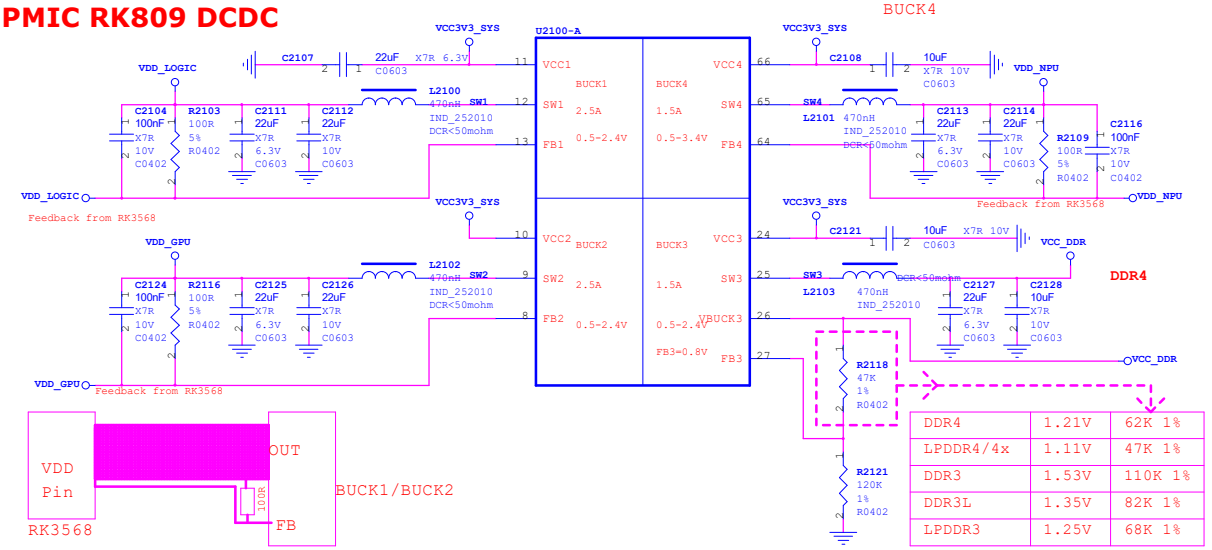

VCC_1V8
R6580
R6581
2.2K
SPI3_CLK_M0/I2C4_SCLK_M0
SPI3_MOSI_M0/I2C4_SDA_M0
PM_VSYS
C9016 0.1uF X7R 10V C0402
C9012 22uF X7R 10V C0603
C9013 22uF X7R 10V C0603
12VINP
CIF_CLKOUTP
C9017 0.1uF X7R 25V C0402
C9014 22uF X7R 25V C0603
C9015 22uF X7R 25V C0603
C9024 22PF/NC X7R 10V C0201
MCU_EXCLK
C9025 22PF/NC X7R 10V C0201
SPI0_MISO_M0
SPI0_MOSI_M0
R6568
R6569
SPI0_MISO_M01
SPI0_MOSI_M01
J9908
BTB60PB3291B7L111260E100
SPI3_CLK_M0/I2C4_SCLK_M0
SPI3_MOSI_M0/I2C4_SDA_M0
SPI3_MISO_M0
SPI3_CS0_M0
GPIO4_B5/CSEL
GPIO4_B1_DI_SINT
CIF_CLKOUTP
GPIO4_A5_D/RX_TRGI
GPIO4_B6/FSYNC
GPIO4_B7/SSYNC
GPIO4_B4/RSTB
GPIO0_C7_D/ERR-P31_TAIO
MCU_RESETB_GPIO0_C1_D
SDMMC0_CLK/MCU_EXCLK
SPI0_CS0_M0
SPI0_CLK_M0
SPI0_MOSI_M0
SPI0_MISO_M0
VCC9V_SYS
MIPI_CSI_RX_D3P
MIPI_CSI_RX_D3N
MIPI_CSI_RX_D2P
MIPI_CSI_RX_D2N
MIPI_CSI_RX_CLK0P
MIPI_CSI_RX_CLK0N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D0P
MIPI_CSI_RX_D0N
UART7_TX_M1
UART7_RX_M1
SPI2_CS0_M1
SPI2_CLK_M1
SPI2_MOSI_M1
SPI2_MISO_M1
SPI2_CS1_M1
FSPI_D31
PWM4_VOP
PWM3_PVDD
R6454
VCC3V3_SYS
J9910
CON20
12VINP
GND_IN
TRD_M
TRD_P
CANL
CANH
SPI2_CS1_M1
FSPI_D31
R6574
R6573
R6576
VCC_3V3
SPI2_CS0_M1
SPI2_MOSI_M1
SPI2_MISO_M1
R6577
R6578
R6579
R6584
R6582
R6583
R6585
0.815V
C9098 47pF C0G 50V
R6520 9.1K1%
R6522 100K1%
C9086 0.1uF X5R 50V C0402
R6519 62K1%
VCC122
C9097 4.7uF X7R 10V C0402
U4309
MODE
SYNCIN
VIN
PGND1
PGND0
FREQ
SS
FB
AGND
VCC
NC
PGO
SYNCO
VIN1
PGND3
PGND2
BST
SW1
SW0
EN
MPQ4315
AEC-Q100
R6525 4.7K5%
R6524 4.7K/NC
R6523 51K
R6526 100K5%
S33
TP10
C9087 22uF X7R 50V C0805
C9088 0.1uF X7R 50V C0402
C9092 22uF X7R 50V C0805
C9091 0.1uF X7R 50V C0402
R6527 100K5%
100NF C0G 50V C0402
C9099
L3803 4.7UH KON-L6X6
C9089 47uF X7R 16V C0805
C9090 47uF X7R 16V C0805
C9093 47uF X7R 16V C0805
C9094 1NF X7R 16V C0402
C9095 10uF X7R 16V C0603
C9096 1NF X7R 16V C0402
9V/5A
VCC9V_SYS
S34
TP10
out=5A
VCC3V3_SYS
C12 100nF X7R 10V C0201
Y1
VDD
OUT
E/D
GND
24MHZ +/-50ppm 1.8V
Y-SMD4P3225
R9648 470K
C11 1NF X7R C0201
CIF_CLKOUTP
12VINP
ED1 0310SMBJ24CA SMB
ED10 0310SMBJ24CA SMB
ED9 ESD5451N ESD0402
ED11 ESD5451N ESD0402
CANL
CANH
VCC9V_SYS
5.5V<VIN<26V
C19 10uF/25V C0603
C499 100nF/25V C0402
U3
VIN
SW
BST
EN
NC
FB
VOUT
VCC
PGND
AGND
PG
MODE
MP8759
QFN12_2R00X3R00X1R00
R11 470K R0402 5%
R16 82K R0402 5%
C26 NC/100nF X7R 25V C0402
C28 1uF X7R 25V C0402
R18 100K 5% R0402
R19 NC/100K 5% R0402
R20 100K 5% R0402
R10 3.3R R0402 5%
C17 220nF/50V X5R 25V C0402
L6 8A MWSA0603S-1R5MT L545220
>8A
R12 DNP R0402
R15 DNP R0402
C20 DNP C0402
>25mil
C27 100nF X5R 10V C0402
Default 3.8V
R13 43K/1% 1% R0402
R17 7.3K1% 1% R0402
C21 47uF/10V C0805
C22 22uF/10V C0603
C23 22uF/10V C0603
C24 22uF/10V C0603
C25 100nF X5R 10V C0402
R14 NC/10K R0603
S37
TP10
PM_VSYS
out=5A
Guohua Jianye Electronic Technology Co., Ltd.
Project:
File:
Date: Friday, June 2, 2023
Rev:
Designed by: <designer>
Reviewed by: <Checker>
Sheet: 11 of 99





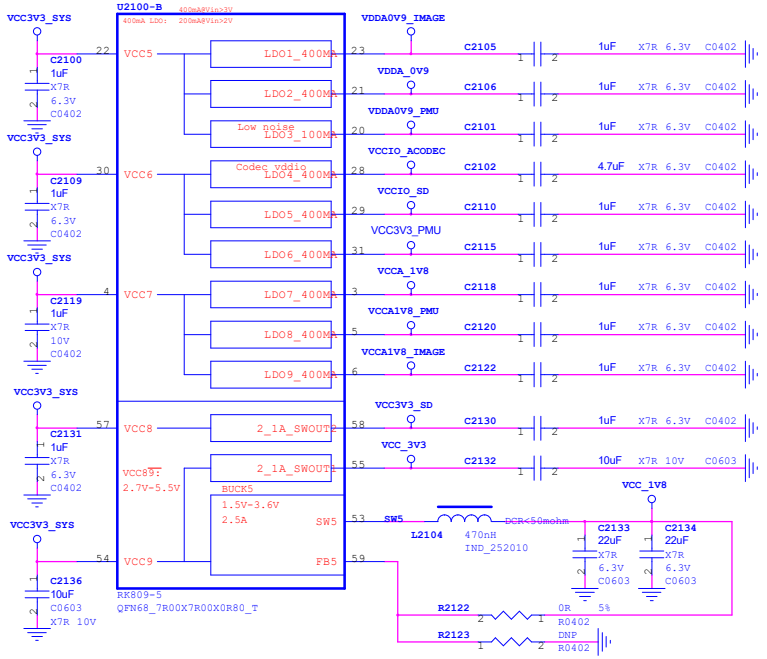


# PMIC RK809 DCDC

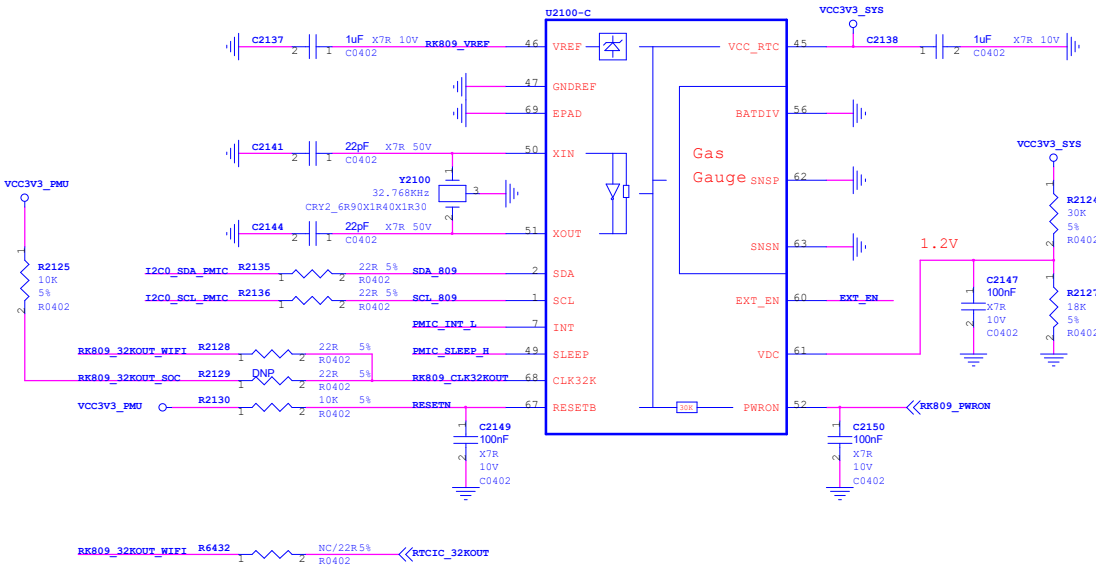



| | | |
|---|---|---|
| DDR4 | 1.21V | 62K 1% |
| LPDDR4/4x | 1.11V | 47K 1% |
| DDR3 | 1.53V | 110K 1% |
| DDR3L | 1.35V | 82K 1% |
| LPDDR3 | 1.25V | 68K 1% |

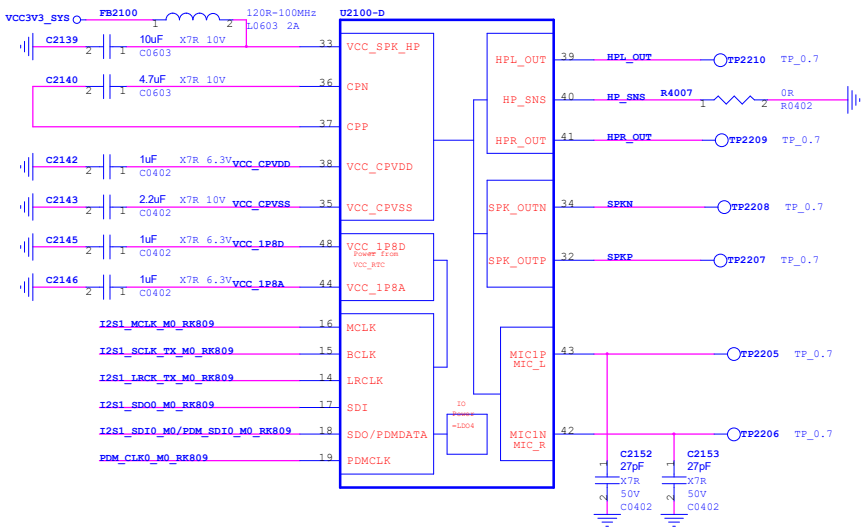
# PMIC RK809 LDO




# PMIC RK809 Managerment




# PMIC RK809 CODEC

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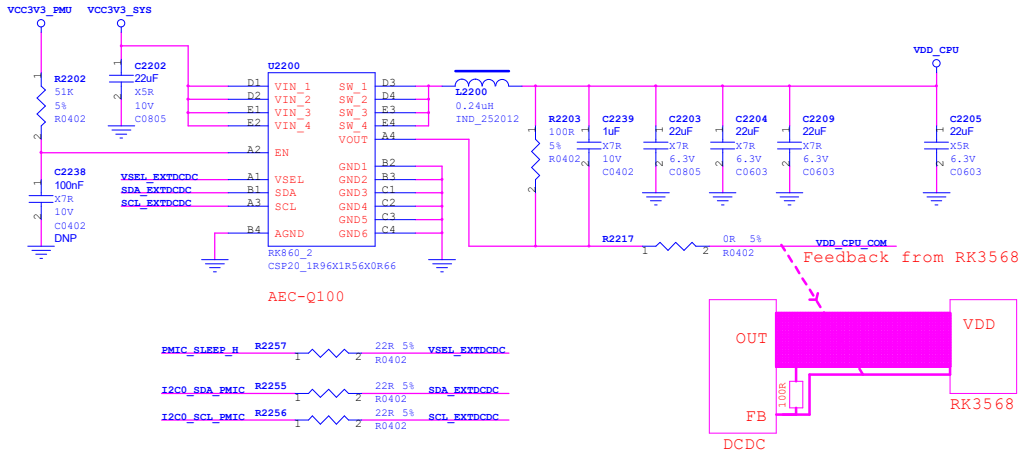
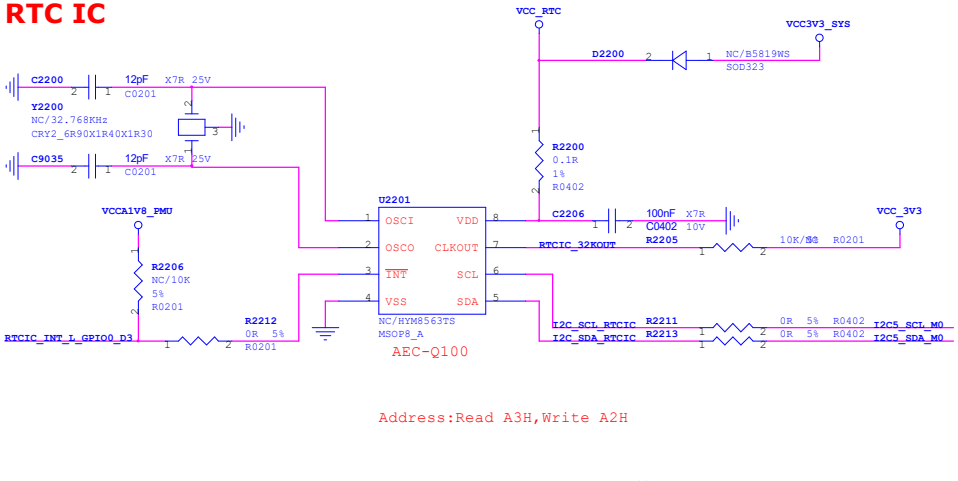
| Guohua Jianye Electronic Technology Co., Ltd. | | | | |
| Project: | | | | |
| File: | | | | |
| Date: | Friday, June 2, 2023 | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: 11 of 99 |

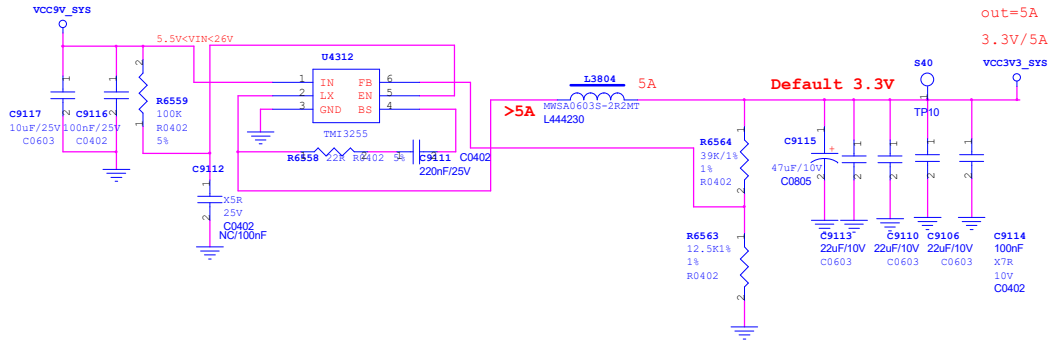
PMIC_SLEEP_H
VDD_CPU_COM
I2C0_SCL_PMIC
I2C0_SDA_PMIC
RTCIC_INT_L_GPIO0_D3
I2C5_SCL_M0
I2C5_SDA_M0

# VDD_CPU

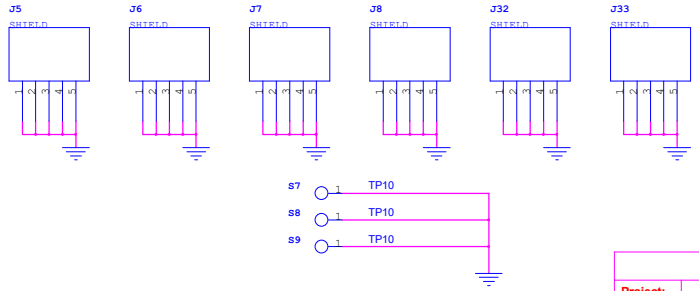



# RTC IC




# Back-up Power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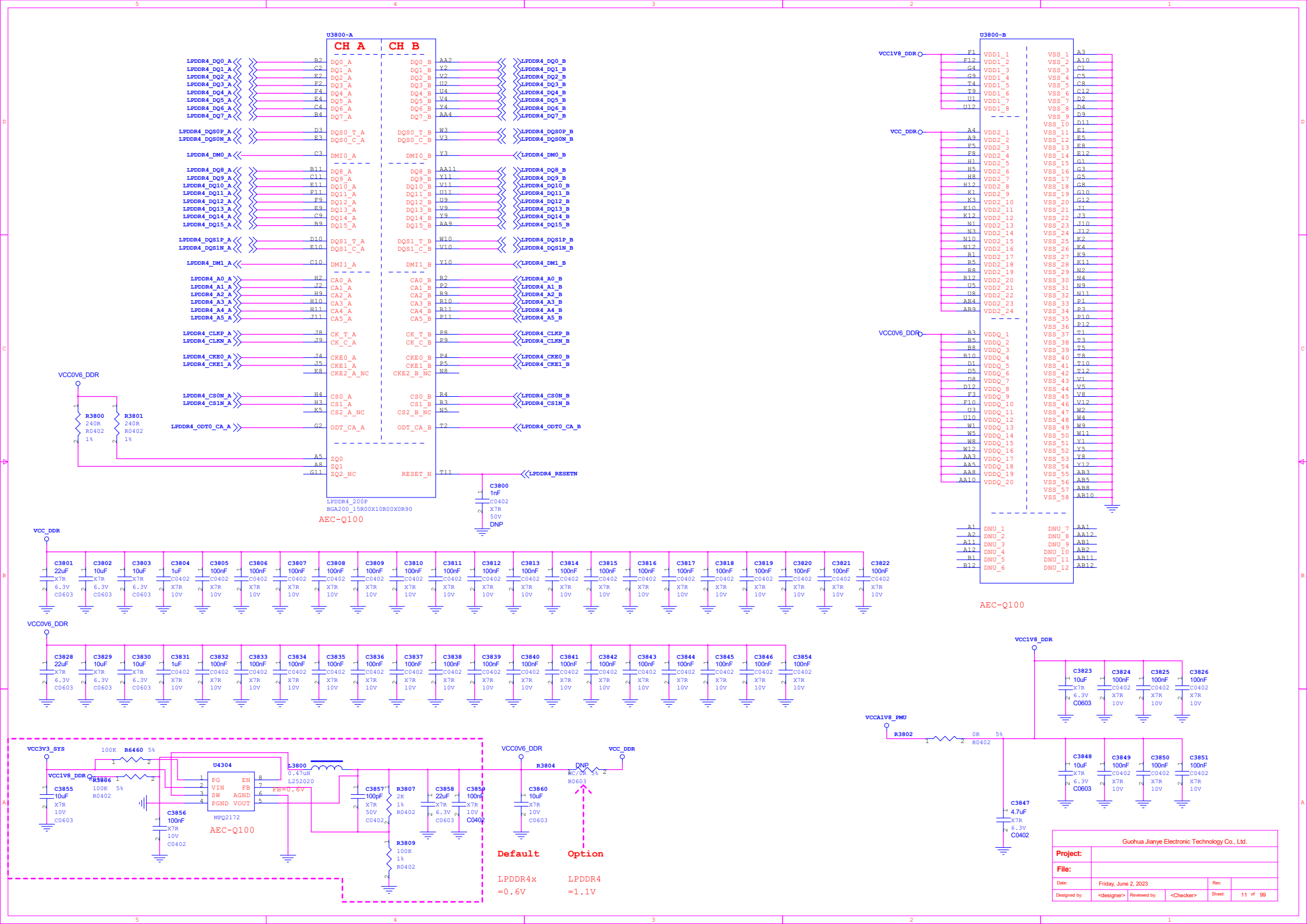
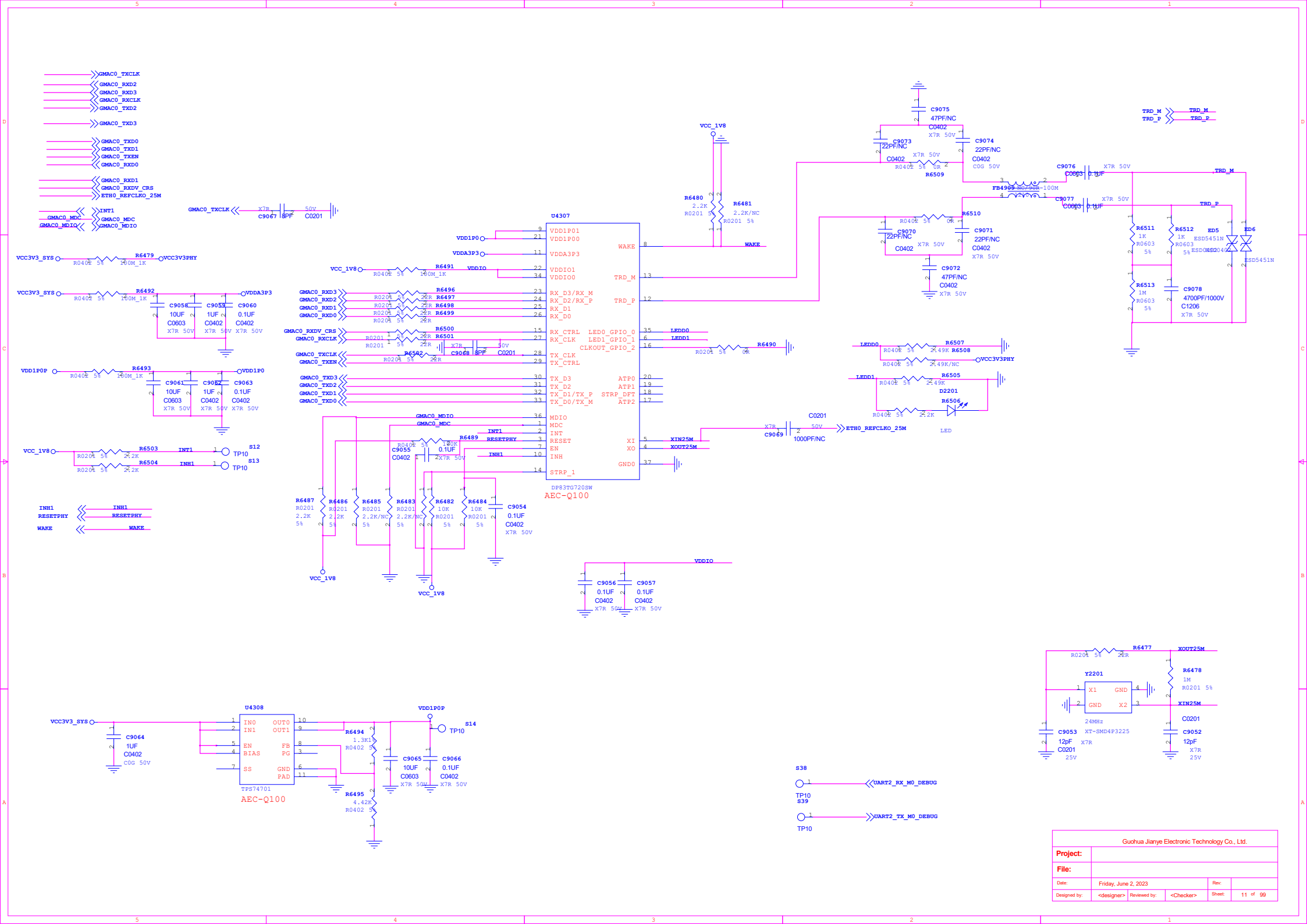
| Project: | | | | | |
| File: | | | | | |
| Date: | Friday, June 2, 2023 | | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: | 11 of 99 |


U3800-A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0N_A
LPDDR4_CS1N_A
LPDDR4_ODT0_CA_A
LPDDR4_RESETN
LPDDR4_200P
BGA200_15R00X10R00X0R90
AEC-Q100
VCC0V6_DDR
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0402 X7R 50V DNP
U3800-B
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
DNU_1
DNU_2
DNU_3
DNU_4
DNU_5
DNU_6
DNU_7
DNU_8
DNU_9
DNU_10
DNU_11
DNU_12
AEC-Q100
C3801 22uF X7R 6.3V C0603
C3802 10uF X7R 6.3V C0603
C3803 10uF X7R 6.3V C0603
C3804 1uF C0402 X7R 10V
C3805 100nF C0402 X7R 10V
C3806 100nF C0402 X7R 10V
C3807 100nF C0402 X7R 10V
C3808 100nF C0402 X7R 10V
C3809 100nF C0402 X7R 10V
C3810 100nF C0402 X7R 10V
C3811 100nF C0402 X7R 10V
C3812 100nF C0402 X7R 10V
C3813 100nF C0402 X7R 10V
C3814 100nF C0402 X7R 10V
C3815 100nF C0402 X7R 10V
C3816 100nF C0402 X7R 10V
C3817 100nF C0402 X7R 10V
C3818 100nF C0402 X7R 10V
C3819 100nF C0402 X7R 10V
C3820 100nF C0402 X7R 10V
C3821 100nF C0402 X7R 10V
C3822 100nF C0402 X7R 10V
C3828 22uF X7R 6.3V C0603
C3829 10uF X7R 6.3V C0603
C3830 10uF X7R 6.3V C0603
C3831 1uF C0402 X7R 10V
C3832 100nF C0402 X7R 10V
C3833 100nF C0402 X7R 10V
C3834 100nF C0402 X7R 10V
C3835 100nF C0402 X7R 10V
C3836 100nF C0402 X7R 10V
C3837 100nF C0402 X7R 10V
C3838 100nF C0402 X7R 10V
C3839 100nF C0402 X7R 10V
C3840 100nF C0402 X7R 10V
C3841 100nF C0402 X7R 10V
C3842 100nF C0402 X7R 10V
C3843 100nF C0402 X7R 10V
C3844 100nF C0402 X7R 10V
C3845 100nF C0402 X7R 10V
C3846 100nF C0402 X7R 10V
C3854 100nF C0402 X7R 10V
VCC3V3_SYS
R6460 100K 5%
VCC1V8_DDR
R3806 100K 5% R0402
C3855 10uF X7R 10V C0603
U4304
PG EN
VIN FB
SW AGND
PGND VOUT
MPQ2172
AEC-Q100
C3856 100nF X7R 10V C0402
L3800 0.47uH LZ52020
FB=0.6V
C3857 100pF X7R 50V C0402
R3807 2K 1% R0402
C3858 22uF X7R 6.3V C0603
C3859 100nF X7R 10V C0402
R3809 100K 1% R0402
VCC0V6_DDR
R3804 DNP RC/DC 5% R0603
VCC_DDR
C3860 10uF X7R 10V C0603
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCC1V8_DDR
C3823 10uF X7R 6.3V C0603
C3824 100nF C0402 X7R 10V
C3825 100nF C0402 X7R 10V
C3826 100nF C0402 X7R 10V
VCCA1V8_PMU
R3802 0R 5% R0402
C3848 10uF X7R 6.3V C0603
C3849 100nF C0402 X7R 10V
C3850 100nF C0402 X7R 10V
C3851 100nF C0402 X7R 10V
C3847 4.7uF X7R 6.3V C0402
Guohua Jianye Electronic Technology Co., Ltd.
Project:
File:
Date: Friday, June 2, 2023
Rev:
Designed by: <designer>
Reviewed by: <Checker>
Sheet: 11 of 99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GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXCLK
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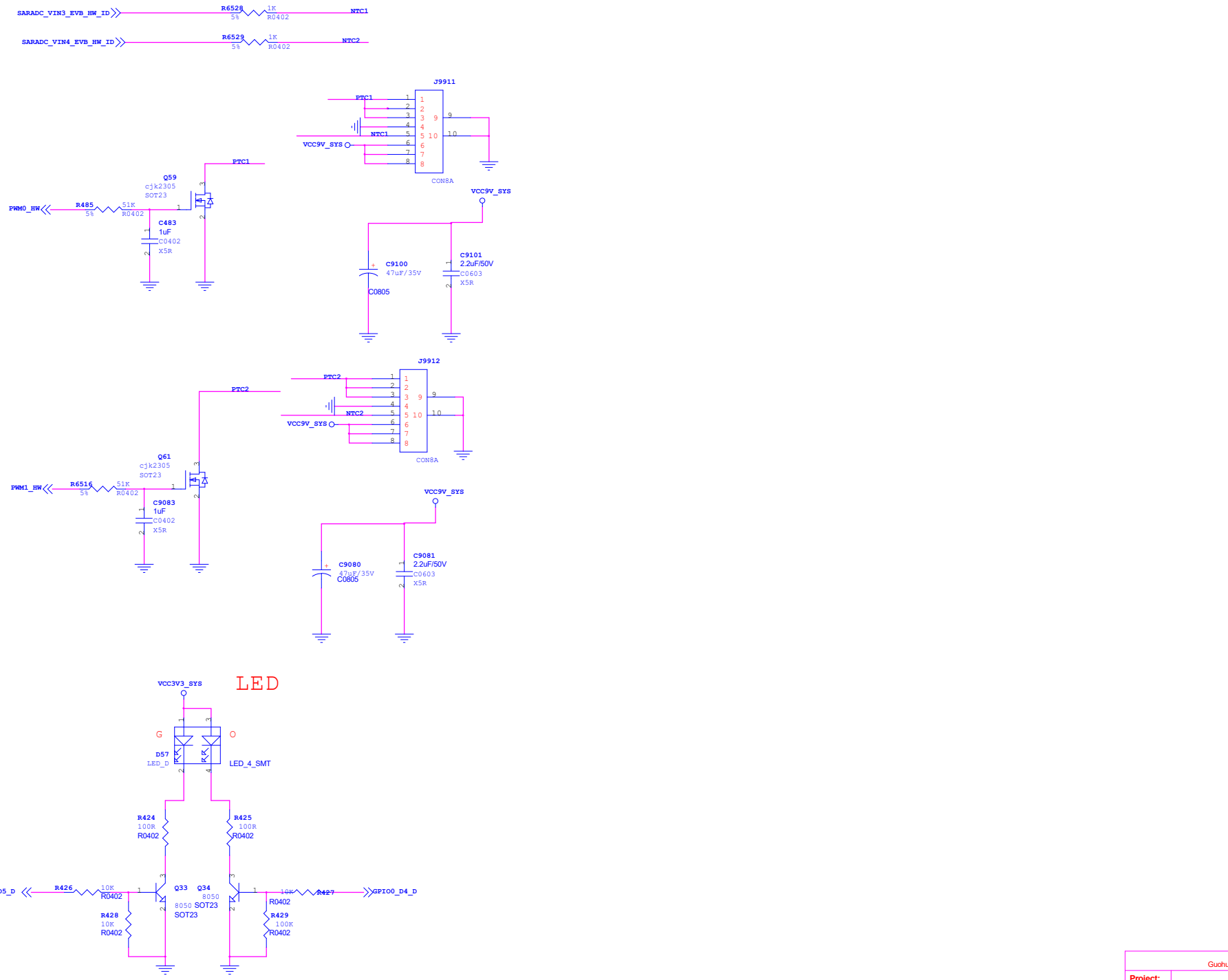
GMAC0_TXD3
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXEN
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXDV_CRS
ETH0_REFCLKO_25M
INT1
GMAC0_MDC
GMAC0_MDIO
U4307
DP83TG720SW
AEC-Q100
VCC_1V8
VDDIO
VDD1P0P
VCC3V3_SYS
VDDA3P3
WAKE
RESETPHY
INH1
XIN25M
XOUT25M
LEDD0
LEDD1
TRD_M
TRD_P
ETH0_REFCLKO_25M
LED
U4308
TPS74701
AEC-Q100
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG
Guohua Jianye Electronic Technology Co., Ltd.
Project:
File:
Date: Friday, June 2, 2023
Rev:
Designed by: <designer>
Reviewed by: <Checker>
Sheet: 11 of 99

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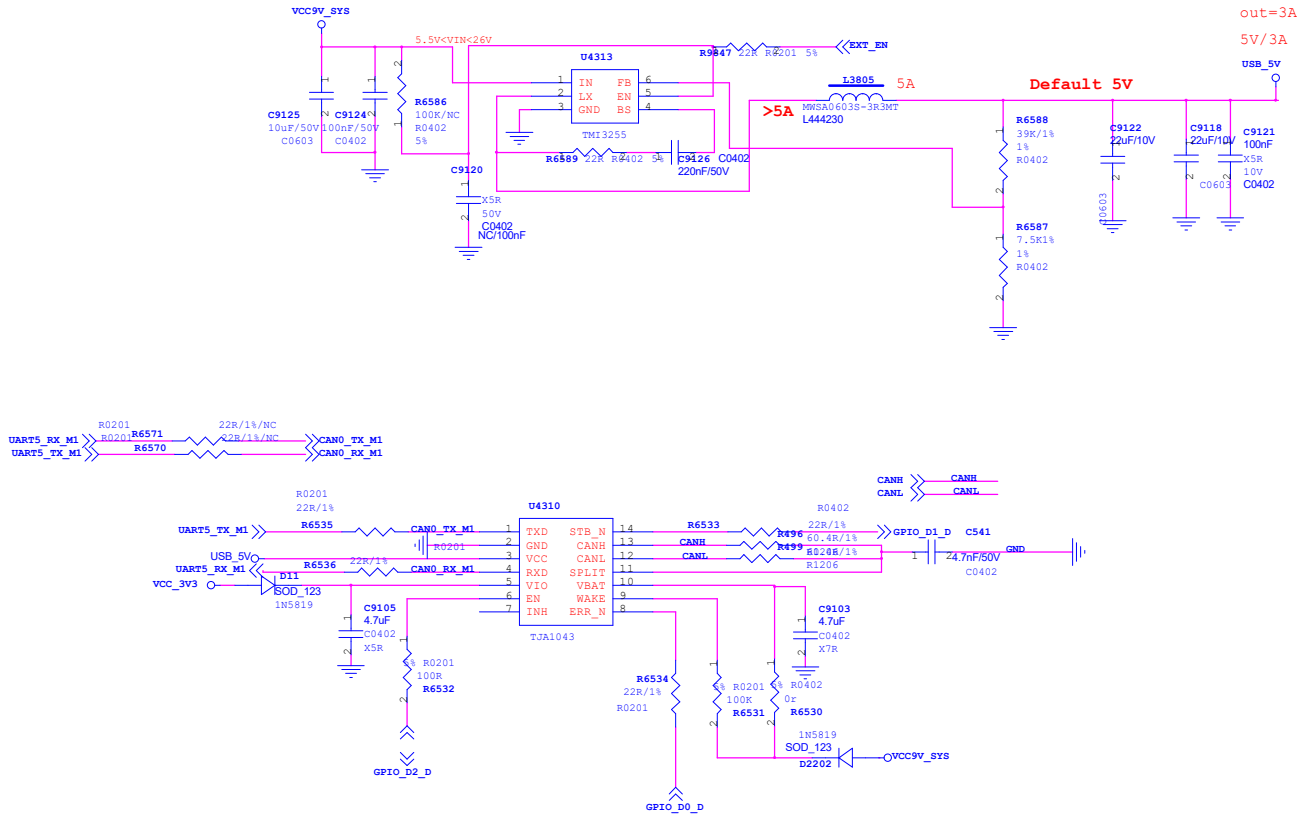
| Guohua Jianye Electronic Technology Co., Ltd. | | | | | |
| **Project:** | | | | | |
| **File:** | | | | | |
| Date: | Friday, June 2, 2023 | | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: | 11 of 99 |

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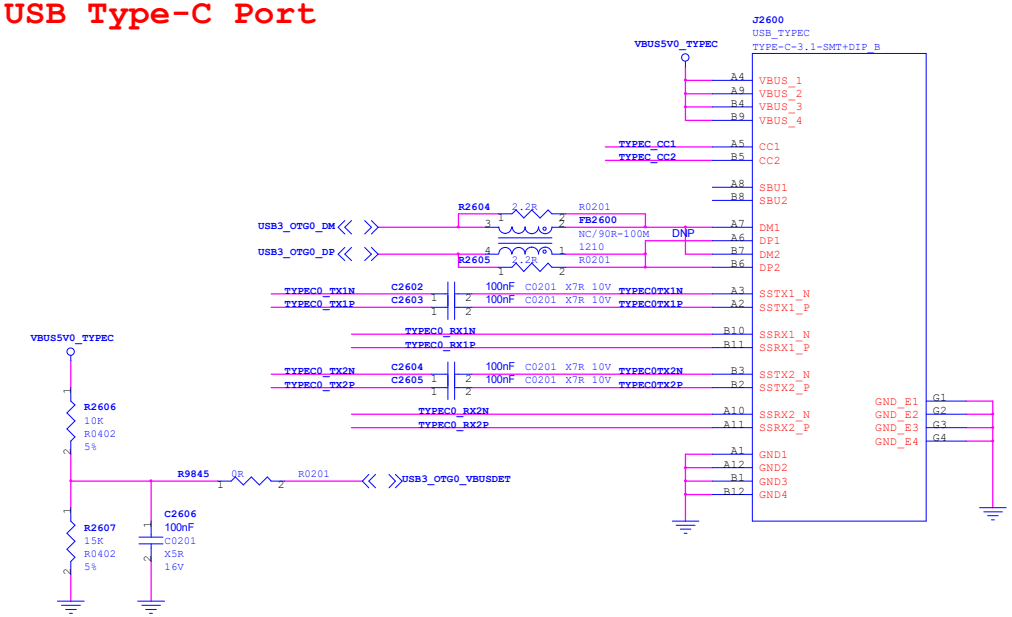
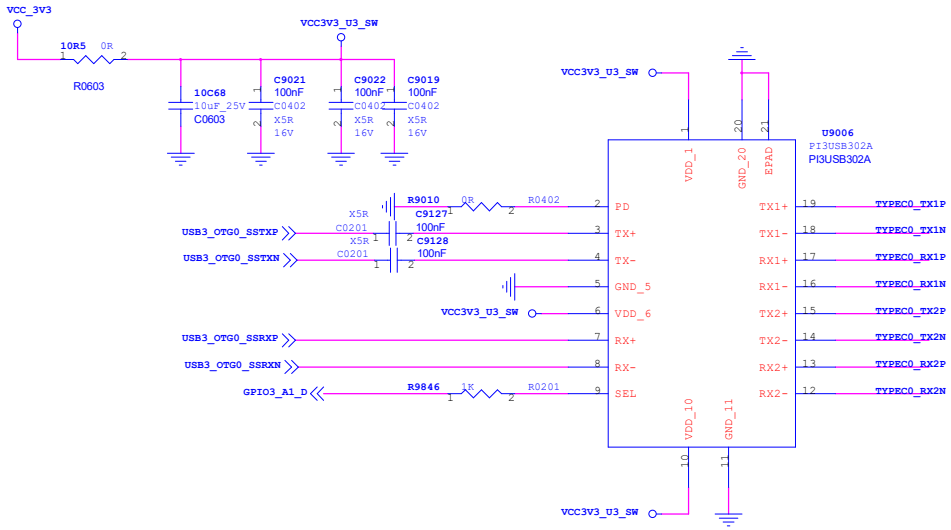
| Guohua Jianye Electronic Technology Co., Ltd. | | | | | |
| Project: | | | | | |
| File: | | | | | |
| Date: | Friday, June 2, 2023 | | | Rev: | |
| Designed by: | <designer> | Reviewed by: | <Checker> | Sheet: | 11 of 99 |

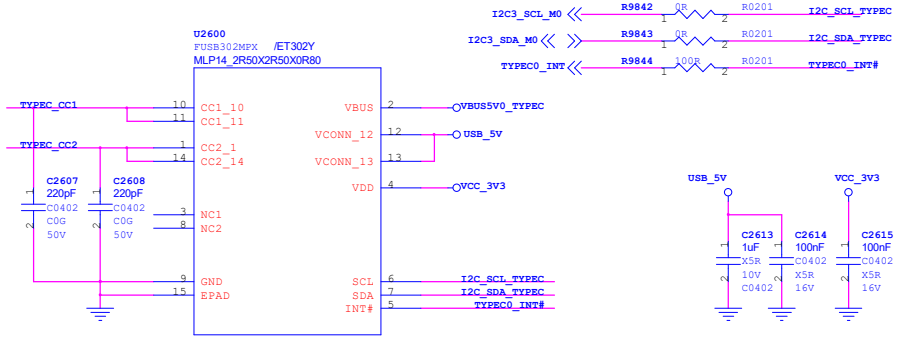
# USB Type-C Port



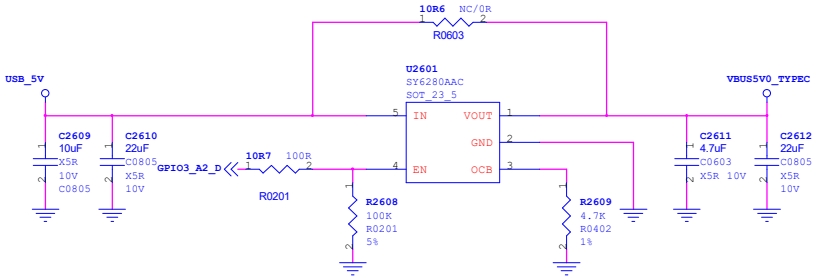

# Differential Channel Crossbar Switch




# USB Type-C CC CTRL PD

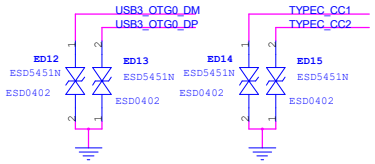



# USB Type-C Power




# ESD

Note:All the ESD components should be placed close to the port and Cj<=0.4pF


| | | | |
|---|---|---|---|
| Fuzhou Rockchip Electronics | | | |
| Project: | | | |
| File: | USB Type-C | | |
| Date: | Friday, June 2, 2023 | Rev: | V1.0 |
| Designed by: | Linus | Sheet: | 11 of 99 |