RM520N Series

Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-11-25	Wynna SHU/ Simon WANG	Creation of the document
1.0	2022-07-15	Juriyi XIE/ Wynna SHU/ Simon WANG	First official release
1.1	2023-03-16	Archibald JIANG/ Simon WANG/ Lewis PENG/ James YU	1. Added the module RM520N-EU. 2. Deleted the description of I/O characteristics about PU and PD (Table 6, Table 9, Table 12, Table 15, Table 20, Table 26 and Table 27). 3. Added the AT command for communication interface setting. (Chapter 3.2). 4. Added the peak current capability requirement of the power supply and deleted the rated current requirement of the power supply (Chapter 3.3). 5. Updated the reference circuit for power supply (Figure 7). 6. Updated the timing and related comment of T_{on} and T_{on3} (Table 10 and Table 14). 7. Added a reference circuit for laptop PCIe reset logic (Figure 10). 8. Added descriptions to explain the timing control of AUX Reset and Global PCIe Reset in the Laptop application scenario (Chapter 3.4). 9. Added the instruction of PCIe $D3_{cold}$ State (Chapter 4.3.4). 10. Updated VSWR parameter in antenna requirements (Chapter 5.3). 11. Added the notification of module installing (Chapter 6.8.3).

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1 Introduction

1.1. Introduction

The document introduces RM520N series module and describes its air interface and hardware interfaces which are connected to your applications.

This document helps you quickly understand the interface specifications, RF characteristics, electrical and mechanical details, as well as other related information of the module. To facilitate its application in different fields, reference design is also provided for reference. Associated with application notes and user guides, you can use the module to design and set up mobile applications easily. You can also see ***document [1]*** to understand the module hardware architecture.

1.2. Reference Standard

The module complies with the following standards:

- *PCI Express M.2 Specification Revision 4.0, Version 1.0*
- *PCI Express Base Specification Revision 4.0*
- *Universal Serial Bus 3.1 Specification*
- *ISO/IEC 7816-3*
- *MIPI Alliance Specification for RF Front-End Control Interface version 2.0*
- *3GPP TS 27.007* and *3GPP TS 27.005*

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

RM520N is a series of 5G NR/LTE-FDD/LTE-TDD/UMTS/HSPA+ wireless communication modules with receive diversity. It provides data connectivity on 5G NR SA and NSA, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks. RM520N series is a standard M.2 Key-B WWAN module. For more details, see *PCI Express M.2 Specification Revision 4.0, Version 1.0*.

RM520N series supports embedded operating systems such as Windows, Linux and Android, and also provides GNSS and voice* functions to meet specific application demands.

RM520N is a series of industrial-grade modules for industrial and commercial applications only.

The following table shows the frequency bands, MIMO and GNSS systems supported by the module.

Table 2: RM520N-GL Frequency Bands & MIMO & GNSS Systems

Mode	Frequency Bands
5G NR SA	n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n29/n30/n38/n40/n41/n48/n66/n70/n71/n75/n76/n77/n78/n79 **DL 4 × 4 MIMO**: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n70/n77/n78/n79 **UL 2 × 2 MIMO**: n38/n41/n48/n77/n78/n79
5G NR NSA	n1/n2/n3/n5/n7/n8/n12/n13/n14/n18/n20/n25/n26/n28/n29/n30/n38/n40/n41/n48/n66/n70/n71/n75/n76/n77/n78/n79 **DL 4 × 4 MIMO**: n1/n2/n3/n7/n25/n30/n38/n40/n41/n48/n66/n70/n77/n78/n79
LTE	FDD: B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71 TDD: B34/B38/B39/B40/B41/B42/B43/B46(LAA)/B48 **DL 4 × 4 MIMO**: B1/B2/B3/B4/B7/B25/B30/B38/B40/B41/B42/B43/B48/B66
WCDMA	B1/B2/B4/B5/B8/B19
GNSS	GPS/GLONASS/BDS/Galileo/QZSS

Table 3: RM520N-EU Frequency Bands & MIMO & GNSS Systems

Mode	Frequency Bands
5G NR SA	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n71/n75/n76/n77/n78 **DL 4 × 4 MIMO**: n1/n3/n7/n38/n40/n41/n77/n78 **UL 2 × 2 MIMO**: n38/n40/n41/n77/n78
5G NR NSA	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n71/n75/n76/n77/n78 **DL 4 × 4 MIMO**: n1/n3/n7/n38/n40/n41/n77/n78
LTE	FDD: B1/B3/B5/B7/B8/B20/B28/B32/B71 TDD: B38/B40/B41/B42/B43 **DL 4 × 4 MIMO**: B1/B3/B7/B38/B40/B41/B42/B43
WCDMA	B1/B5/B8
GNSS	GPS/GLONASS/BDS/Galileo/QZSS

The module can be applied to the following fields:

- Rugged tablet PC and laptop computer
- Remote monitor system
- Smart metering system
- Wireless CPE
- Smart TV
- Outdoor live streaming equipment
- Wireless router and switch
- Other wireless terminal devices

2.2. Key Features

Table 4: Key Features of RM520N series

Feature	Details
Function Interface	PCI Express M.2 Interface
Power Supply	● Supply voltage: 3.135–4.4 V ● Typical supply voltage: 3.7 V
(U)SIM Interface	● Compliant with *ISO/IEC 7816-3*, ETSI and IMT-2000 ● Supported (U)SIM card: Class B (3.0 V) and Class C (1.8 V) ● (U)SIM1 and (U)SIM2 interfaces ● Dual SIM Single Standby
eSIM	Optional eSIM function
USB Interface	● Compliant with USB 3.1 Gen2 and USB 2.0 specifications ● Maximum transmission rates: – USB 3.1 Gen2: 10 Gbps – USB 2.0: 480 Mbps ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice over USB* ● Supported USB serial drivers: – Windows 7/8/8.1/10 – Linux 2.6–5.18 – Android 4.x–12.x
PCIe Interface	● Compliant with PCIe Gen3 ● PCIe × 1 lane, supporting up to 8 Gbps ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output
Transmitting Power	**RM520N-GL:** ● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR HPUE bands (n38/n40/n41/n77/n78/n79): Class 2 (26 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE HPUE [1] bands (B38/B41/B42/B43): Class 2 (26 dBm ±2 dB) ● WCDMA bands: Class 3 (23 dBm ±2 dB) **RM520N-EU:** ● 5G NR bands: Class 3 (23 dBm ±2 dB) ● 5G NR HPUE bands (n38/n41/n77/n78): Class 2 (26 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm ±2 dB) ● LTE bands HPUE [1] bands (B38/B41B42/B43): Class 2 (26 dBm ±2 dB)

[1] HPUE is only for single carrier.

	● WCDMA bands: Class 3 (23 dBm ±2 dB)
5G NR Features	**RM520N-GL:** ● Supports 3GPP Rel-16 ● Supported modulations: - Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports SCS 15 kHz [2] and 30 kHz [2] ● Supports SA [3] and NSA [3] operation modes on all the 5G band ● Supports Option 3x, 3a, 3 and Option 2 ● Max. transmission data rates [4]: - NSA: 3.4 Gbps (DL), 550 Mbps (UL) - SA: 2.4 Gbps (DL), 900 Mbps (UL) **RM520N-EU:** ● Supports 3GPP Rel-16 ● Supported modulations: - Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM - Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports SCS 15 kHz [5] and 30 kHz [2] ● Supports SA [3] and NSA [3] operation modes on all the 5G band ● Supports Option 3x, 3a, 3 and Option 2 ● Max. transmission data rates [6]: - NSA: 3.4 Gbps (DL), 550 Mbps (UL) - SA: 2.4 Gbps (DL), 900 Mbps (UL)
LTE Features	● Supports 3GPP Rel-16 ● LTE Category: DL Cat 19/ UL Cat 18 ● Supported modulations: - Uplink: QPSK, 16QAM and 64QAM and 256QAM - Downlink: QPSK, 16QAM and 64QAM and 256QAM ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Max. transmission data rates [4]: 1.6 Gbps (DL), 200 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulation ● Max. transmission data rates [4]: - DC-HSDPA: 42 Mbps (DL) - HSUPA: 5.76 Mbps (UL) - WCDMA: 384 kbps (DL), 384 kbps (UL)
Rx-diversity	● Supports 5G NR/LTE/WCDMA Rx-diversity

[2] 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.
[3] See ***document [2]*** for bandwidth supported by each frequency band in the NSA and SA modes.
[4] The maximum rates are theoretical and the actual values refer to the network configuration.
[5] 5G NR FDD bands only support 15 kHz SCS, and NR TDD bands only support 30 kHz SCS.
[6] The maximum rates are theoretical and the actual values refer to the network configuration.

GNSS Features	● Protocol: NMEA 0183 ● Data Update Rate: 1 Hz
Antenna Interfaces	● RM520N-GL: ANT0, ANT1, ANT2, and ANT3 ● RM520N-EU: ANT0, ANT1, ANT2, ANT3 and ANT4
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Internet Protocol Features	● Supports NITZ, PING and QMI protocols ● Supports PAP and CHAP for PPP connections
Firmware Upgrade	● USB 2.0 & USB 3.1 interface ● PCIe interface ● (D)FOTA (A/B system updates supported)
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
Physical Characteristics	● M.2 Key-B ● Size: 30.0 mm × 52.0 mm × 2.3 mm ● Weight: approx. 8.7 g
Temperature Range	● Operating temperature range: -30 °C to +75 °C [7] ● Extended temperature range: -40 °C to +85 °C [8] ● Storage temperature range: -40 °C to +90°C
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (5G-M2 EVB) with accessories to control or test the module. For more details, see ***document [3]***.

[7] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
[8] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice*, SMS, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

2.4. Functional Diagram

The following figure shows a block diagram of RM520N series

- Power management
- Baseband
- LPDDR4X SDRAM + NAND Flash
- Radio frequency
- M.2 Key-B interface

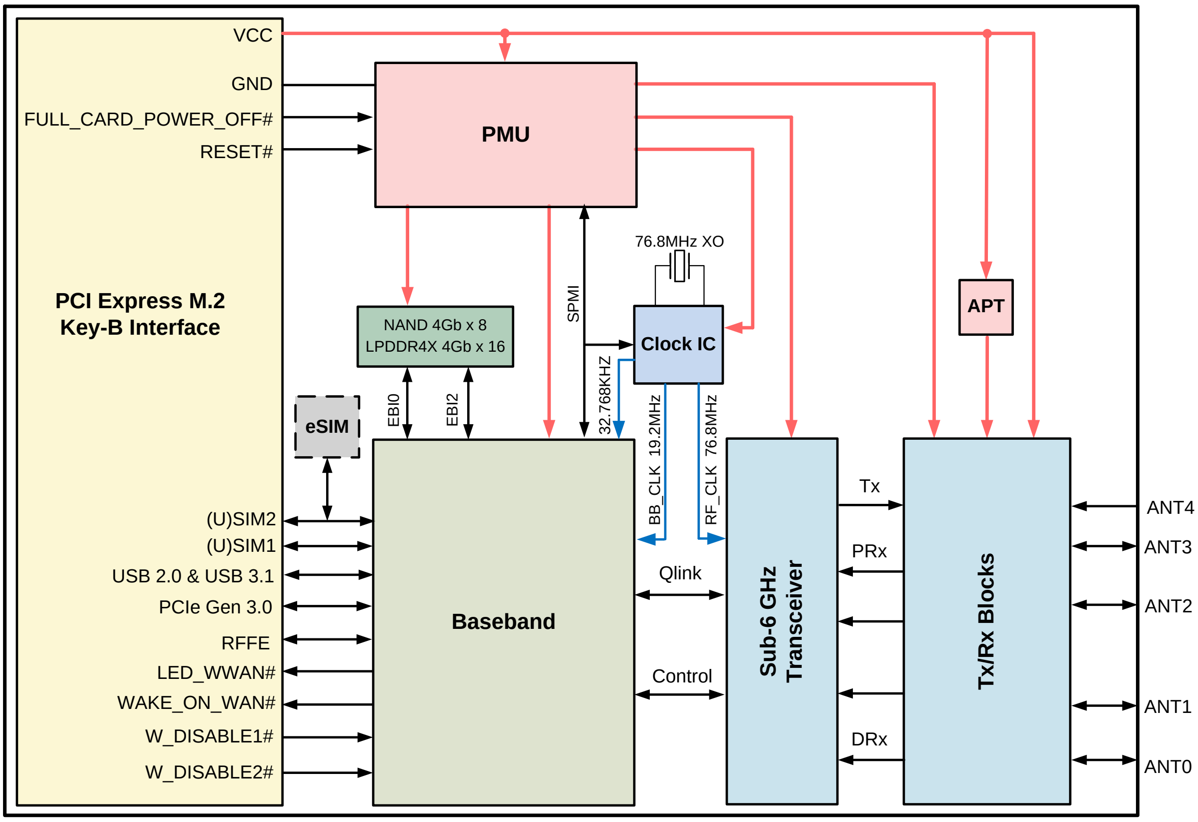


Figure 1: Functional Diagram

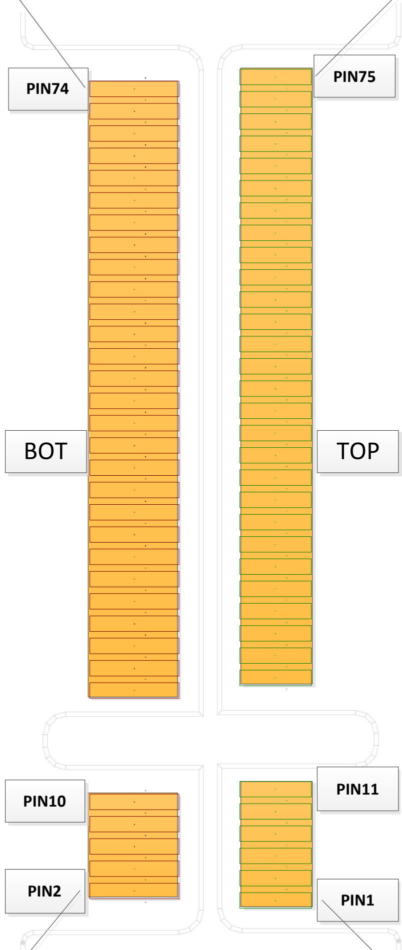
NOTE

RM520N-EU supports 5 antennas (ANT0, ANT1, ANT2, ANT3 and ANT4). ANT4 supports GNSS function (GNSS L1 + L5) by default. You may also choose ANT3 to support GNSS L1 function according to actual needs. For details, please contact Quectel Technical Support.

2.5. Pin Assignment

The following figure shows the pin assignment of the RM520N series.

No.	Pin Name
74	VCC
72	VCC
70	VCC
68	RESERVED
66	USIM1_DET
64	COEX_TXD
62	COEX_RXD
60	N79_TX_EN/NC
58	RFFE_DATA
56	RFFE_CLK
54	PCIE_WAKE_N
52	PCIE_CLKREQ_N
50	PCIE_RST_N
48	USIM2_VDD
46	USIM2_RST
44	USIM2_CLK
42	USIM2_DATA
40	USIM2_DET
38	WLAN_TX_EN/NC
36	USIM1_VDD
34	USIM1_DATA
32	USIM1_CLK
30	USIM1_RST
28	RESERVED/PCM_SYNC
26	W_DISABLE2#
24	VDDIO_1V8/PCM_DOUT
22	RESERVED/PCM_DIN
20	RESERVED/PCM_CLK
	Notch
	Notch
	Notch
	Notch
10	LED_WWAN#
8	W_DISABLE1#
6	FULL_CARD_POWER_OFF#
4	VCC
2	VCC



Pin Name	No.
CONFIG_2	75
GND	73
GND	71
CONFIG_1	69
RESET#	67
RESERVED	65
RESERVED	63
RESERVED	61
RESERVED	59
GND	57
PCIE_REFCLK_P	55
PCIE_REFCLK_M	53
GND	51
PCIE_RX_P	49
PCIE_RX_M	47
GND	45
PCIE_TX_P	43
PCIE_TX_M	41
GND	39
USB_SS_RX_P	37
USB_SS_RX_M	35
GND	33
USB_SS_TX_P	31
USB_SS_TX_M	29
GND	27
DPR	25
WAKE_ON_WAN#	23
CONFIG_0	21
Notch	
Notch	
Notch	
Notch	
GND	11
USB_DM	9
USB_DP	7
GND	5
GND	3
CONFIG_3	1

Figure 2: Pin Assignment [9]

[9] Pins 20/22/24/28 are defined as PCM pins for RM520N-EU, while as RESERVED (Pins 20/22/28) and VDDIO_1V8 (Pin 24) pins for RM520N-GL.

2.6. Pin Description

Table 5: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

The following table shows the pin definition and description of the module.

Table 6: Pin Description

Pin No.	Pin Name	I/O	Description	DC Characteristic	Comment
1	CONFIG_3	DO	Not connected internally		
2	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
3	GND		Ground		
4	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
5	GND		Ground		
6	FULL_CARD_ POWER_OFF#	DI	Turn on/off the module High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Internally pulled down with a 100 kΩ resistor.

7	USB_DP	AIO	USB differential data (+)		Test point must be reserved.
8	W_DISABLE1#	DI	Airplane mode control Active LOW	1.8/3.3 V	Internally pulled up to 1.8 V with a 100 kΩ resistor.
9	USB_DM	AIO	USB differential data (-)		Test point must be reserved.
10	LED_WWAN#	OD	RF status LED indicator Active LOW	VCC	
11	GND		Ground		
12	Notch		Notch		
13	Notch		Notch		
14	Notch		Notch		
15	Notch		Notch		
16	Notch		Notch		
17	Notch		Notch		
18	Notch		Notch		
19	Notch		Notch		
20 [10]	RESERVED				
	PCM_CLK	DIO	PCM clock	1.8 V	
21	CONFIG_0	DO	Not connected internally		
22 [10]	RESERVED				
	PCM_DIN	DI	PCM data input	1.8 V	
23	WAKE_ON_WAN#	OD	Wake up the host Active LOW	1.8/3.3 V	
24 [10]	VDDIO_1V8	PO	Provide 1.8 V for external circuit	1.8 V	Maximum output current: 50 mA
	PCM_DOUT	DO	PCM data output	1.8 V	
25	DPR	DI	Dynamic power reduction	1.8 V	

[10] Pins 20/22/24/28 are defined as PCM pins for RM520N-EU, while as RESERVED (Pins 20/22/28) and VDDIO_1V8 (Pin 24) pins for RM520N-GL.

26	W_DISABLE2#	DI	GNSS control Active LOW	1.8/3.3 V	Internally pulled up to 1.8 V with a 100 kΩ resistor.
27	GND		Ground		
28 [10]	RESERVED				
	PCM_SYNC	DIO	PCM data frame sync	1.8 V	
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)		
30	USIM1_RST	DO	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V	
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)		
32	USIM1_CLK	DO	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V	
33	GND		Ground		
34	USIM1_DATA	DIO	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V	
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)		
36	USIM1_VDD	PO	(U)SIM1 card power supply	USIM1_VDD 1.8/3.0 V	
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)		
38 [11]	WLAN_TX_EN*	DI	Notification from WLAN to SDR when WLAN transmitting	1.8 V	
	NC				
39	GND		Ground		
40	USIM2_DET [12]	DI	(U)SIM2 card hot-plug detect	1.8 V	
41	PCIE_TX_M	AO	PCIe transmit (-)		
42	USIM2_DATA	DIO	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V	
43	PCIE_TX_P	AO	PCIe transmit (+)		

[11] Pin 38 is defined as WLAN_TX_EN for RM520N-GL, while as NC for RM520N-EU.
[12] USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

44	USIM2_CLK	DO	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
45	GND		Ground	
46	USIM2_RST	DO	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
47	PCIE_RX_M	AI	PCIe receive (-)	
48	USIM2_VDD	PO	(U)SIM2 card power supply	USIM2_VDD 1.8/3.0V
49	PCIE_RX_P	AI	PCIe receive (+)	
50	PCIE_RST_N	DI [13]	PCIe reset Active LOW	1.8/3.3 V
51	GND		Ground	
52	PCIE_CLKREQ_N	OD [13]	PCIe clock request Active LOW	1.8/3.3 V
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
54	PCIE_WAKE_N	OD [13]	PCIe wake up Active LOW	1.8/3.3 V
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	
56	RFFE_CLK* [14]	DO	Used for external MIPI IC control	1.8 V
57	GND		Ground	
58	RFFE_DATA* [14]	DIO	Used for external MIPI IC control	1.8 V
59	RESERVED			
60 [15]	N79_TX_EN*	DO	Notification from SDR to WLAN when n79 transmitting	1.8 V
	NC			
61	RESERVED			
62	COEX_RXD* [16]	DI	5G/LTE and WLAN coexistence receive	1.8 V

[13] PCIE_RST_N behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. PCIE_CLKREQ_N and PCIE_WAKE_N behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.
[14] If this function is required, please contact Quectel for more details.
[15] Pin 60 is defined as N79_TX_EN for RM520N-GL, while as NC for RM520N-EU.
[16] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.

63	RESERVED				
64	COEX_TXD* [16]	DO	5G/LTE and WLAN coexistence transmit	1.8 V	
65	RESERVED				
66	USIM1_DET [12]	DI	(U)SIM1 card hot-plug detect	1.8 V	
67	RESET#	DI	Reset the module Active LOW	1.8 V	Internally pulled up to 1.8 V. Test point is recommended to be reserved if unused.
68	RESERVED				
69	CONFIG_1	DO	Connected to GND internally		
70	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
71	GND		Ground		
72	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
73	GND		Ground		
74	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V	
75	CONFIG_2	DO	Not connected internally		

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. When the module is connected with an IPQ device to achieve Wi-Fi function, pin 68, pin 64, and pin 62 can be used for status signal between the IPQ device and the module.
   - Pin 68 (AP2SDX_STATUS): Status indication signal from the IPQ device to the module
   - Pin 64 (SDX2AP_STATUS): Status indication signal from the module to the IPQ device
   - Pin 62 (SDX2AP_E911_STATUS): E911 status indication signal from the module to IPQ device.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice*/Data	Network is connected. In this mode, the power consumption is determined by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE1# pin LOW will set the module to airplane mode. In this mode, the RF function is invalid.	
Sleep Mode	When **AT+QSCLK=1** command is executed and the host's USB enters suspend mode, the module will enter sleep mode. The module keeps receiving paging messages, SMS, voice calls* and TCP/UDP data from the network with its current consumption reducing to the minimal level.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VCC) remains applied.	

NOTE

For more details about the AT command, see ***document [4]***.

3.1.1. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during the sleep mode, and DRX cycle values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current consumption in sleep mode. The longer the DRX cycle is, the lower the current consumption will be.

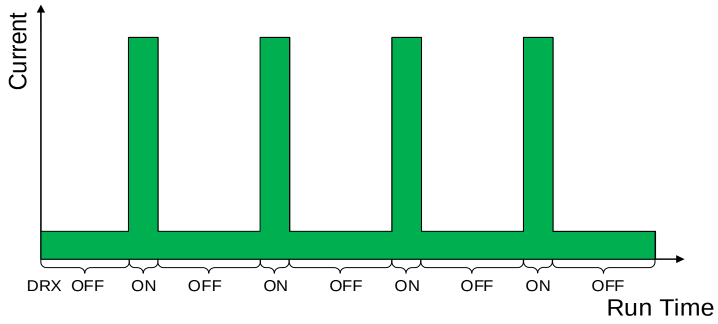


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

The following part of this section presents the power saving procedure and sleep mode of the module.

If the host supports USB suspend/resume and remote wakeup function, the following two conditions must be met to set the module to sleep mode.

- Execute **AT+QSCLK=1** command.
- The module's USB interface enters suspend mode.

The following figure shows the connection between the module and the host.

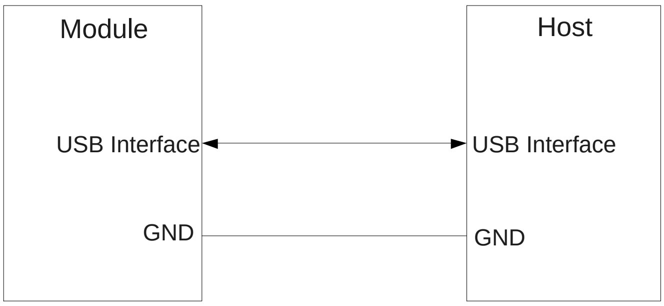


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will wake up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wake-up signals via USB to wake up the host.

3.1.2. Airplane Mode

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. See ***Chapter 4.4.1*** for more details.

3.2. Communication Interface with a Host

The module supports to communicate through both USB and PCIe interfaces, respectively referring to the USB mode and the PCIe mode as described below:

USB Mode

- Supports all USB 2.0/3.1 features
- Supports MBIM/QMI/QRTR/AT over USB interface
- Communication can be switched to PCIe mode by AT command

USB is the default communication interface between the module and the host. To use PCIe interface for the communication between a host, an AT command under USB mode can be used. For more details about the AT command, see ***document [4]***.

It is suggested that USB 2.0 interface be reserved for firmware upgrade.

USB-AT-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT over PCIe interface
- Supports AT over USB interface
- Communication can be switched back to USB mode by AT command

When the module works at the USB-AT-based (switched from USB mode by AT command) PCIe mode, it can be switched back to USB mode by **AT+QCFG= "data_interface",0,0**. For more details about the command, see ***document [4]***.

For USB-AT-based PCIe mode, the firmware upgrade via PCIe interface is not supported, so USB 2.0 interface must be reserved for the firmware upgrade.

eFuse-based PCIe Mode

- Supports MBIM/QMI/QRTR/AT over PCIe interface
- Supports Non-X86 systems and X86 system (supports BIOS PCIe early initial)

The module can also be reprogrammed to PCIe mode based on eFuse. If switched to PCIe mode by burnt eFuse, the communication cannot be switched back to USB mode.

Note that if the host does not support firmware upgrade through PCIe, the firmware can be upgraded by the 5G-M2 EVB, which could be connected to PC with a USB cable. For more details, see ***document [3]***.

3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

Table 8: Definition of VCC and GND Pins

Pin	Pin Name	I/O	Description	DC Characteristics
2, 4, 70, 72, 74	VCC	PI	Power supply for the module	Vmin = 3.135 V Vnom = 3.7 V Vmax = 4.4 V
3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND	-	Ground	-

3.3.1. Voltage Stability Requirements

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will power off automatically. The voltage ripple of the input power supply should be less than 100 mV. The figure below shows the power supply limits during burst transmission when 3.3 V power supply is applied.

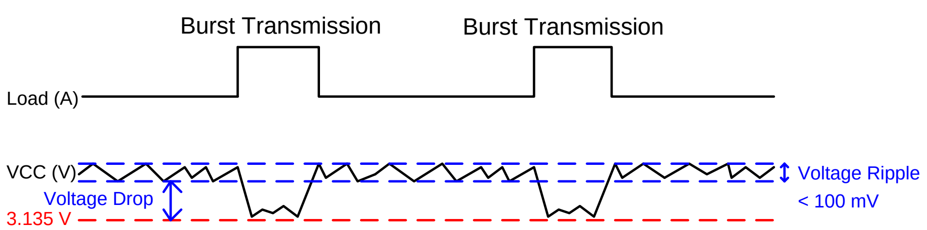


Figure 5: Power Supply Limits during Burst Transmission

Ensure the continuous current capability of the power supply is 3.0 A at least and the peak current capability of the power supply is 4 A at least. To decrease the voltage drop, two bypass capacitors of 220 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its ultra-low ESR. It is recommended to use ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be not less than 3 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, to guarantee stability of the power supply, it is recommended to use a TVS with working peak reverse voltage of 5 V.

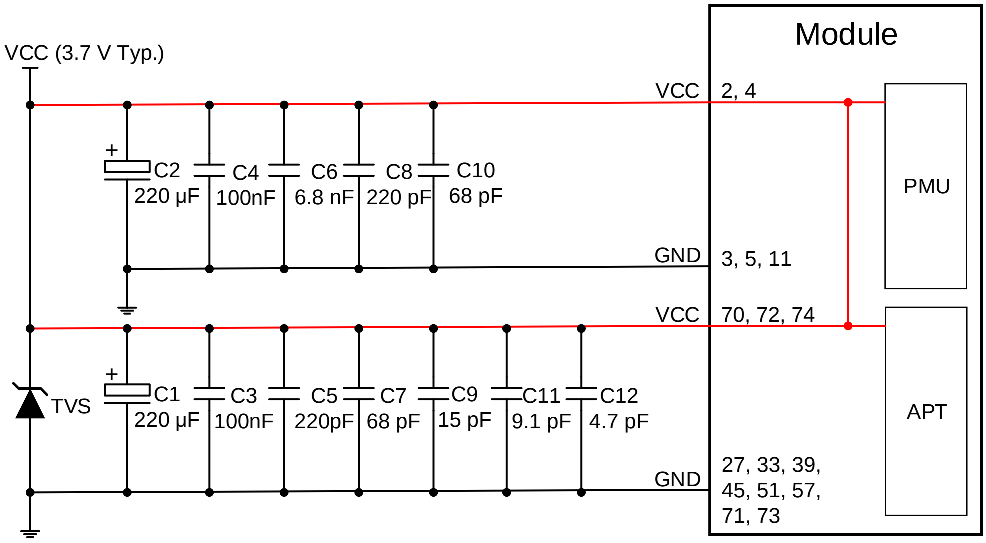


Figure 6: Reference Circuit for VCC

3.3.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage difference between the input and output is not too big, it is suggested that an LDO should be used when supplying power for the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V Typ.), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5.0 V input power source based on a DC-DC converter. The typical output of the power supply is 3.7 V.

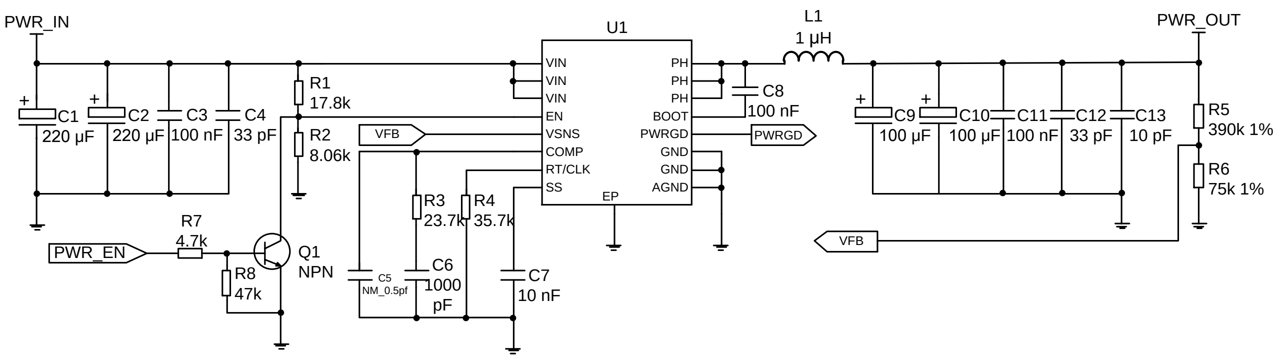


Figure 7: Reference Circuit for Power Supply

NOTE

To avoid corrupting the data in the internal flash, DO NOT cut off the power supply before the module is completely turned off by pulling down FULL_CARD_POWER_OFF# pin for more than 900 ms, and DON'T cut off power supply directly when the module is working.

3.3.3. Power Supply Monitoring

AT+CBC can be used to monitor the voltage value of VCC. For more details about the AT command, see ***document [4]***.

3.4. Turn On

FULL_CARD_POWER_OFF# is used to turn on/off the module or reset the module through hard reset. This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. And it has internally pulled down with a 100 kΩ resistor.

When FULL_CARD_POWER_OFF# is de-asserted (driven HIGH, ≥ 1.19 V), the module will turn on.

Table 9: Definition of FULL_CARD_POWER_OFF#

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
6	FULL_CARD_ POWER_OFF#	DI	Turn on/off the module. High level: Turn on Low level: Turn off	V_{IH}max = 4.4 V V_{IH}min = 1.19 V V_{IL}max = 0.2 V	Pull down with a 100 kΩ resistor.

It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated by the following figure.

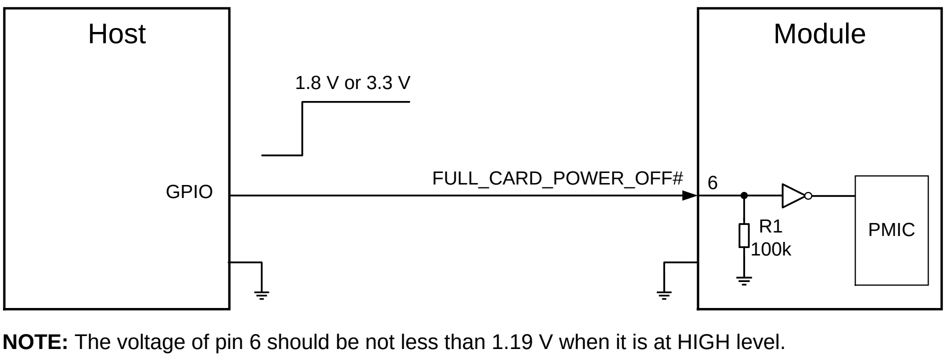
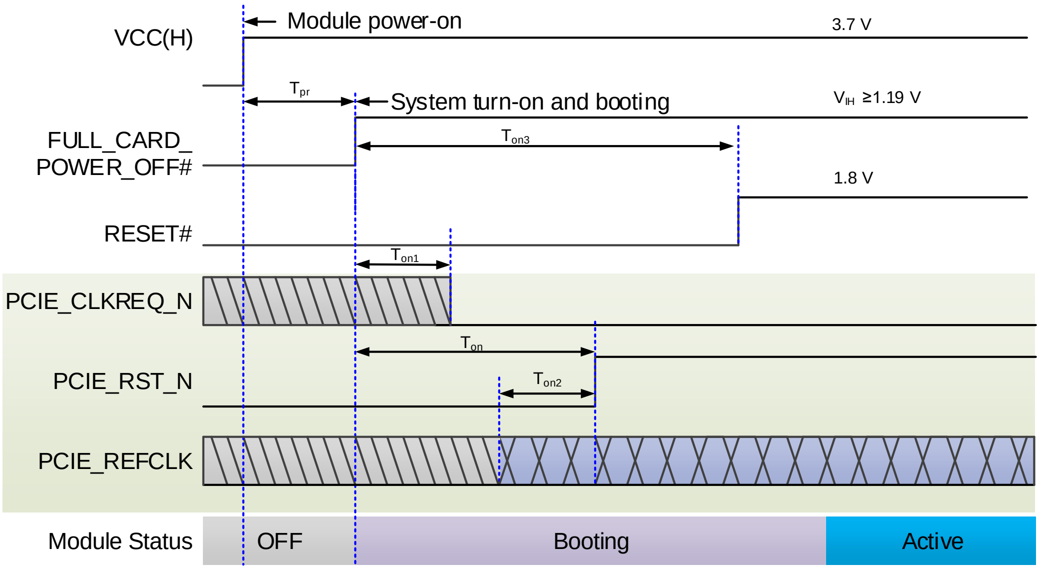


Figure 8: Turn on the Module with a Host GPIO

The timing of turn-on scenario is illustrated by the following figure.



NOTE: When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 9: Turn-on Timing of the Module

Table 10: Turn-on Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T_{pr}	100 ms	-	-	Power-on time of the module before system turning-on and booting depending on the host.
T_{on1}	-	-	$T_{on} – T_{on2}$	The period when the module requests the PCIe clock from the host.
T_{on}	100 ms	-	-	The period when the host GPIO controls the module to exit the PCIe reset state. 1. For eFuse-based PCIe mode, Min. T_{on} is 100 ms. 2. For USB-AT-based PCIe mode, Typ. T_{on} is 3 s.
	-	3 s	-	
T_{on2}	100 µs	-	-	The period during which PCIE_REFCLK_P/M is stable before PCIE_RST_N is de-asserted.
T_{on3} [17]	400 ms	-	-	The module will pull up RESET# internally and automatically after FULL_CARD_POWER_OFF# is de-asserted.

[17] At booting stage, the host must not drive RESET# low after FULL_CARD_POWER_OFF# is de-asserted.

For the laptop application scenario, there are two reset signals to control PCIE_RST_N pin of the module, and the following figure is for reference. It is recommended that AUX Reset be pulled up before Global PCIe Reset is de-asserted.

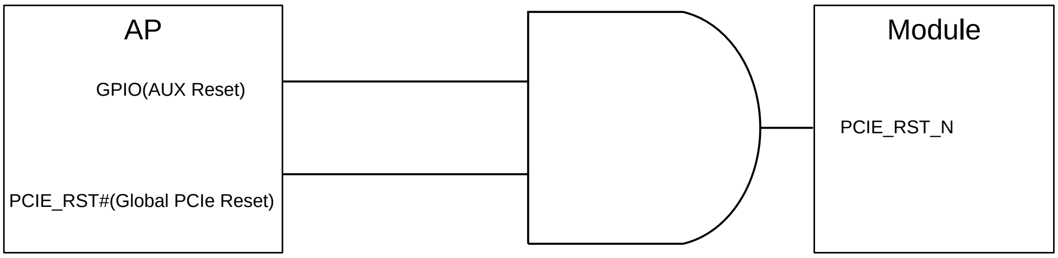


Figure 10: Reference Circuit for Laptop PCIe Reset Logic

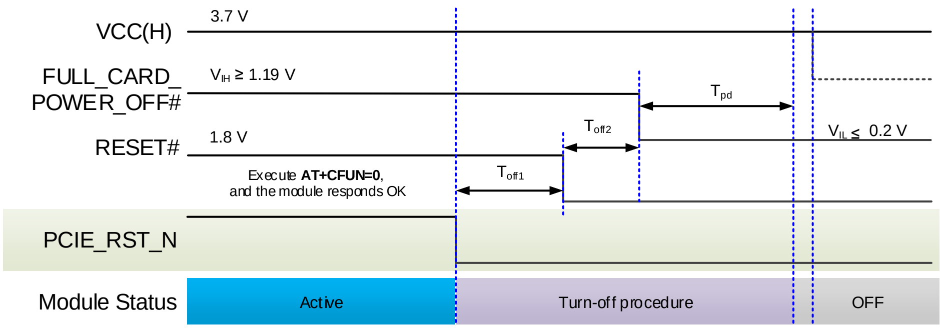
3.5. Turn Off

For the design that turns on the module with a host GPIO, when the power is supplied to VCC, driving FULL_CARD_POWER_OFF# pin LOW (≤ 0.2 V) or tri-stating the pin will turn off the module. Sending the command **AT+CFUN=0** is necessary before shutting down the module.

The following is a proper shutdown handshake for FULL_CARD_POWER_OFF#, which complies with the M.2 specification. Only after this process is completed, can the module be successfully turned off by pulling down FULL_CARD_POWER_OFF#.

1. The host sends **AT+CFUN=0** to the module.
2. The module will do the essential shutdown tasks.
3. The module responds **OK**.

The timing of turn-off scenario is illustrated by the following figure.



NOTE:
When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 11: Turn-off Timing through FULL_CARD_POWER_OFF#

Table 11: Turn-off Timing of the Module through FULL_CARD_POWER_OFF#

Symbol	Min.	Typ.	Max.	Comment
T_{off1}	-	100 ms	-	The period from the host pulling down PCIE_RST_N to it pulling down RESET#.
T_{off2}	0 ms	100 ms	-	The period from the host pulling down RESET# to it pulling down FULL_CARD_POWER_OFF#.
T_{pd}	900 ms	-	-	The period from the host pulling down FULL_CARD_POWER_OFF# to the module turning off. It is recommended to cut off VCC when the module has been powered off completely.

3.6. Reset

RESET# is an active LOW signal (1.8 V logic level). When this pin is asserted, the module will immediately enter reset condition.

Please note that triggering the RESET# signal will lead to loss of all data in the module and removal of system drivers. It will also disconnect the modem from the network.

Table 12: Definition of RESET# Pin

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
67	RESET#	DI	Reset the module. Active LOW	1.8 V	Internally pulled up to 1.8 V. Test point is recommended to be reserved if unused.

The module can be reset by pulling down the RESET#. An open collector/drain driver or a button can be used to control RESET#.

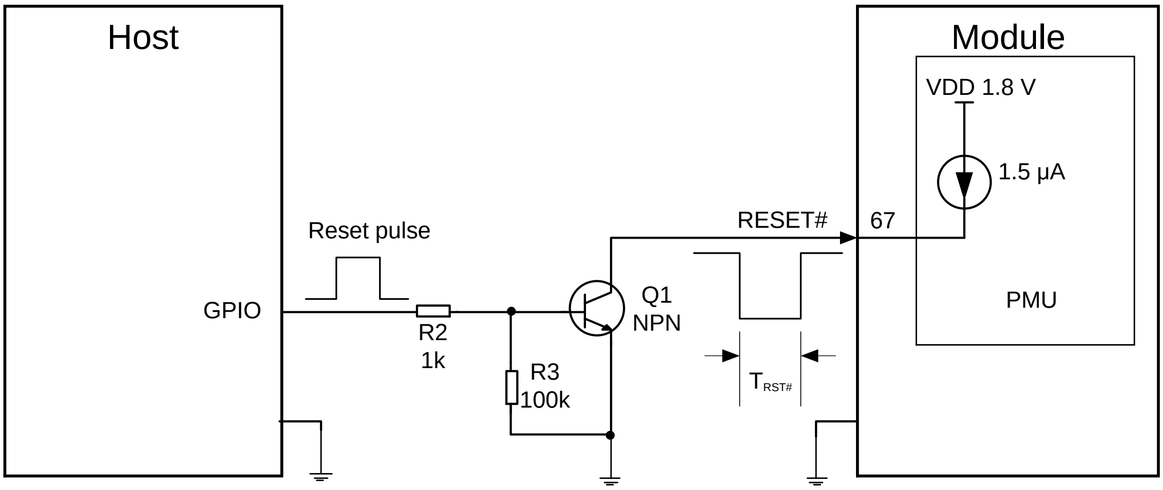
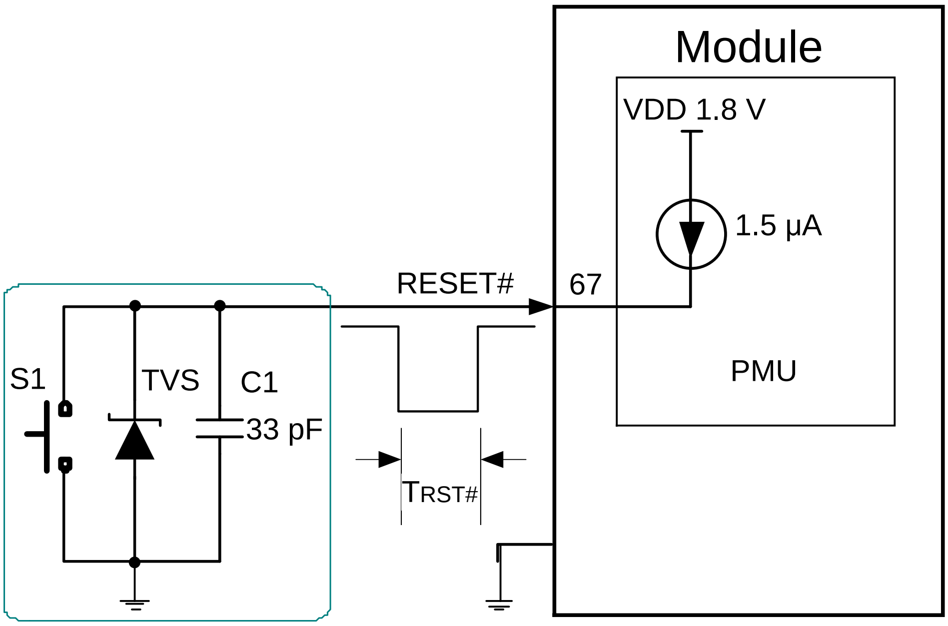


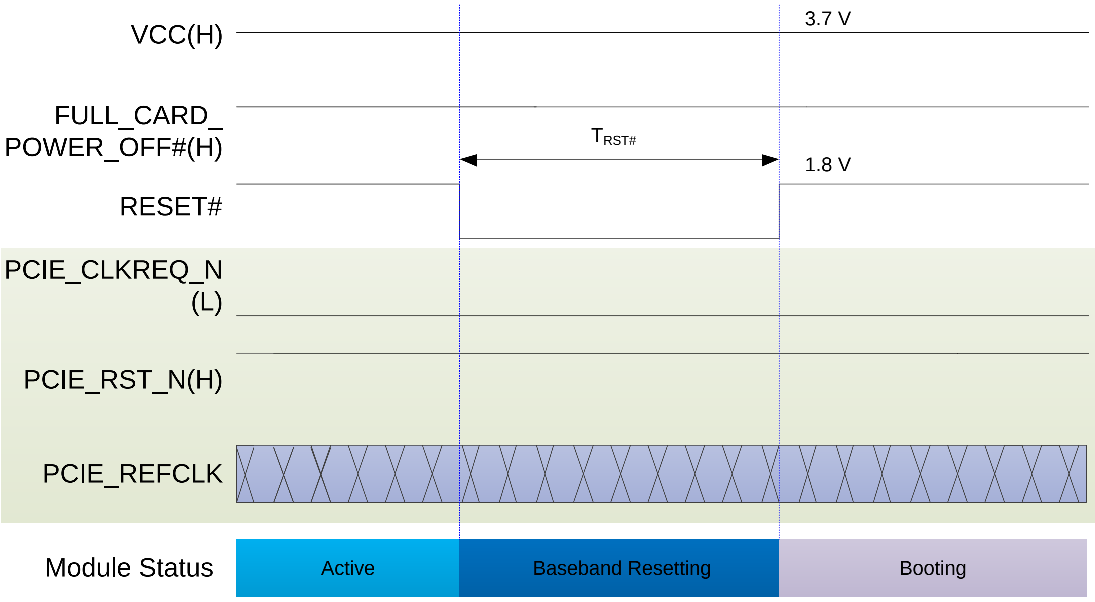
Figure 12: Reference Circuit for RESET# with NPN Driver Circuit



NOTE: The capacitor C1 is recommended to be less than 47 pF.

Figure 13: Reference Circuit for RESET# with a Button

For a warm reset when only the reset signal is pulled LOW, see the timing illustrated by the figure below. In this reset mode, the power of the module will not be turned off. This timing sequence is recommended for scenarios where the module is reset with a button.



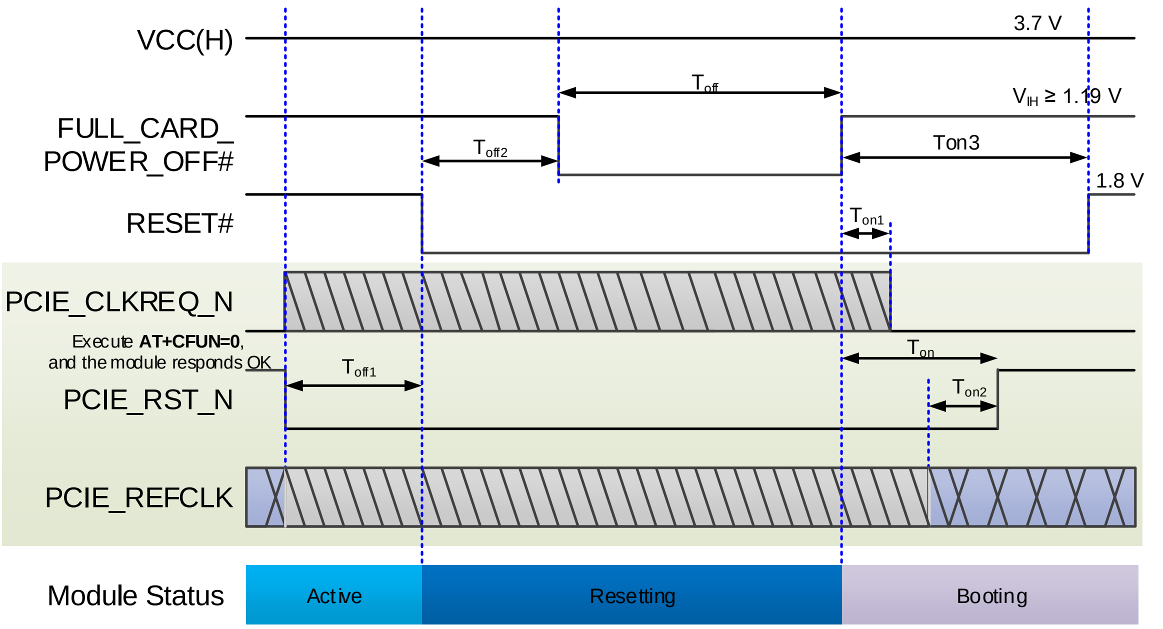
NOTE:
When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 14: Reset Timing of the Module's Warm Reset

Table 13: Reset Timing of the Module's Warm Reset

Symbol	Min.	Typ.	Max.	Comment
$T_{RST\#}$	200 ms	400 ms	-	Reset baseband chip IC only

For a hard reset, see the timing illustrated by the figure below. This timing sequence is recommended for scenarios where the module is reset with NPN driver circuit. Sending the command **AT+CFUN=0** is necessary before resetting the module.



NOTE:
1. The timing parameters after the host pulls up FULL_CARD_POWER_OFF# refer to the boot timing of the PCIe mode module.
2. When the module is in USB mode, please ignore the PCIe related signals and their timing parameters in the figure.

Figure 15: Reset Timing of the Module's Hard Reset

Table 14: Reset Timing of the Module's Hard Reset

Symbol	Min.	Typ.	Max.	Comment
T_{off1}	-	100 ms	-	The period from the host pulling down PCIE_RST_N to it pulling down RESET#.
T_{off2}	0 ms	100 ms	-	The period from the host pulling down RESET# to it pulling down FULL_CARD_POWER_OFF#.
T_{off}	900 ms	-	-	Module hard reset. Ensure that the module has been turned off completely.
T_{on1}	-	-	T_{on} - T_{on2}	The period when the module requests the PCIe clock from the host.
T_{on}	100 ms	-	-	The period when the host GPIO controls the module to exit the PCIe reset state. 1. For eFuse-based PCIe mode, Min. T_{on} is 100 ms. 2. For USB-AT-based PCIe mode, Typ. T_{on} is 3 s.
	-	3 s	-	
T_{on2}	100 µs	-	-	The period during which REFCLK_P/M is stable before PCIE_RST_N is de-asserted.
T_{on3} [17]	400 ms	-	-	The module will pull up RESET# internally and automatically after FULL_CARD_POWER_OFF# is de-asserted.

4 Application Interfaces

The physical connections and signal levels of the module comply with the PCI Express M.2 specification. This chapter mainly describes the definition and application of the following interfaces/pins of the module:

- (U)SIM interfaces
- USB interface
- PCIe interface
- Control and indication interfaces
- Cellular/WLAN COEX interface
- Antenna tuner control interface
- Configuration pins
- PCM interface

4.1. (U)SIM Interfaces

The (U)SIM interface circuitry meets *ISO/IEC 7816-3,* ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported.

4.1.1. Pin Definition of (U)SIM

The module has two (U)SIM interfaces, and supports dual SIM single standby.

Table 15: Pin Definition of (U)SIM Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics
36	USIM1_VDD	PO	(U)SIM1 card power supply	USIM1_VDD 1.8/3.0 V
34	USIM1_DATA	DIO	(U)SIM1 card data	USIM1_VDD 1.8/3.0 V
32	USIM1_CLK	DO	(U)SIM1 card clock	USIM1_VDD 1.8/3.0 V
30	USIM1_RST	DO	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V

66	USIM1_DET	DI	(U)SIM1 card hot-plug detect	1.8 V
48	USIM2_VDD	PO	(U)SIM2 card power supply	USIM2_VDD 1.8/3.0V
42	USIM2_DATA	DIO	(U)SIM2 card data	USIM2_VDD 1.8/3.0 V
44	USIM2_CLK	DO	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V
46	USIM2_RST	DO	(U)SIM2 card reset	USIM2_VDD 1.8/3.0 V
40	USIM2_DET	DI	(U)SIM2 card hot-plug detect	1.8 V

4.1.2. (U)SIM Hot-Plug

The module supports (U)SIM card hot-plug via the (U)SIM card hot-plug detect pins (USIM1_DET and USIM2_DET), which is disabled by default. (U)SIM card is detected by USIM_DET interrupt. (U)SIM card insertion is detected by high/low level.

The following command enables or disables (U)SIM card hot-plug function. The level of (U)SIM card detection pin should also be set when the (U)SIM card is inserted.

AT+QSIMDET	**(U)SIM Card Detection**
Test Command **AT+QSIMDET=?**	Response **+QSIMDET: (**list of supported **<enable>**s)**,(**list of supported **<insert_level>**s**)** **OK**
Read Command **AT+QSIMDET?**	Response **+QSIMDET: <enable>,<insert_level>** **OK**
Write Command **AT+QSIMDET=<enable>,<insert_level>**	Response **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<enable>	Integer type. Enable or disable (U)SIM card detection. 0 Disable 1 Enable
<insert_level>	Integer type. The level of (U)SIM detection pin when a (U)SIM card is inserted. 0 Low level 1 High level

NOTE

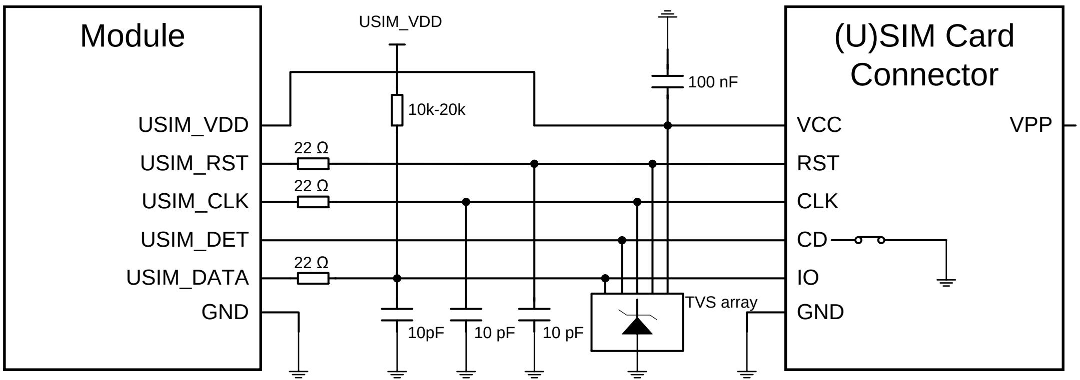
1. Hot-plug function is invalid if the configured value of **<insert_level>** is inconsistent with hardware design.
2. Hot-plug function takes effect after the module is restarted.
3. The underlined value is the default.
4. USIM1_DET and USIM2_DET are pulled LOW by default, and will be internally pulled up to 1.8 V by software configuration only when (U)SIM hot-plug is enabled by **AT+QSIMDET**.

4.1.3. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET pin is shorted to ground when there is no (U)SIM card inserted. (U)SIM card detection by high level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,1**, a (U)SIM card insertion will drive USIM_DET from low to high level, and the removal of it will drive USIM_DET from high to low level.

- When the (U)SIM is absent, CD is shorted to ground and USIM_DET is at low level.
- When the (U)SIM is present, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design for (U)SIM interface with a normally closed (U)SIM card connector.



NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

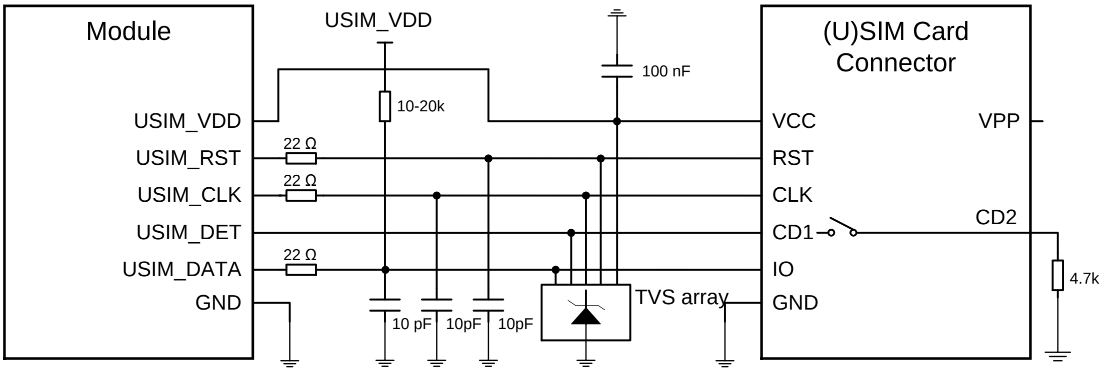
Figure 16: Reference Circuit for Normally Closed (U)SIM Card Connector

4.1.4. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, CD1 and CD2 of the connector are disconnected when there is no (U)SIM card inserted. (U)SIM card detection by low level is applicable to this type of connector. Once (U)SIM hot-plug is enabled by executing **AT+QSIMDET=1,0**, a (U)SIM card insertion will drive USIM_DET from high to low level, and the removal of it will drive USIM_DET from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high level.
- When the (U)SIM is present, CD1 is pull down to ground and USIM_DET is at low level.

The following figure shows a reference design for (U)SIM interface with a normally open (U)SIM card connector.

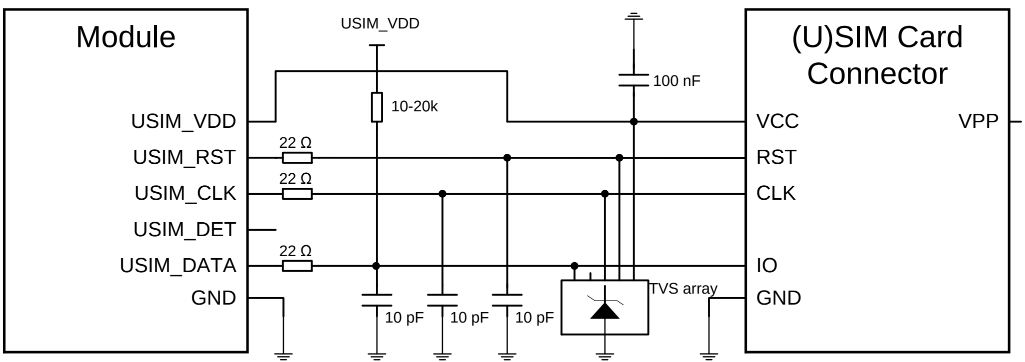


NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 17: Reference Circuit for Normally Open (U)SIM Card Connector

4.1.5. (U)SIM Card Connector Without Hot-Plug

If (U)SIM card hot-plug is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated by the following figure.



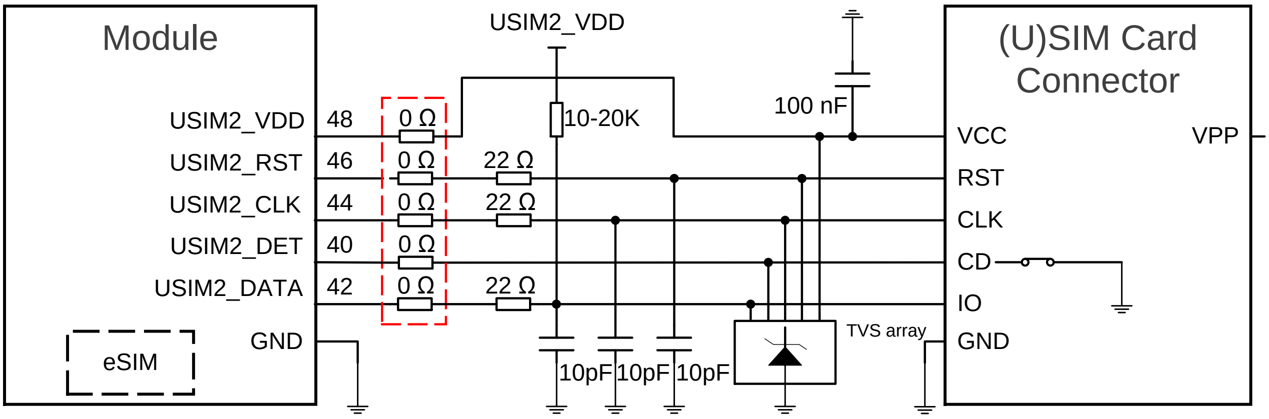
NOTE: All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

Figure 18: Reference Circuit for a 6-Pin (U)SIM Card Connector

4.1.6. (U)SIM2 Card Compatible Design

It should be noted that when the (U)SIM2 interface is used for an external (U)SIM card, the circuits are the same as those of (U)SIM1 interface. When the (U)SIM2 interface is used for the optional internal eSIM card, pins 40, 42, 44, 46 and 48 of the module must be kept open.

A recommended compatible design for the (U)SIM2 interface is shown below.



NOTE:
The five 0 Ω resistors must be placed close to the module, and all other components should be placed close to (U)SIM card connector in PCB layout.

Figure 19: Recommended Compatible Design for (U)SIM2 Interface

4.1.7. (U)SIM Design Notices

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible, (U)SIM card related resistance and capacitance and ESD protection devices should be placed close to the card connector. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VCC traces.
- Ensure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be not higher than 10 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to suppress EMI spurious transmission. The 10 pF capacitors are used to filter out RF interference.
- For USIM_DATA, it is optional to add a 10–20 kΩ pull-up resistor near the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1 Gen2 and USB 2.0 specifications and supports SuperSpeed (10 Gbps) on USB 3.1 and high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Table 16: Pin Definition of USB Interface

Pin No.	Pin Name	I/O	Description	Comment
7	USB_DP	AIO	USB differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
9	USB_DM	AIO	USB differential data (-)	
29	USB_SS_TX_M	AO	USB 3.1 super-speed transmit (-)	Require differential impedance of 90 Ω.
31	USB_SS_TX_P	AO	USB 3.1 super-speed transmit (+)	
35	USB_SS_RX_M	AI	USB 3.1 super-speed receive (-)	
37	USB_SS_RX_P	AI	USB 3.1 super-speed receive (+)	

For more details about the USB 3.1 Gen2 and 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit of USB interface.

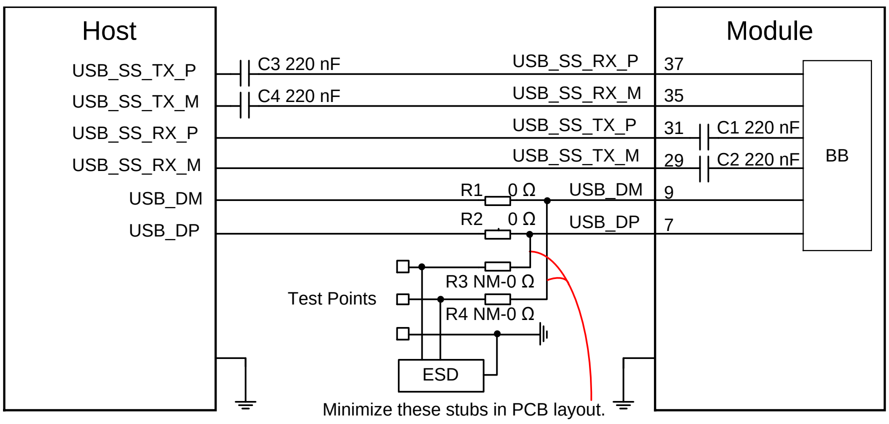


Figure 20: Reference Circuit of USB 3.1 & 2.0 Interface

AC coupling capacitors C3 and C4 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB. To ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

You should follow the principles below when designing for the USB interface to meet USB specifications.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of differential trace of USB 2.0 and USB 3.1 are 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 225 mm, and the intra-pair length matching (P/M) should be less than 2 mm. For USB 3.1, the intra-pair length matching (P/M) should be less than 0.7 mm, while the inter-pair length matching (Tx/Rx) should be less than 10 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on the same layer and with ground planes above and below.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so you should pay attention to the selection of the device. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.15 pF for USB 3.1.
- Keep the ESD protection components as close to the USB connector as possible.
- If possible, reserve 0 Ω resistors on USB_DP and USB_DM traces respectively.

Table 17: USB Trace Length Inside the Module

Signal	Pin No.	Length (mm)		Length Difference (mm)	
		RM520N-GL	RM520N-EU	RM520N-GL	RM520N-EU
USB_DP	7	19.44	18.29	0.02	0.05
USB_DM	9	19.42	18.34		
USB_SS_RX_P	37	11.97	11.94	0.14	0.07
USB_SS_RX_M	35	11.83	11.87		
USB_SS_TX_P	31	8.33	8.31	0.28	0.10
USB_SS_TX_M	29	8.05	8.21		

4.3. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface.

- *PCI Express Base Specification Revision 4.0* compliant
- Data rate up to 8 Gbps

4.3.1. PCIe Operating Mode

The module supports endpoint (EP) mode and root complex (RC) mode, and EP mode is the default. In EP mode, the module operates as a PCIe EP device, while in RC mode, as a PCIe root complex device.

AT+QCFG="pcie/mode" is used to set PCIe RC/EP mode.

AT+QCFG="pcie/mode" Set PCIe RC/EP Mode	
Write Command **AT+QCFG="pcie/mode"[,<mode>]**	Response If the optional parameter is omitted, query the current setting: **+QCFG: "pcie/mode",<mode>** **OK** If the optional parameter is specified, set PCIe RC/EP mode: **OK** If there is any error: **ERROR**
Maximum Response Time	300 ms
Characteristics	The command takes effect after the module is restarted. The configuration will be saved automatically.

Parameter

<mode>	Integer type. Set PCIe RC or EP mode. <u>0</u> PCIe EP mode. 1 PCIe RC mode.

NOTE

1. The underlined value is the default.
2. For more details about the command, see ***document [4]***.

4.3.2. Pin Definition of PCIe

The following table shows the pin definition of PCIe interface.

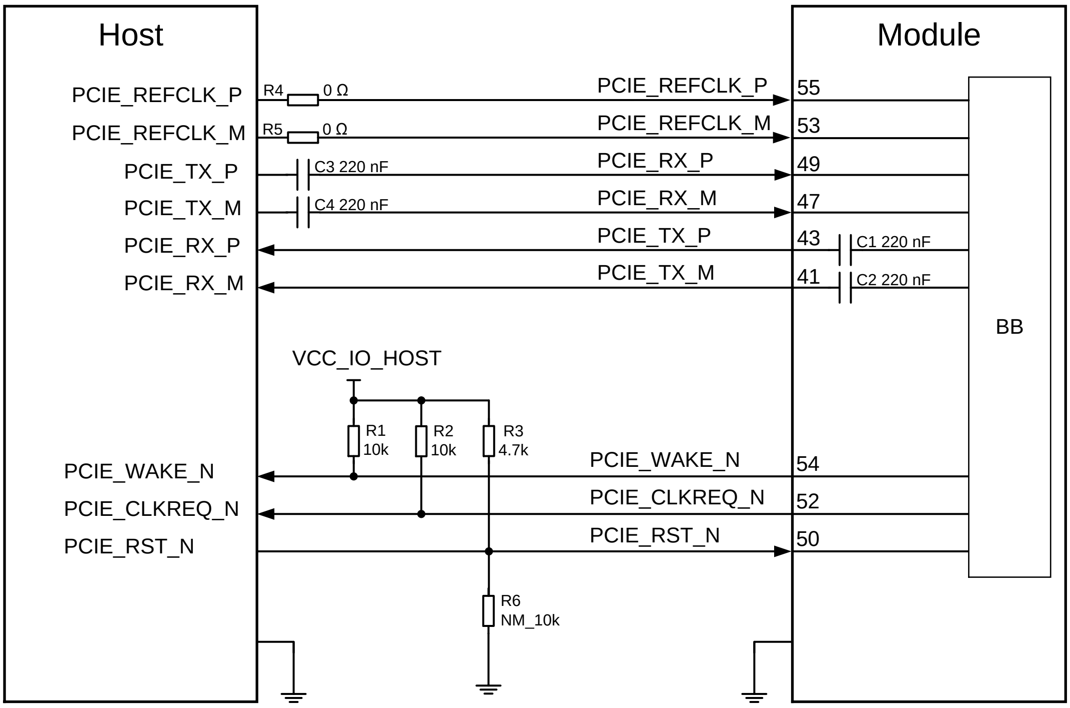
Table 18: Pin Definition of PCIe Interface

Pin No.	Pin Name	I/O	Description	Comment
55	PCIE_REFCLK_P	AIO	PCIe reference clock (+)	100 MHz. Require differential impedance of 85 Ω
53	PCIE_REFCLK_M	AIO	PCIe reference clock (-)	
49	PCIE_RX_P	AI	PCIe receive (+)	Require differential impedance of 85 Ω
47	PCIE_RX_M	AI	PCIe receive (-)	
43	PCIE_TX_P	AO	PCIe transmit (+)	Require differential impedance of 85 Ω
41	PCIE_TX_M	AO	PCIe transmit (-)	
50	PCIE_RST_N	DI [18]	PCIe reset Active LOW	1.8/3.3 V
52	PCIE_CLKREQ_N	OD [18]	PCIe clock request Active LOW	1.8/3.3 V
54	PCIE_WAKE_N	OD [18]	PCIe wake up Active LOW	1.8/3.3 V

[18] PCIE_RST_N behaves as DI in PCIe EP mode, and as OD in PCIe RC mode. PCIE_CLKREQ_N and PCIE_WAKE_N behave as OD in PCIe EP mode, and as DI in PCIe RC mode. PCIe EP mode is the default.

4.3.3. Reference Design for PCIe

The following figure shows a reference circuit for the PCIe interface.



NOTE: The voltage level VCC_IO_HOST of these three signals depend on the host side due to open drain.

Figure 21: PCIe Interface Reference Circuit

To ensure the signal integrity of PCIe interface, AC coupling capacitors C3 and C4 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on your schematic and PCB.

The following principles of PCIe interface design should be complied with to meet PCIe specification.

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, crystal, and oscillator signals.
- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length no more than 200 mm.
- Keep the intra-pair length matching of each differential data pair (P/M) less than 0.7 mm.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.
- It is recommended to use a push-pull GPIO to output a low level that approaches to 0 V rather than using a pull-down resistor to get a low level. Otherwise, voltage division may be formed with the pull-up resistor inside the module, resulting in an uncertain 0 V voltage that could further lead to unpredictable problems.

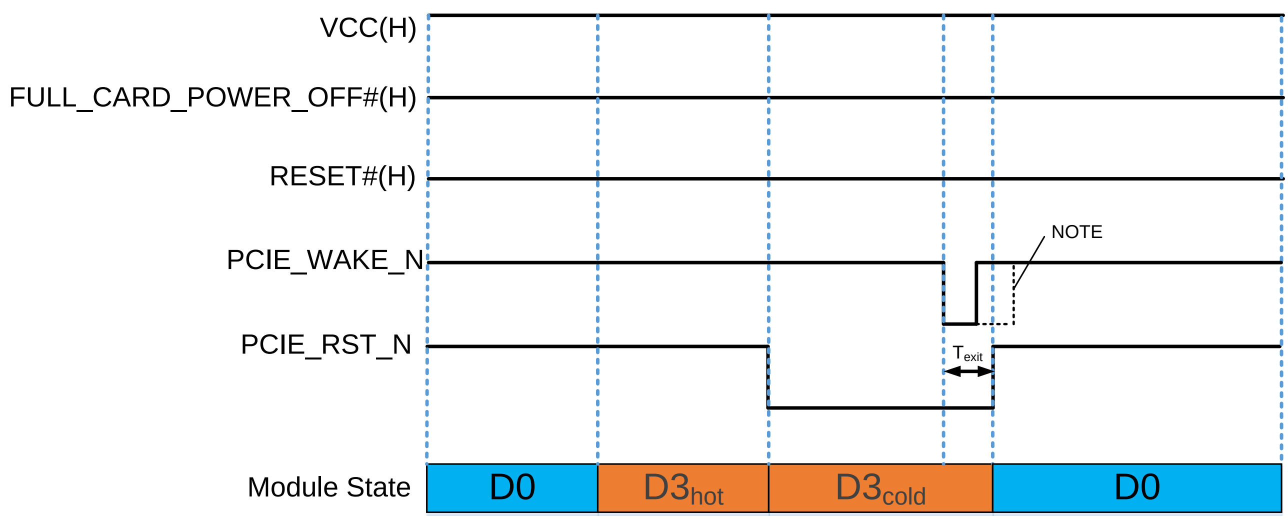
Table 19: PCIe Trace Length Inside the Module

Signal	Pin No.	Length (mm)		Length Difference (mm)	
		RM520N-GL	RM520N-EU	RM520N-GL	RM520N-EU
PCIE_REFCLK_P	55	12.06	12.83	0.03	0.12
PCIE_REFCLK_M	53	12.03	12.71		
PCIE_TX_P	43	5.10	7.48	0.15	0.10
PCIE_TX_M	41	4.95	7.38		
PCIE_RX_P	49	12.02	12.34	0.04	0.05
PCIE_RX_M	47	11.98	12.39		

4.3.4. PCIe $D3_{cold}$ State

For the laptop application scenario, module must go through $D3_{hot}$ before entering $D3_{cold}$. In $D3_{hot}$ state, PCIE_RST_N must be kept in high level.

The module enters $D3_{cold}$ state after PCIE_RST_N is asserted. The module enters D0 state after PCIE_RST_N is de-asserted



NOTE: PCIE_WAKE_N may be pulled up before or after PCIE_RST_N is pulled up, depending on when HOST pulls up PCIE_RST_N. This time does not affect the normal operation of the module and can be ignored.

Figure 22: PCIe $D3_{Cold}$ State Timing

Table 20: EXIT $D3_{cold}$ State Timing of the Module

Symbol	Min.	Typ.	Max.	Comment
T_{exit}	50 ms	150 ms	500 ms	The period from the module pulling down PCIE_WAKE_N to HOST pulling up PCIE_RST_N.

4.4. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

Table 21: Pin Definition of Control and Indication Interfaces

Pin No.	Pin Name	I/O	Description	DC Characteristics	Comment
8	W_DISABLE1#	DI	Airplane mode control Active LOW	1.8/3.3 V	Internally pulled up to 1.8 V with a 100 kΩ resistor.
26	W_DISABLE2#	DI	GNSS control Active LOW	1.8/3.3 V	
10	LED_WWAN#	OD	RF status LED indicator Active LOW	VCC	-
23	WAKE_ON_WAN#	OD	Wake up the host Active LOW	1.8/3.3 V	-
25	DPR	DI	Dynamic power reduction	1.8 V	-

4.4.1. W_DISABLE1#

The module provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. W_DISABLE1# is pulled up by default. Driving it LOW will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through AT commands. The following table shows the AT command and corresponding RF function status of the module.

Table 22: RF Function Status

W_DISABLE1# Logic Level	AT Command	RF Function Status	Operating Mode
HIGH	**AT+CFUN=1**	Enabled	Full functionality mode
	AT+CFUN=0	Disabled	Minimum functionality mode
	AT+CFUN=4		Airplane mode
LOW	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

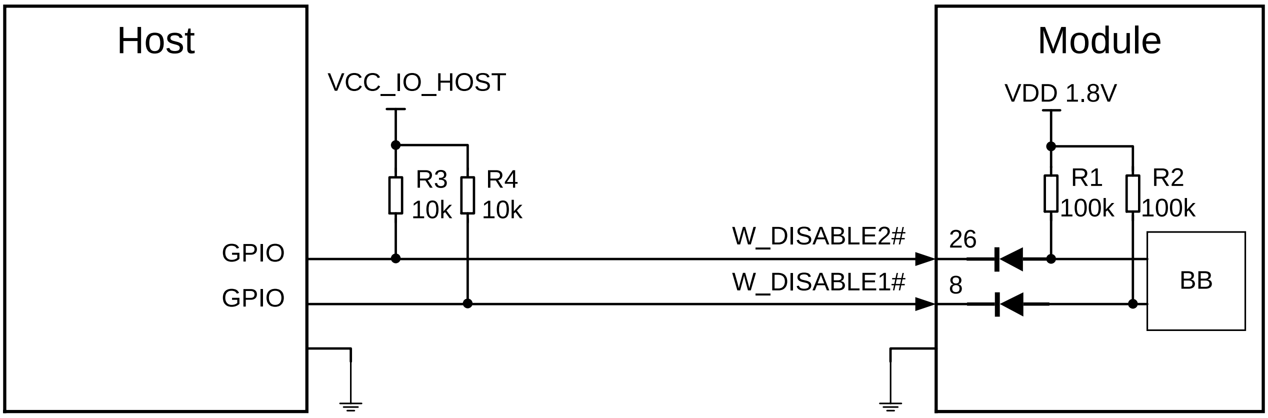
4.4.2. W_DISABLE2#

The module provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it LOW will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function. For details about the AT commands, see ***document [5]***

Table 23: GNSS Function Status

W_DISABLE2# Logic Level	AT Commands	GNSS Function Status
HIGH	**AT+QGPS=1**	Enabled
HIGH	**AT+QGPSEND**	Disabled
LOW	**AT+QGPS=1**	Disabled
LOW	**AT+QGPSEND**	

A simple voltage level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# which are pulled up to a 1.8 V voltage in the module, as shown in the following figure. Therefore, the control signals (GPIO) of the host device could be at 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active LOW signals, and a reference circuit is shown as below.



NOTE: The voltage level of VCC_IO_HOST could be 1.8 V or 3.3 V typically.

Figure 23: W_DISABLE1# and W_DISABLE2# Reference Circuit

4.4.3. LED_WWAN#

LED_WWAN# is used to indicate the RF status of the module, and its sink current is up to 10 mA.

To reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the LED_WWAN# signal is at low level.

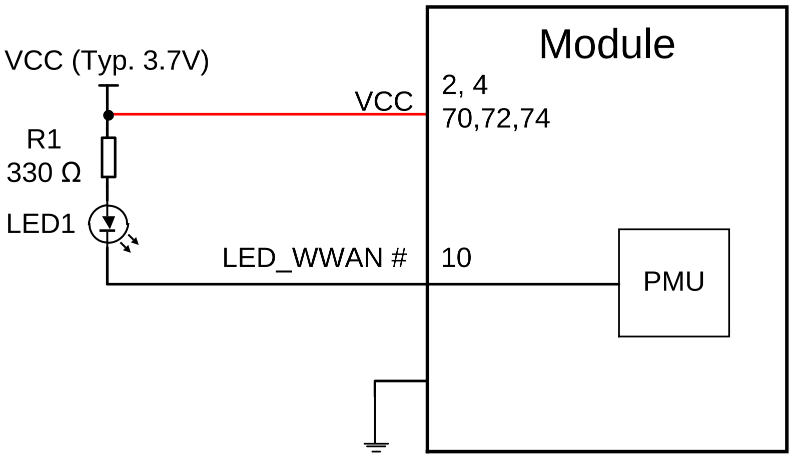


Figure 24: LED_WWAN# Reference Circuit

Table 24: Network Status Indications of LED_WWAN#

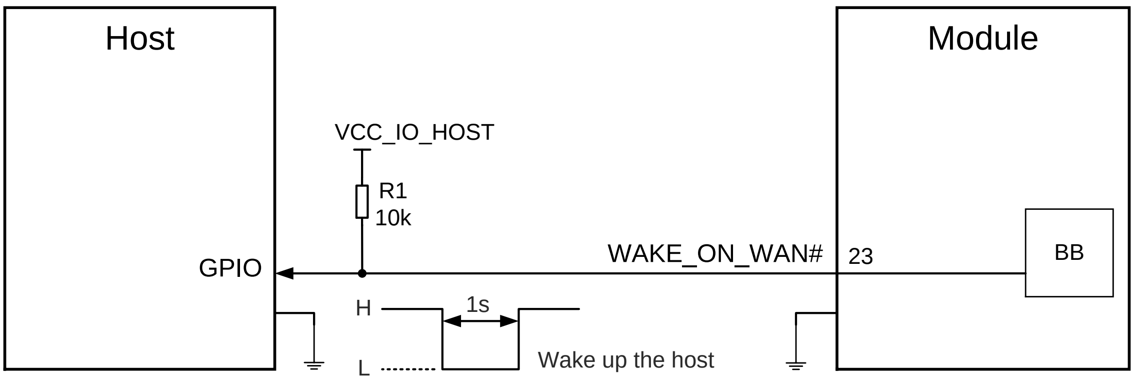
LED_WWAN# Logic Level	Description
LOW (LED on)	RF function is turned on
HIGH (LED off)	RF function is turned off if any of the following occurs: ● The (U)SIM card is not powered. ● W_DISABLE1# is at low level (airplane mode enabled). ● **AT+CFUN=4** (RF function disabled).

4.4.4. WAKE_ON_WAN#

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a one-second low level pulse signal will be outputted to wake up the host.

Table 25: State of the WAKE_ON_WAN#

WAKE_ON_WAN# State	Module Operation Status
Outputs a one-second pulse signal at low level	Call/SMS/Data is incoming (to wake up the host)
Always at high level	Idle/Sleep



NOTE:
The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

Figure 25: WAKE_ON_WAN# Signal Reference Circuit

4.4.5. DPR

The module provides the DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from the proximity sensor of the host system to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 26: Function of the DPR Signal

DPR Level	Function
HIGH/Floating	NO maximum transmitting power backoff
LOW	Maximum transmitting power backoff by **AT+QSAR**

NOTE

See ***document [6]*** for more details about **AT+QSAR**.

4.5. Cellular/WLAN COEX Interface

The module provides the cellular/WLAN COEX interface, the following table shows the pin definition of this interface.

Table 27: Pin Definition of COEX Interface

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Description</th><th>DC Characteristics</th></tr>
<tr><td rowspan="2">60 [19]</td><td>N79_TX_EN*</td><td>DO</td><td>Notification from SDR to WLAN when n79 transmitting</td><td>1.8 V</td></tr>
<tr><td>NC</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td rowspan="2">38 [20]</td><td>WLAN_TX_EN*</td><td>DI</td><td>Notification from WLAN to SDR when WLAN transmitting</td><td>1.8 V</td></tr>
<tr><td>NC</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>62</td><td>COEX_RXD [21]</td><td>DI</td><td>5G/LTE and WLAN coexistence</td><td>1.8 V</td></tr>
</table>

[19] Pin 38 is defined as WLAN_TX_EN for RM520N-GL, while as NC for RM520N-EU.
[20] Pin 60 is defined as N79_TX_EN for RM520N-GL, while as NC for RM520N-EU.
[21] Please note that COEX_RXD and COEX_TXD cannot be used as general UART ports.

			receive	
64	COEX_TXD [21]	DO	5G/LTE and WLAN coexistence transmit	1.8 V

4.6. Antenna Tuner Control Interface

RFFE interface are used for antenna tuner control and should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

Table 28: Pin Definition of Antenna Tuner Control Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
56	RFFE_CLK*	DO	Used for external MIPI IC control	1.8 V
58	RFFE_DATA*	DIO		1.8 V
24	VDDIO_1V8	PO	Provide 1.8 V for external circuit	1.8 V Max. output current: 50 mA

NOTE

If RFFE function is required, please contact Quectel for more details.

4.7. Configuration Pins

The module provides four configuration pins, which are defined as below.

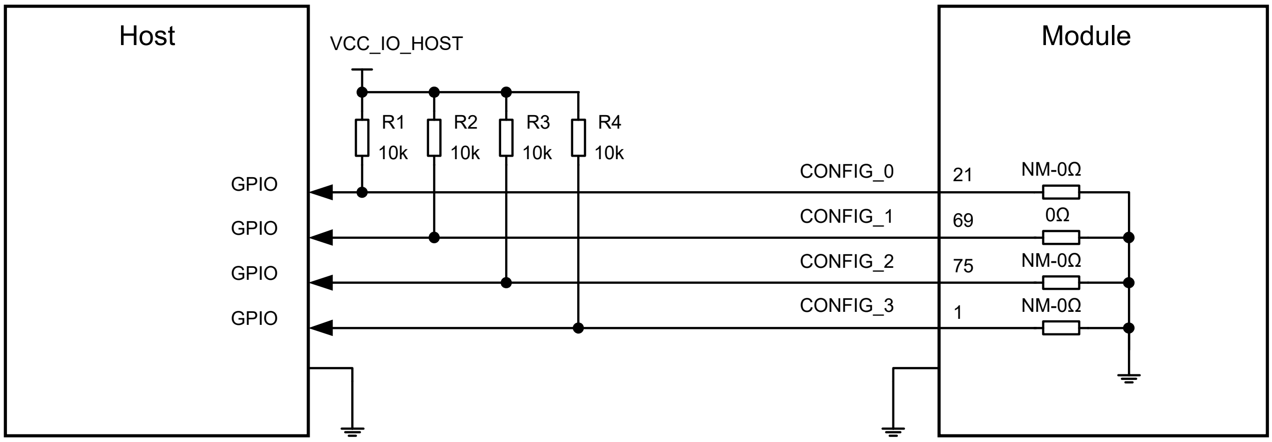
Table 29: Configuration Pins List of M.2 Specification

CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN-PCIe, USB 3.1	2 (Quectel defined)

Table 30: Configuration Pins of the Module

Pin No.	Pin Name	I/O	Description
21	CONFIG_0	DO	Not connected internally
69	CONFIG_1	DO	Connected to GND internally
75	CONFIG_2	DO	Not connected internally
1	CONFIG_3	DO	Not connected internally

The following figure shows a reference circuit of these four pins.



NOTE: The voltage level of VCC_IO_HOST depends on the host side and could be 1.8 V or 3.3 V.

Figure 26: Recommended Circuit for Configuration Pins

4.8. PCM Interface

RM520N-EU module supports audio communication via Pulse Code Modulation (PCM) digital interface.

Table 31: Pin Definition of PCM Interface

Pin No.	Pin Name	I/O	Description	DC Characteristics
20	PCM_CLK	DIO	PCM clock	1.8 V
22	PCM_DIN	DI	PCM data input	1.8 V

24	PCM_DOUT	DO	PCM data output	1.8 V
28	PCM_SYNC	DIO	PCM data frame sync	1.8 V

The PCM interface supports the following modes:

- Short frame mode: the module works as both the slave and the master device
- Long frame mode: the module works as the master device only

The module supports 16-bit linear encoding format. The following figures are the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz) and the long frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 256 kHz).

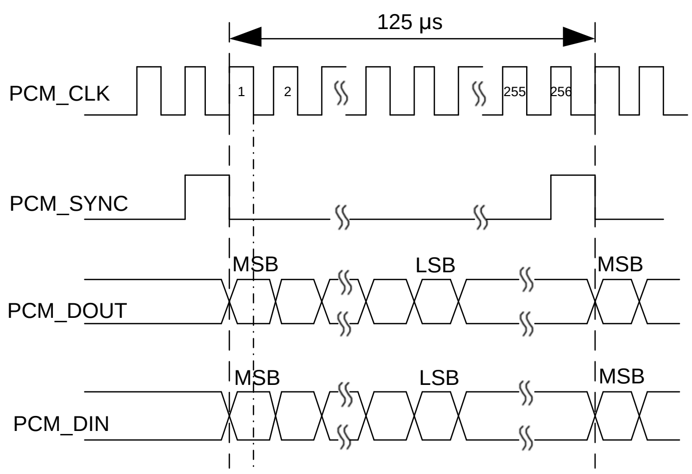


Figure 27: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM_SYNC operates at 16 kHz.

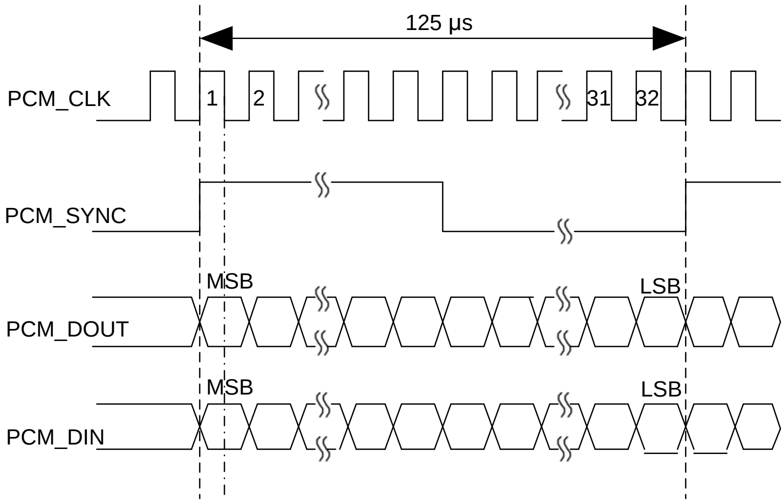


Figure 28: Timing of Long Frame Mode

In long frame mode, data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. But in this mode, the PCM_SYNC rising edge represents the MSB. PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC reaches 8 kHz with a 50 % duty cycle.

5 RF Characteristics

This chapter mainly describes RF characteristics of the module.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Antenna Interfaces

5.1.1. Pin Definition

The pin definition of antenna interfaces is shown below.

Table 32: RM520N-GL Pin Definition of Antenna Interfaces

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Comment</th></tr>
<tr><td>ANT0</td><td>AIO</td><td>Antenna 0 interface:
5G NR:
- Refarmed: LB TX0 /PRX & MHB TX0 /PRX & UHB TX1/DRX
- n41 TX0/PRX
- n77/n78/n79 TX1/DRX
LTE: LB TX0/PRX & MHB TX0/PRX & UHB TX1/DRX
WCDMA: LMB TRX</td><td rowspan="2">LB: 617–960 MHz
MHB: 1452–2690 MHz
UHB: 3400–3800 MHz
n77/n78: 3300–4200 MHz
n79: 4400–5000 MHz
LAA: 5150-5925 MHz</td></tr>
<tr><td>ANT1</td><td>AIO</td><td>Antenna 1 interface:
5G NR:
- Refarmed: MHB PRX MIMO & UHB PRX MIMO
- n41 PRX MIMO
- n77/n78/n79 PRX MIMO
LTE: MHB PRX MIMO & UHB PRX MIMO & LAA PRX
GNSS: L5</td></tr>
</table>

ANT2	AIO	Antenna 2 interface: **5G NR:** - Refarmed: MHB TX1 [22]/ DRX MIMO & UHB TX0/PRX - n41 TX1/DRX MIMO - n77/n78/n79 TX0/PRX **LTE:** MHB TX1 [22]/DRX MIMO & UHB TX0/PRX	
ANT3	AIO	Antenna 3 interface: **5G NR:** - Refarmed: LB TX1 [23] / DRX & MHB DRX & UHB DRX MIMO - n41 DRX - n77/n78/n79 DRX MIMO **LTE:** LB TX1 [24]/DRX & MHB DRX & UHB DRX MIMO & LAA DRX **WCDMA:** LMB DRX **GNSS:** L1	

Table 33: RM520N-EU Pin Definition of Antenna Interfaces

Pin Name	I/O	Description	Comment
ANT0	AIO	Antenna 0 interface: **5G NR:** - Refarmed: MLB TX0 /PRX & HB TX1 /DRX - n41 TX1/DRX - n77/n78 TX0/PRX **LTE:** MLB TX0/PRX & HB TX1/DRX & UHB TX0/PRX **WCDMA:** MLB TRX	LB: 617–960 MHz MHB: 1452–2690 MHz UHB: 3400–3800 MHz n77/n78: 3300–4200 MHz
ANT1	AIO	Antenna 1 interface: **5G NR:** - Refarmed: MB PRX MIMO & HB DRX MIMO - n41 DRX MIMO - n75/n76 PRX - n77/n78 PRX MIMO **LTE:** MB PRX MIMO & HB DRX MIMO & UHB PRX MIMO &B32 PRX	
ANT2	AIO	Antenna 2 interface: **5G NR:**	

[22] MHB TX1 will be active when supporting Sub 2.6 GHz EN-DC.
[23] LB TX1 n20 will be active when supporting DC_B28_n20.
[24] LB TX1 B20 will be active when supporting DC_B20_n28.

		- Refarmed: MB TX1/ DRX & HB TX0/ PRX & UHB TX0/PRX - n41 TX0/PRX - n77/n78 TX1/DRX **LTE:** MB TX1/DRX & HB TX0/PRX & UHB TX1/DRX **WCDMA:** MB DRX	
ANT3	AIO	Antenna 3 interface: **5G NR:** - Refarmed: LB TX1 / DRX & MB DRX MIMO & HB PRX MIMO - n41 PRX MIMO - n75/n76 DRX - n77/n78 DRX MIMO **LTE:** LB DRX & MB DRX MIMO & HB PRX MIMO & UHB DRX MIMO & B32 DRX **WCDMA:** LB DRX **GNSS:** L1 (optional)	
ANT4	AI	**GNSS:** L1 & L5	GNSS L1: 1559–1609 MHz GNSS L5: 1166–1187 MHz

NOTE

RM520N-EU supports 5 antennas (ANT0, ANT1, ANT2, ANT3 and ANT4). ANT4 supports GNSS function by default. You may also choose ANT3 to support GNSS L1 function according to actual needs. For details, please contact Quectel Technical Support.

5.1.2. Cellular Network

5.1.2.1. Rx Sensitivity

Table 34: RM520N-GL Conducted Receiving Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [25]	3GPP (SIMO)
WCDMA	WCDMA B1	-109.1	-110	-112	-106.7
	WCDMA B2	-109.5	-109.8	-112.5	-104.7

[25] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which improves Rx performance.

	WCDMA B4	-110.0	-109.8	-113	-106.7
	WCDMA B5	-111.4	-113.4	-114	-104.7
	WCDMA B8	-112.0	-113.8	-115	-103.7
	WCDMA B19	-112.4	-113.4	-115.5	-104.7
LTE	LTE-FDD B1 (10 MHz)	-97.3	-97.8	-101.7	-96.3
	LTE-FDD B2 (10 MHz)	-97.8	-97.7	-101.8	-94.3
	LTE-FDD B3 (10 MHz)	-97.6	-97.3	-102.2	-93.3
	LTE-FDD B4 (10 MHz)	-98.2	-97.8	-102.1	-96.3
	LTE-FDD B5 (10 MHz)	-100.3	-101.7	-103.6	-94.3
	LTE-FDD B7 (10 MHz)	-97.1	-97.2	-101.1	-94.3
	LTE-FDD B8 (10 MHz)	-99.7	-101.8	-102.5	-93.3
	LTE-FDD B12(B17) (10 MHz)	-100.8	-102.1	-104.5	-93.3
	LTE-FDD B13 (10 MHz)	-98.7	-100.8	-102.4	-93.3
	LTE-FDD B14 (10 MHz)	-99.5	-99.4	-102.5	-93.3
	LTE-FDD B18 (10 MHz)	-100.3	-101.6	-103.8	-96.3
	LTE-FDD B19 (10 MHz)	-100.3	-99.7	-103.3	-96.3
	LTE-FDD B20 (10 MHz)	-100.5	-102.2	-104.4	-93.3
	LTE-FDD B25 (10 MHz)	-97.7	-97.5	-100.5	-92.8
	LTE-FDD B26 (10 MHz)	-100.3	-101.8	-104.1	-93.8
	LTE-FDD B28 (10 MHz)	-99.7	-99.9	-102.8	-94.8
	LTE-FDD B29 (10 MHz)	-98.2	-99.5	-101.5	TBD
	LTE-FDD B30 (10 MHz)	-97.3	-97.4	-101.2	-95.3
	LTE-FDD B32 (10 MHz)	-97.3	-98.4	-100.1	-95.3
	LTE-TDD B34 (10 MHz)	-97.8	-98.1	-101.0	-96.3
	LTE-TDD B38 (10 MHz)	-95.7	-96.6	-99.6	-96.3

	LTE-TDD B39 (10 MHz)	-98.7	-98.1	-100.6	-96.3
	LTE-TDD B40 (10 MHz)	-96.9	-96.7	-101.3	-96.3
	LTE-TDD B41 (10 MHz)	-95.7	-96.5	-100.3	-94.3
	LTE-TDD B42 (10 MHz)	-96.8	-97.7	-101.5	-95
	LTE-TDD B43 (10 MHz)	-97.1	-97.5	-102.6	-95
	LTE-TDD B46 (10 MHz)	-96.2	-96.5	-99.3	TBD
	LTE-TDD B48 (10 MHz)	-96.9	-97.6	-101.9	-95
	LTE-FDD B66 (10 MHz)	-98.0	-97.7	-101.4	-96.5
	LTE-FDD B71 (10 MHz)	-99.9	-100.7	-102.0	-94.2
5G NR	5G NR-FDD n1 (20 MHz)	-94.3	-95.1	-97.5	-94.0
	5G NR-FDD n2 (20 MHz)	-94.3	-94.7	-97.3	-92.0
	5G NR-FDD n3 (20 MHz)	-94.5	-94.2	-97.2	-91.0
	5G NR-FDD n5 (20 MHz)	-95.5	-97.6	-100.0	-91
	5G NR-FDD n7 (20 MHz)	-94.5	-94.2	-96.2	-92.0
	5G NR-FDD n8 (20 MHz)	-96.2	-97.7	-99.2	-90.0
	5G NR-FDD n12 (15 MHz)	-96.7	-99.4	-100.7	-84.0
	5G NR-FDD n13 (10MHz)	-97.6	-99.0	-101.0	-93.8
	5G NR-FDD n14 (10 MHz)	-98.7	-98.4	-101.4	-93.8
	5G NR-FDD n18 (15 MHz)	-98.0	-99.0	-101.5	-95.0
	5G NR-FDD n20 (20 MHz)	-96.9	-98.9	-100.6	-90.0
	5G NR-FDD n25 (20 MHz)	-94.6	-95.3	-99.1	-90.5
	5G NR-FDD n26 (20 MHz)	-95.0	-97.7	-100.1	-87.6
	5G NR-FDD n28 (20 MHz)	-96	-95.9	-98.3	-91.0
	5G NR-FDD n29 (10 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n30 (10 MHz)	-95.4	-97.0	-98.8	-95.8

	5G NR-TDD n38 (20 MHz)	-93.4	-94.0	-96.7	-94.0
	5G NR-TDD n40 (20 MHz)	-93.8	-94.8	-97.3	-94.0
	5G NR-TDD n41 (100 MHz)	-85.8	-86.8	-91.3	-84.7
	5G NR-FDD n48 (20 MHz)	-96.6	-96.6	-99.5	-93.0
	5G NR-FDD n66 (40 MHz)	-92.3	-93.0	-94.3	-90.1
	5G NR-FDD n70 (20 MHz)	-94.5	-95.1	-97.7	-93.8
	5G NR-FDD n71 (20 MHz)	-96.5	-96.0	-99.1	-86.0
	5G NR-FDD n75 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR-FDD n76 (5 MHz)	TBD	TBD	TBD	TBD
	5G NR-TDD n77 (100 MHz)	-87.4	-88.6	-92.0	-85.1
	5G NR-TDD n78 (100 MHz)	-87.7	-88.9	-92.1	-85.6
	5G NR-TDD n79 (100 MHz)	-87.2	-88.1	-92.5	-85.6

Table 35: RM520N-EU Conducted Receiving Sensitivity (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [25]	3GPP (SIMO)
WCDMA	WCDMA B1	-109	-109.5	-112	-106.7
	WCDMA B5	-109.5	-110	-112.3	-104.7
	WCDMA B8	-109.5	-110	-112.6	-103.7
LTE	LTE-FDD B1 (10 MHz)	-97.22	-97	-99.5	-96.3
	LTE-FDD B3 (10 MHz)	-98.1	-97.8	-100.2	-93.3
	LTE-FDD B5 (10 MHz)	-98.4	-99	-102	-94.3
	LTE-FDD B7 (10 MHz)	-95.5	-95.5	-97.5	-94.3
	LTE-FDD B8 (10 MHz)	-98.5	-99	-101.8	-93.3
	LTE-FDD B20 (10 MHz)	-98.4	-99	-101.8	-93.3
	LTE-FDD B28 (10 MHz)	-98.32	-99.3	-102	-94.8

	LTE-FDD B32 (10 MHz)	-97.5	-96.5	-99	-95.3
	LTE-TDD B38 (10 MHz)	-96	-95.3	-97.6	-96.3
	LTE-TDD B40 (10 MHz)	-95	-95	-97.2	-96.3
	LTE-TDD B41 (10 MHz)	-95.5	-94.5	-97	-94.3
	LTE-TDD B42 (10 MHz)	-97.5	-97.3	-99.62	-95
	LTE-TDD B43 (10 MHz)	-97.5	-97.3	-100	-95
	LTE-FDD B71 (10 MHz)	-99	-99.5	-102.2	-94.2
5G NR	5G NR-FDD n1 (20 MHz)	-94.1	-94.4	-96.9	-94.0
	5G NR-FDD n3 (20 MHz)	-95.3	-95	-97.9	-91.0
	5G NR-FDD n5 (20 MHz)	-93.5	-95.5	-97.4	-91
	5G NR-FDD n7 (20 MHz)	-92.8	-92.8	-95.4	-92.0
	5G NR-FDD n8 (20 MHz)	-93.7	-95.3	-97.2	-90.0
	5G NR-FDD n20 (20 MHz)	-93.2	-95.4	-97.2	-90.0
	5G NR-FDD n28 (20 MHz)	-94.8	-95.3	-97.7	-91.0
	5G NR-TDD n38 (20 MHz)	-93.5	-92.8	-96.1	-94.0
	5G NR-TDD n40 (20 MHz)	-93.3	-92.8	-95.7	-94.0
	5G NR-TDD n41 (100 MHz)	-86.2	-85.9	-88.8	-84.7
	5G NR-FDD n71 (20 MHz)	-96	-96.1	-98.5	-86.0
	5G NR-FDD n75 (20 MHz)	-95.4	-95.4	-97	-94
	5G NR-FDD n76 (5 MHz)	-100	-100	-102	-100
	5G NR-TDD n77 (100 MHz)	-88.4	-87.1	-90.7	-85.1
	5G NR-TDD n78 (100 MHz)	-88.4	-87.1	-90.8	-85.6

5.1.2.2. Tx Power

The following table shows the RF output power of the module.

Table 36: RM520N-GL Cellular Output Power

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE HPUE bands (B38/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [26]
	5G NR HPUE bands (n38/n40/n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm [26]

Table 37: RM520N-EU Cellular Output Power

Mode	Frequency	Max.	Min.
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
	LTE HPUE bands (B38/B41/B42/B43)	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [26]
	5G NR HPUE bands (n38/n41/n77/n78)	26 dBm +2/-3 dB (Class 2)	< -40 dBm [26]

[26] For 5G NR TDD bands, the normative reference for this requirement is *TS 38.101-1 clause 6.3.1.*

5.1.3. GNSS

The module includes a fully integrated global navigation satellite system solution (GPS, GLONASS, BDS, Galileo and QZSS).

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine is switched off by default. It has to be switched on via AT command.

5.1.3.1. GNSS Frequency

Table 38: GNSS Frequency

Bands	Type	Frequency	Unit
L1	GPS/Galileo/QZSS	1575.42 ±1.023 (L1)	MHz
	Galileo	1575.42 ±2.046 (E1)	MHz
	QZSS	1575.42 (L1)	MHz
	GLONASS	1597.5–1605.8	MHz
	BDS	1561.098 ±2.046	MHz
L5	GPS/Galileo/QZSS	1176.45 ±10.23 (GPS L5)	MHz

5.1.3.2. GNSS Performance

The following table shows GNSS performance of the module.

Table 39: GNSS Performance

Parameter	Description	Conditions	RM520N-GL	RM520N-EU	Unit
Sensitivity	Acquisition	Autonomous	-147	TBD	dBm
	Reacquisition	Autonomous	-160	TBD	dBm
	Tracking	Autonomous	-160	TBD	dBm

TTFF	Cold start @ open sky	Autonomous	27.93	TBD	s
		XTRA enabled	19.25	TBD	s
	Warm start @ open sky	Autonomous	11.55	TBD	s
		XTRA enabled	0.94	TBD	s
	Hot start @ open sky	Autonomous	1.09	TBD	s
		XTRA enabled	0.79	TBD	s
Accuracy	CEP-50	Autonomous @ open sky	1.35	TBD	m

NOTE

1. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).

5.2. Antenna Connectors

5.2.1. Antenna Connector Specifications

The module is mounted with standard 2 mm × 2 mm receptacle antenna connectors for convenient antenna connection. The antenna connector's PN is IPEX 20579-001E, and the connector dimensions are illustrated as below:

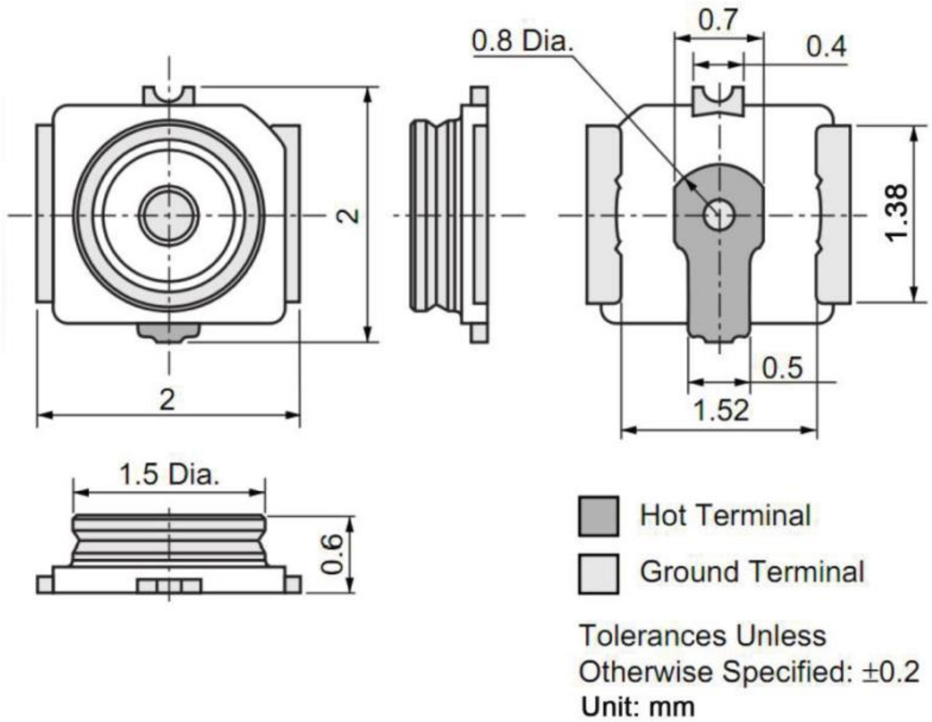


Figure 29: Dimensions of the Receptacle (Unit: mm)

Table 40: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max 1.3 (DC–3 GHz) Max 1.4 (3–6 GHz)

5.2.2. Antenna Connector Location

RM520N-GL has four antenna connectors: ANT0, ANT1, ANT2 and ANT3, which are shown as below.

Figure 30: RM520N-GL Antenna Connectors

RM520N-EU has five antenna connectors: ANT0, ANT1, ANT2, ANT3 and ANT4, which are shown as below.

Figure 31: RM520N-EU Antenna Connectors

5.2.3. Antenna Connector Installation

The receptacle RF connector used in conjunction with the module will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø 0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø 1.13 mm coaxial cable.

The following figure shows the specifications of mated plugs using Ø 0.81 mm coaxial cables.

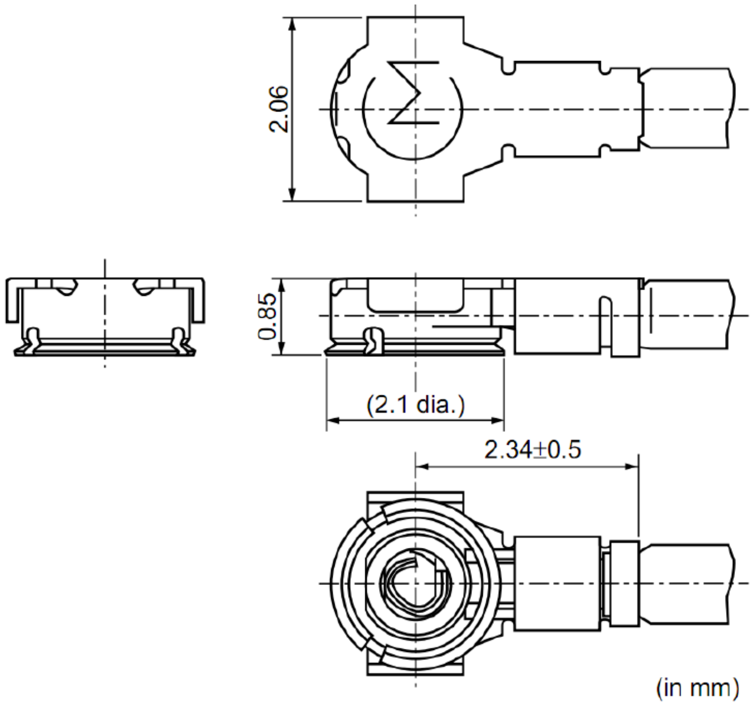


Figure 32: Dimensions of Mated Plugs (Ø0.81/Ø1.13 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle RF connector on the module and the mated plug using a Ø 0.81 mm coaxial cable.

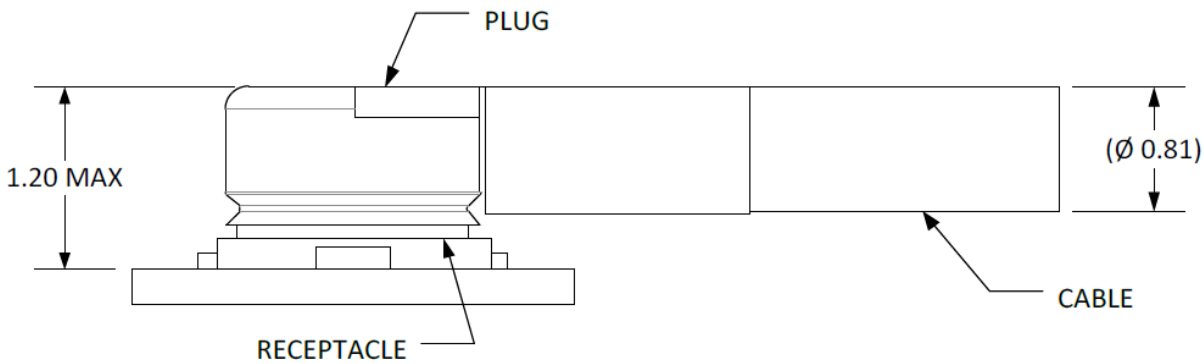


Figure 33: Space Factor of Mated Connectors (Ø0.81 mm Coaxial Cables) (Unit: mm)

The following figure illustrates the connection between the receptacle RF connector on the module and the mated plug using a Ø 1.13 mm coaxial cable.

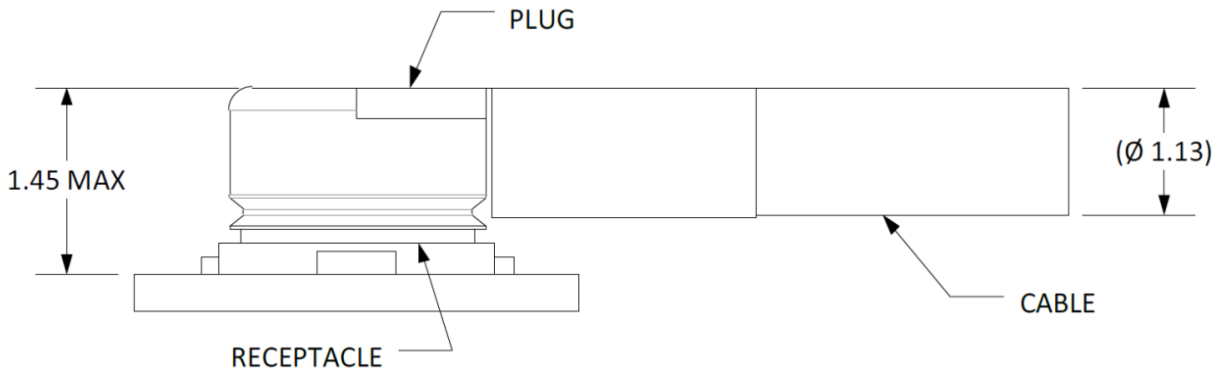


Figure 34: Space Factor of Mated Connectors (Ø 1.13 mm Coaxial Cables) (Unit: mm)

5.2.4. Recommended RF Connector Installation

5.2.4.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

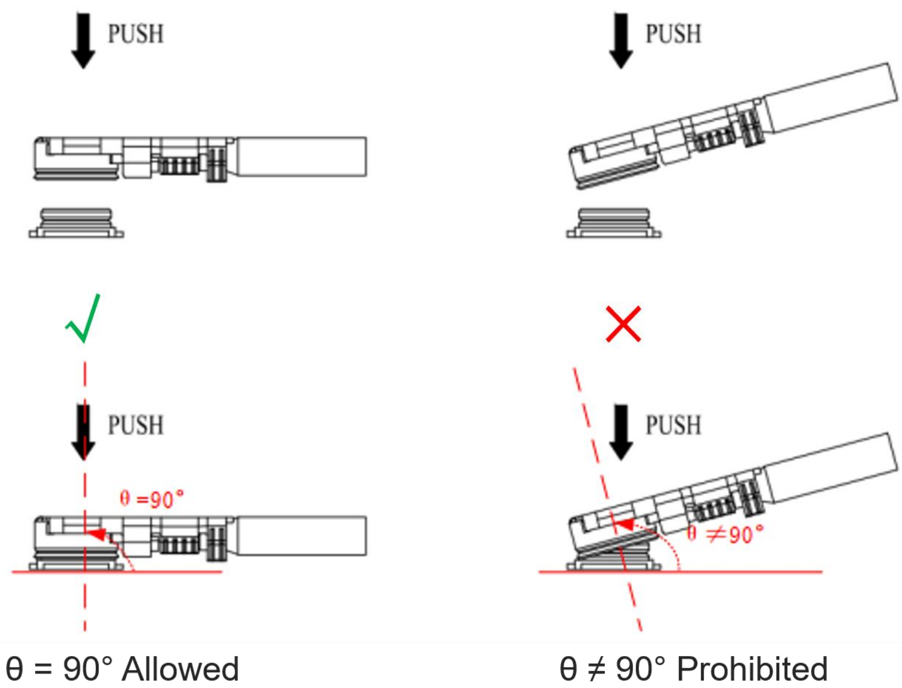


Figure 35: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

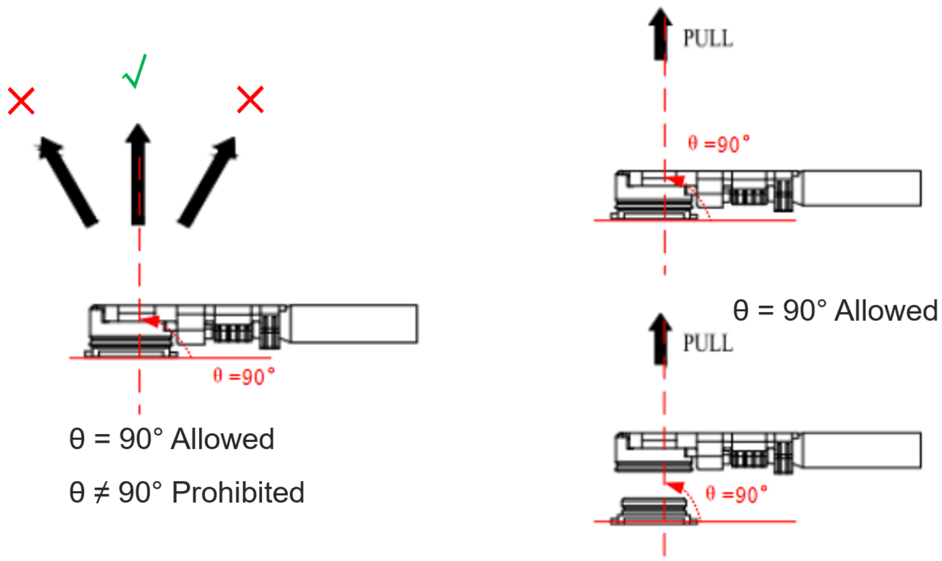


Figure 36: Pull out a Coaxial Cable Plug

5.2.4.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

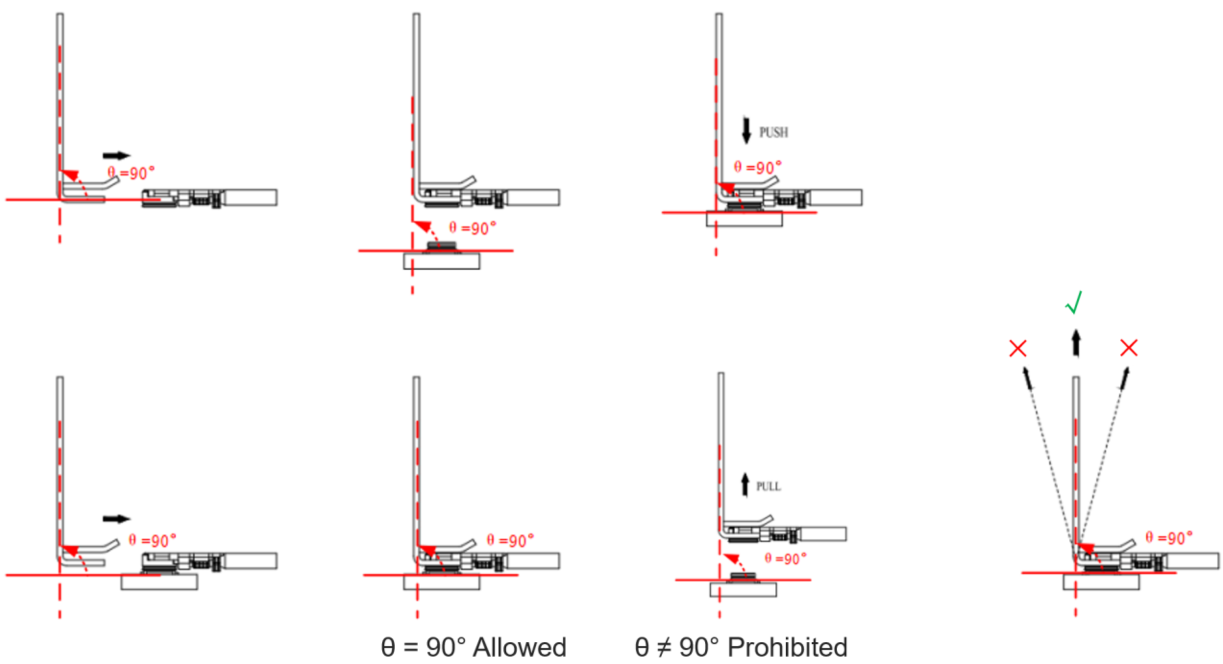


Figure 37: Install the Coaxial Cable Plug with Jig

5.2.5. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

5.3. Antenna Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antennas.

Table 41: Antenna Requirements

Type	Requirements
WCDMA/LTE/5G NR	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Input Impedance: 50 Ω ● Cable insertion loss: - < 1 dB: LB (<1 GHz) - < 1.5 dB: MB (1–2.3 GHz) - < 2 dB: HB (> 2.3 GHz)
GNSS	● Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.) ● Passive antenna gain: > 0 dBi

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6 Electrical Characteristics and Reliability

6.1. Power Supply Requirements

The typical input voltage of the module is 3.7 V, the following table shows the power supply requirements of the module.

Table 42: Power Supply Requirements

Parameter	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	3.135	3.7	4.4	V
Voltage Ripple	-	-	30	100	mV

6.2. Power Consumption

Table 43: Averaged Current Consumption for RM520N-GL

Mode	Conditions	Band/Combinations	Typ.	Unit
Power-off	Power off	-	195	μA
RF Disabled	**AT+CFUN=0** (USB 3.1 suspend)	-	4.6	mA
	AT+CFUN=4 (USB 3.1 suspend)	-	4.7	mA
Sleep State	SA FDD PF = 64 (USB 3.1 suspend)	-	9.7	mA
	SA TDD PF = 64 (USB 3.1 suspend)	-	9.4	mA

Idle State	SA PF = 64 (USB 2.0 active)	-	40	mA
	SA PF = 64 (USB 3.1 active)	-	60	mA
LTE	LTE LB @ 24 dBm	B5	520	mA
	LTE MB @ 24 dBm	B1	1080	mA
	LTE HB @ 24 dBm	B7	970	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	1512	mA
	UL 1CA, 256QAM			
	Tx power @ 24 dBm			
5G SA (1 Tx)	5G NR LB @ 23 dBm	n5	460	mA
	5G NR MB @ 23 dBm	n1	970	mA
	5G NR HB @ 23 dBm	n7	740	mA
	5G NR UHB @ 26 dBm	n78	480	mA
5G SA (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	490	mA
LTE + 5G EN-DC	LTE DL, 256QAM	DC_3A_n78A	1168	mA
	LTE UL QPSK			
	NR DL, 256QAM			
	NR UL QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

Table 44: Averaged Current Consumption for RM520N-EU

Mode	Conditions	Band/Combinations	Typ.	Unit
Power-off	Power off	-	195	μA
RF Disabled	**AT+CFUN=0** (USB 3.1 suspend)	-	4.6	mA
	AT+CFUN=4 (USB 3.1 suspend)	-	4.7	mA

Sleep State	SA FDD PF = 64 (USB 3.1 suspend)	-	9.7	mA
	SA TDD PF = 64 (USB 3.1 suspend)	-	9.4	mA
Idle State	SA PF = 64 (USB 2.0 active)	-	40	mA
	SA PF = 64 (USB 3.1 active)	-	60	mA
LTE	LTE LB @ 23 dBm	B5	747	mA
	LTE MB @ 23 dBm	B1	732	mA
	LTE HB @ 23 dBm	B7	1010	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	1163	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA (1 Tx)	5G NR LB @ 23 dBm	n5	721	mA
	5G NR MB @ 23 dBm	n1	733	mA
	5G NR HB @ 23 dBm	n7	1015	mA
	5G NR UHB @ 26 dBm	n78	449	mA
5G SA (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	565	mA
LTE + 5G EN-DC	LTE DL, 256QAM	DC_3A_n78A	912	mA
	LTE UL QPSK			
	NR DL, 256QAM			
	NR UL QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

NOTE

1. The power consumption test is performed with EVB at room temperature without any thermal dissipation measure.
2. The power consumption above is for reference only, please contact Quectel Technical Support for detailed power consumption test report of the module.

6.3. Digital I/O Characteristic

Table 45: Logic Levels of 1.8 V Digital I/O

Parameter	Description	Min.	Max.	Unit
VDDIO_1V8	Supply voltage	1.7	1.94	V
V_{IH}	High-level input voltage	0.65 × VDDIO_1V8	VDDIO_1V8 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.35 × VDDIO_1V8	V
V_{OH}	High-level output voltage	VDDIO_1V8 - 0.45	-	V
V_{OL}	Low-level output voltage	-	0.45	V

Table 46: Logic Levels of 3.3 V Digital I/O

Parameter	Description	Min.	Max.	Unit
3.3 V	Supply voltage	3.135	3.465	V
V_{IH}	High-level input voltage	2.0	3.6	V
V_{IL}	Low-level input voltage	-0.5	0.8	V

Table 47: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V

V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-	V
V_{OL}	Low-level output voltage	-	0.4	V

Table 48: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 × USIM_VDD	V
V_{OH}	High-level output voltage	0.8 × USIM_VDD	-	V
V_{OL}	Low-level output voltage	-	0.4	V

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 49: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VCC, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.5. Thermal Dissipation

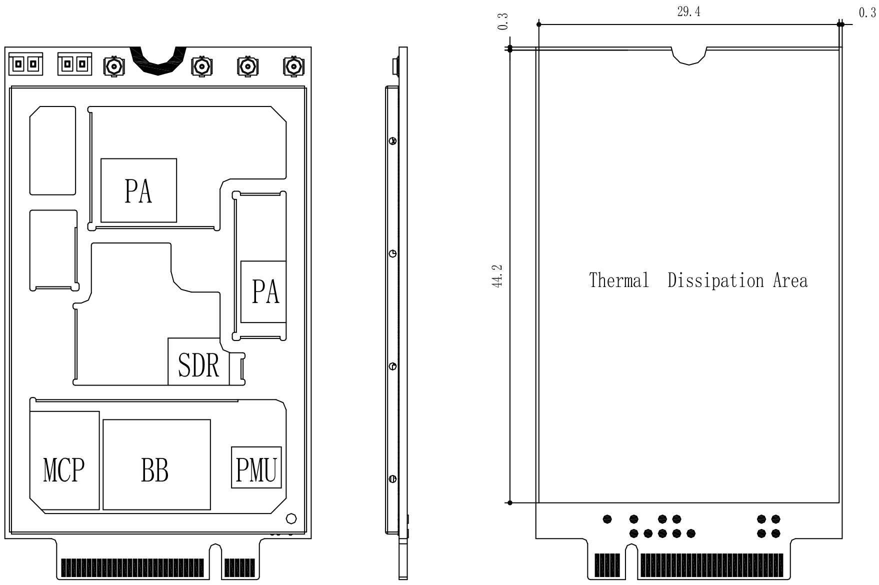


Figure 38: Thermal Dissipation Area Inside and on Bottom Side of the RM520N-GL

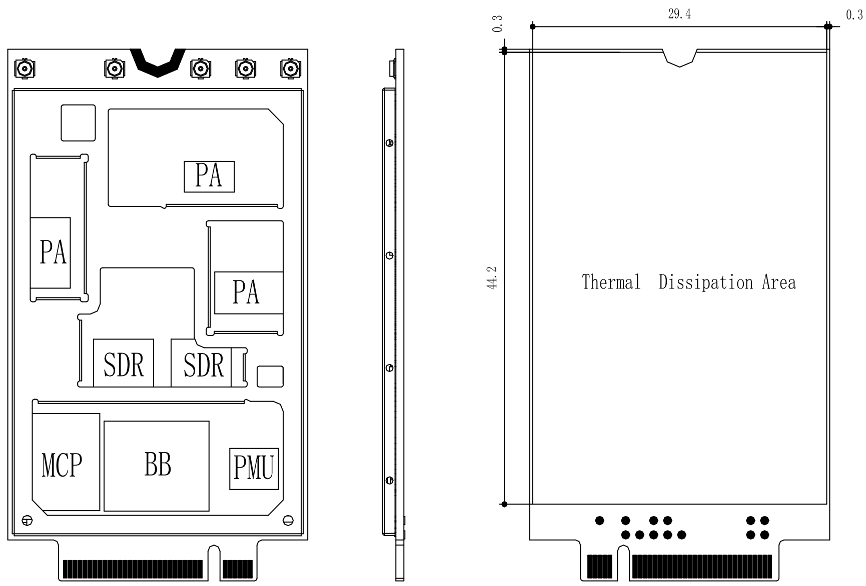


Figure 39: Thermal Dissipation Area Inside and on Bottom Side of the RM520N-EU

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper in the PCB area where module is mounted.
- Apply a soft thermal pad with appropriate thickness and high thermal conductivity between the module and the PCB to conduct heat.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely.
  - Choose the heatsink with adequate fins to dissipate heat.
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module.
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

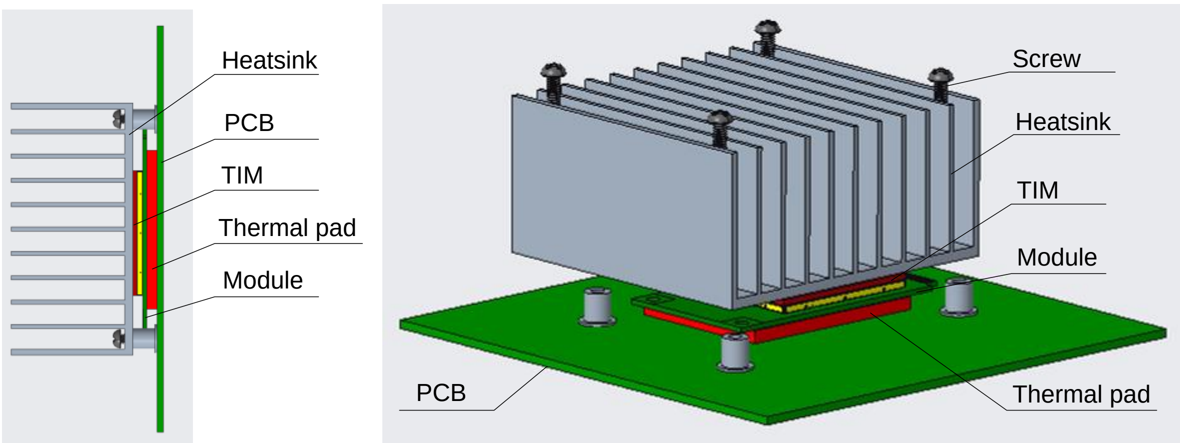


Figure 40: Placement and Fixing of the Heatsink

6.6. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 50: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
VCC	-0.3	-	4.7	V
Voltage at Digital Pins	-0.3	-	2.3	V

6.7. Operating and Storage Temperatures

Table 51: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [27]	-30	+25	+75	ºC
Extended Temperature Range [28]	-40	-	+85	ºC
Storage temperature Range	-40	-	+90	ºC

[27] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module meets 3GPP specifications.
[28] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as voice*, SMS, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

6.8. Notification

Please follow the principles below in module application.

6.8.1. Coating

If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module

6.8.2. Cleaning

Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.

6.8.3. Installing

It is recommended to fix the module firmly when the module is inserted into a socket.

7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of RM520N series modules. All dimensions are measured in mm, and the dimensional tolerances are ±0.15 mm unless otherwise specified.

7.1. Mechanical Dimensions

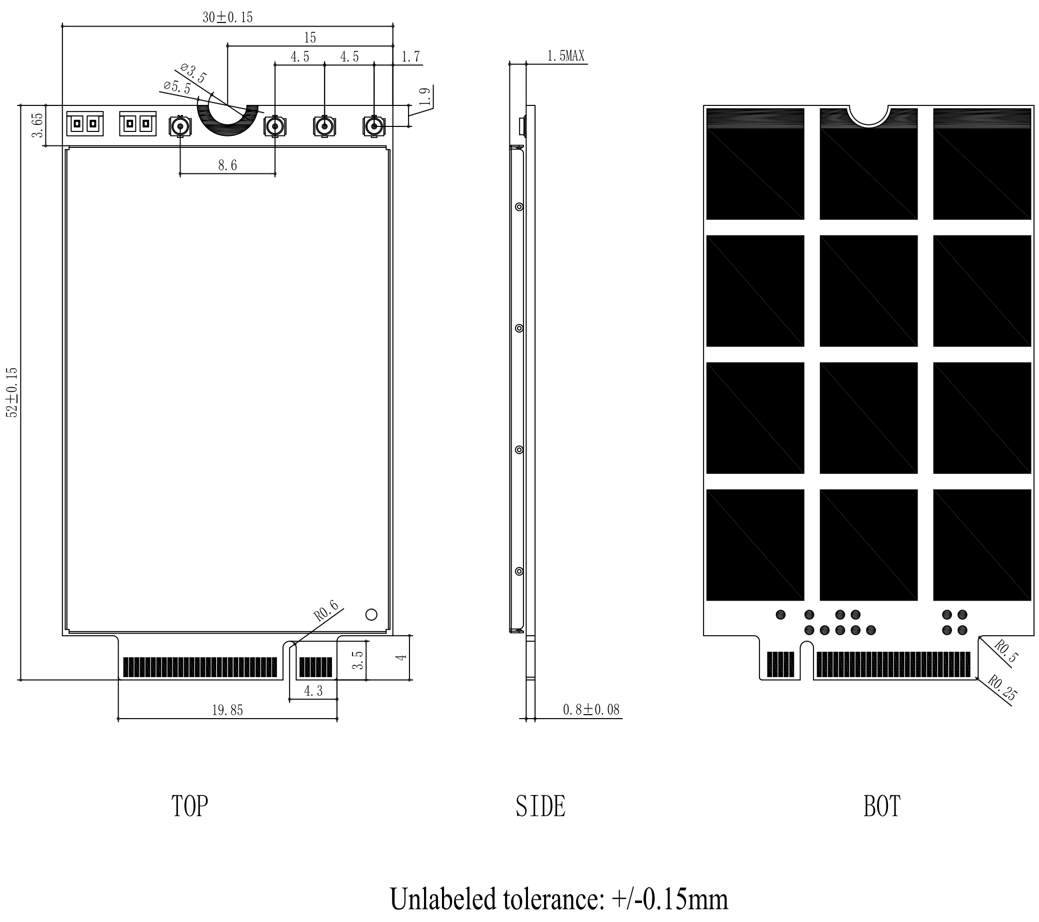


Figure 41: Mechanical Dimensions of the RM520N-GL (Unit: mm)

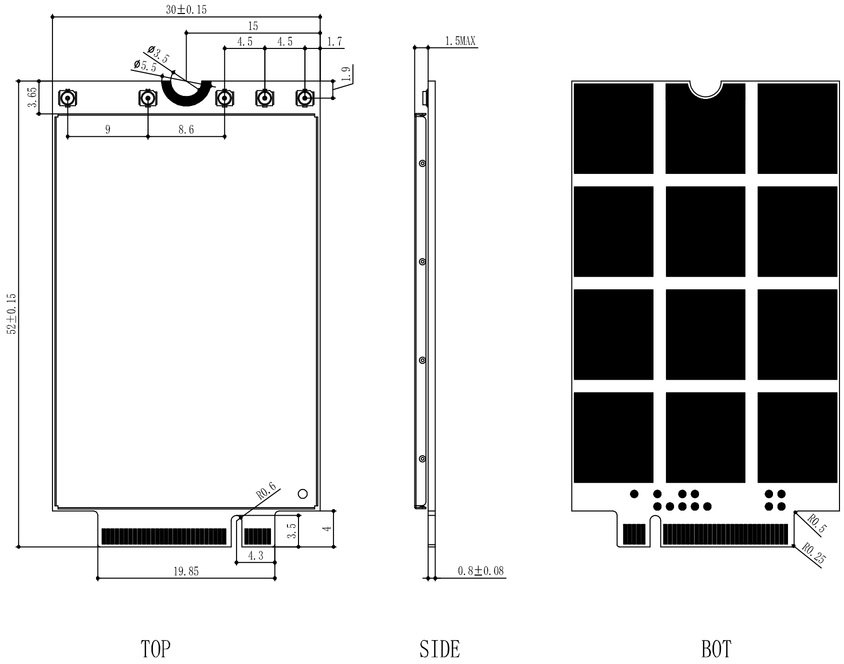


Figure 42: Mechanical Dimensions of the RM520N-EU (Unit: mm)

7.2. Top and Bottom Views

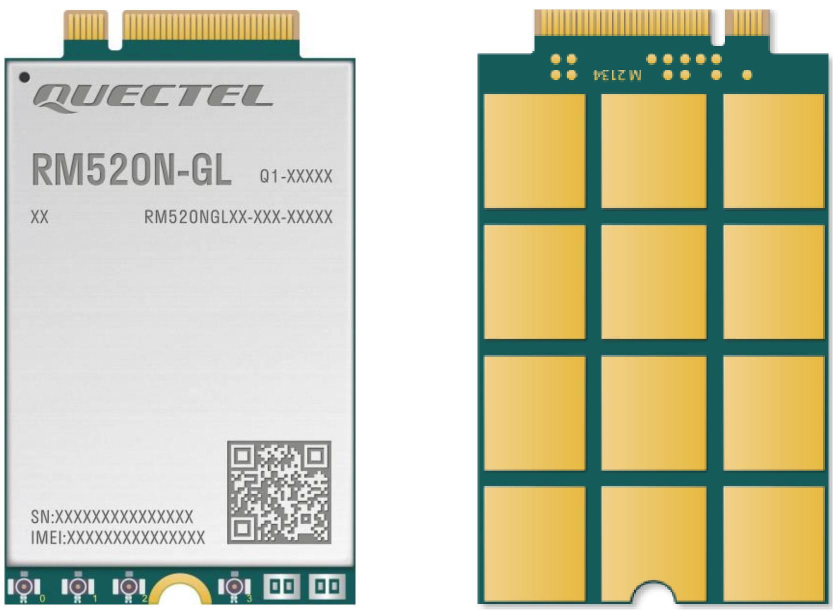
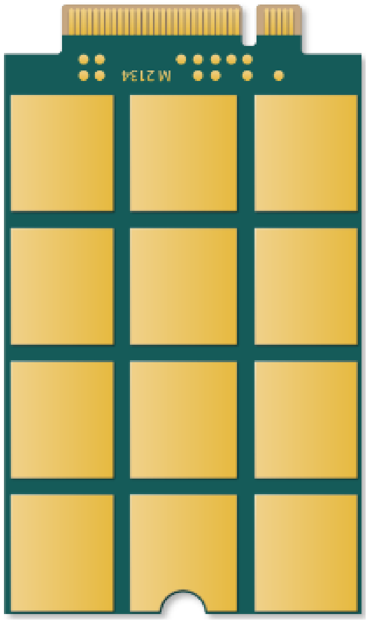


Figure 43: Top and Bottom Views of the RM520N-GL

Top View



Bottom View

Figure 44: Top and Bottom Views of the RM520N-EU

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7.3. M.2 Connector

The module adopts a standard PCI Express M.2 connector which compiles with the directives and standards listed in the PCI Express M.2 Specification.

7.4. Packaging

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts blister tray packaging and details are as follow:

7.4.1. Blister Tray

Dimension details are as follow:

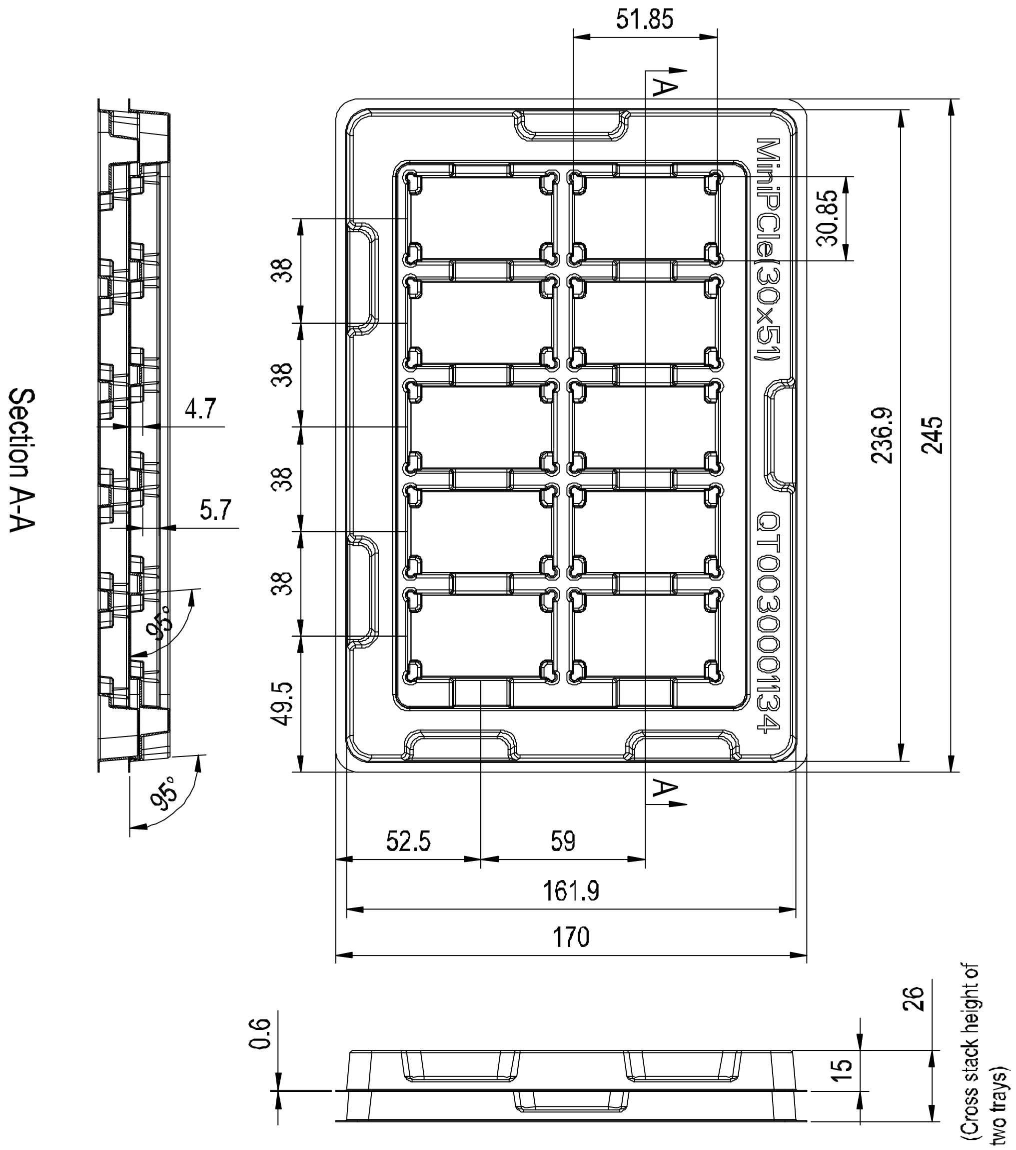
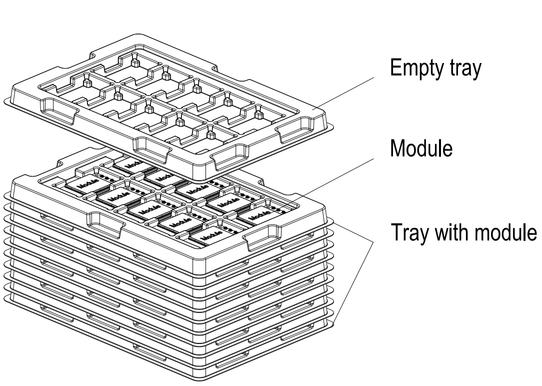
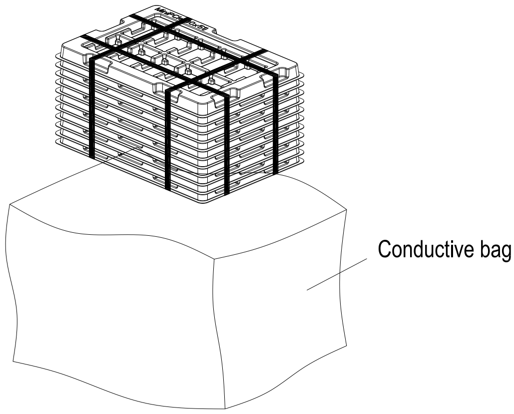


Figure 45: Blister Tray Dimension Drawing

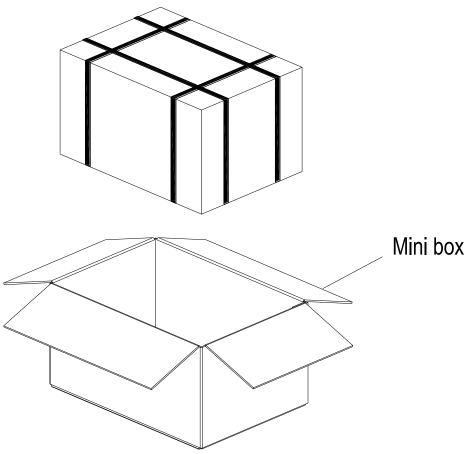
7.4.2. Packaging Process



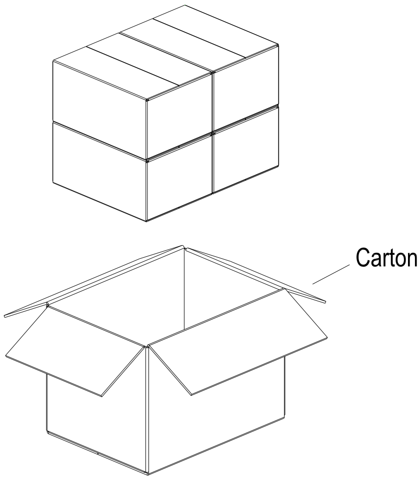
Pack 10 modules in each blister tray. Stack 10 blister trays with modules together, and put 1 empty blister tray on the top.



Pack 11 blister trays together and then put these blister trays into a conductive bag, seal and pack the conductive bag.



Put seal-packed blister trays into a mini box. One mini box contains 100 modules.



Put 4 mini boxes into 1 carton and then seal it. One carton can pack 400 modules.

Figure 46: Packaging Process

8 Appendix A References

Table 52: Related Documents

Document Name
[1] Quectel_RM520N_Series_Reference_Design
[2] Quectel_RM520N-GL_CA&EN-DC_Features
[3] Quectel_5G-M2_EVB_User_Guide
[4] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_AT_Commands_Manual
[5] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_GNSS_Application_Note
[6] Quectel_RG520N&RG525F&RG5x0F&RM5x0N_Series_RF_Application_Note

Table 53: Terms and Abbreviations

Abbreviation	Description
APT	Average Power Tracking
BIOS	Basic Input Output System
bps	Bit Per Second
CHAP	Challenge-Handshake Authentication Protocol
COEX	Coexistence
CPE	Customer Premise Equipment
CSQ	Cellular Signal Quality
DC-DC	Direct Current to Direct Current
DFOTA	Delta Firmware Upgrade Over-The-Air
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access

DL	Downlink
DPR	Dynamic Power Reduction
DRX	Discontinuous Reception (***Chapter 3.1.1***) Diversity Reception (***Chapter 5***)
EN-DC	E-UTRA New Radio Dual Connectivity
EP	End Point
ESD	Electrostatic Discharge
ET	Envelope Tracking
E-UTRA	Evolved Universal Terrestrial Radio Access
FDD	Frequency Division Duplexing
FOTA	Firmware Over-The-Air
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HB	High Band
HPUE	High Power User Equipment
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
IPQ	Qualcomm Internet Processor
kbps	Kilo Bits Per Second
LAA	License Assisted Access
LED	Light Emitting Diode
LTE	Long Term Evolution
MB	Middle Band

Mbps	Mega Bits Per Second
ME	Mobile Equipment
MIMO	Multiple-Input Multiple-Output
MLCC	Multilayer Ceramic Chip Capacitor
MO	Mobile Originated
MSB	Most Significant Bit
MT	Mobile Terminated
NR	New Radio
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RC	Root Complex
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RFFE	RF Front-End
Rx	Receive
SAR	Specific Absorption Rate
SCS	Sub-Carrier Spacing
SIMO	Single Input Multiple Output
SMS	Short Message Service
TCP	Transmission Control Protocol

TDD	Time Division Duplexing
TTFF	Time to First Fix
Tx	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UHB	Ultra High Band
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

9 Appendix B Operating Frequency

Table 54: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz

n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz
n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz

n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz
n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz

Table 55: Operating Frequencies (2G + 3G + 4G)

2G	3G	4G	Duplex Mode	Uplink	Downlink	Unit
-	B1	B1	FDD	1920–1980	2110–2170	MHz
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990	MHz
DCS1800	B3	B3	FDD	1710–1785	1805–1880	MHz
-	B4	B4	FDD	1710–1755	2110–2155	MHz
GSM850	B5/BC0	B5	FDD	824–849	869–894	MHz
-	B6	-	FDD	830–840	875–885	MHz
-	B7	B7	FDD	2500–2570	2620–2690	MHz
EGSM900	B8	B8	FDD	880–915	925–960	MHz
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9	MHz
-	B10	B10	FDD	1710–1770	2110–2170	MHz
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9	MHz

-	B12	B12	FDD	699–716	729–746	MHz
-	B13	B13	FDD	777–787	746–756	MHz
-	B14	B14	FDD	788–798	758–768	MHz
-	-	B17	FDD	704–716	734–746	MHz
-	-	B18	FDD	815–830	860–875	MHz
-	B19	B19	FDD	830–845	875–890	MHz
-	B20	B20	FDD	832–862	791–821	MHz
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9	MHz
-	B22	B22	FDD	3410–3490	3510–3590	MHz
-	-	B24	FDD	1626.5–1660.5	1525–1559	MHz
-	B25	B25	FDD	1850–1915	1930–1995	MHz
-	B26	B26	FDD	814–849	859–894	MHz
-	-	B27	FDD	807–824	852–869	MHz
-	-	B28	FDD	703–748	758–803	MHz
-	-	B29	FDD [29]	-	717–728	MHz
-	-	B30	FDD	2305–2315	2350–2360	MHz
-	-	B31	FDD	452.5–457.5	462.5–467.5	MHz
-	-	B32	FDD [29]	-	1452–1496	MHz
-	B33	B33	TDD	1900–1920	1900–1920	MHz
-	B34	B34	TDD	2010–2025	2010–2025	MHz
-	B35	B35	TDD	1850–1910	1850–1910	MHz
-	B36	B36	TDD	1930–1990	1930–1990	MHz
	B37	B37	TDD	1910–1930	1910–1930	MHz
-	B38	B38	TDD	2570–2620	2570–2620	MHz
-	B39	B39	TDD	1880–1920	1880–1920	MHz

[29] Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	B40	B40	TDD	2300–2400	2300–2400	MHz
-	-	B41	TDD	2496–2690	2496–2690	MHz
-	-	B42	TDD	3400–3600	3400–3600	MHz
-	-	B43	TDD	3600–3800	3600–3800	MHz
-	-	B44	TDD	703–803	703–803	MHz
-	-	B45	TDD	1447–1467	1447–1467	MHz
-	-	B46	TDD	5150–5925	5150–5925	MHz
-	-	B47	TDD	5855–5925	5855–5925	MHz
-	-	B48	TDD	3550–3700	3550–3700	MHz
-	-	B50	TDD	1432–1517	1432–1517	MHz
-	-	B51	TDD	1427–1432	1427–1432	MHz
-	-	B52	TDD	3300–3400	3300–3400	MHz
-	-	B65	FDD	1920–2010	2110–2200	MHz
-	-	B66	FDD	1710–1780	2110–2200 [30]	MHz
-	-	B67	FDD [29]	-	738–758	MHz
-	-	B68	FDD	698–728	753–783	MHz
-	-	B69	FDD [29]	-	2570–2620	MHz
-	-	B70	FDD [31]	1695–1710	1995–2020	MHz
-	-	B71	FDD	663–698	617–652	MHz
-	-	B72	FDD	451–456	461–466	MHz
-	-	B73	FDD	450–455	460–465	MHz
-	-	B74	FDD	1427–1470	1475–1518	MHz
-	-	B75	FDD [29]	-	1432–1517	MHz

[30] The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.
[31] The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 295 MHz.

-	-	B76	FDD [29]	-	1427–1432	MHz
-	-	B85	FDD	698–716	728–746	MHz
-	-	B87	FDD	410–415	420–425	MHz
-	-	B88	FDD	412–417	422–427	MHz