HDMI/DVI to LVDS Bridge

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ABSTRACT

This document provides an overview of HDMI/DVI to LVDS bridge solutions. The two-chip solutions receive 3 TMDS pairs and a clock, and output 4 or 8 LVDS data pairs and clocks.

Block Diagrams

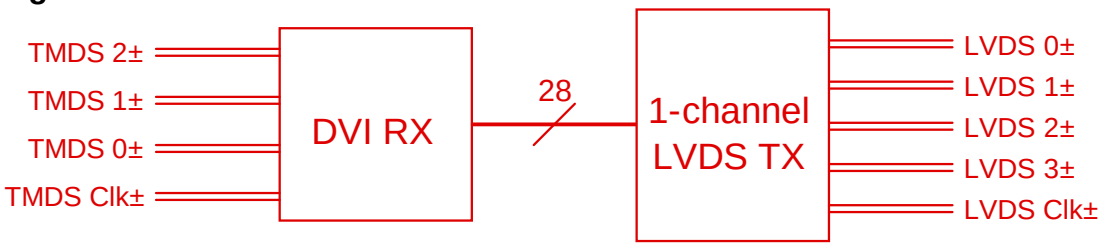

Figure 1. Circuit using 1-channel LVDS

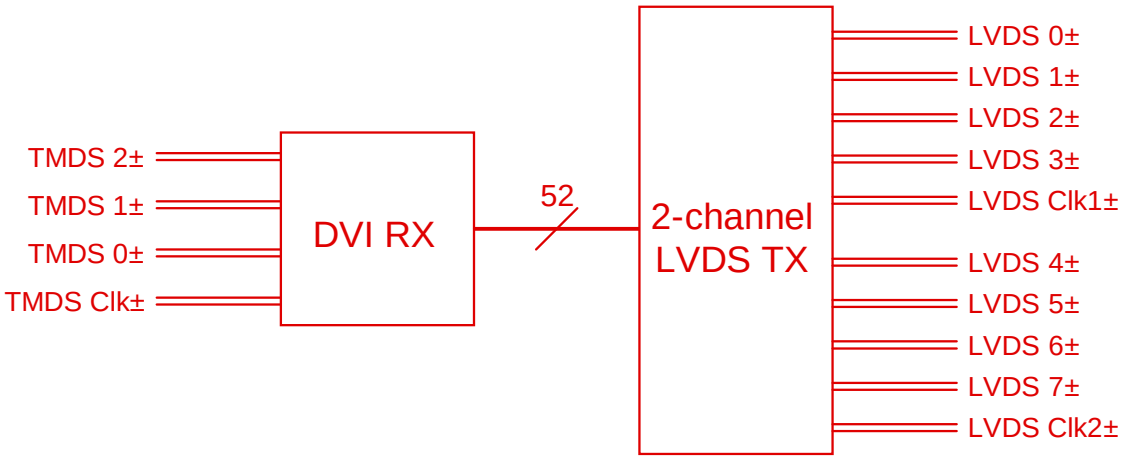

Figure 2. Circuit using 2-channel LVDS

The DVI RX output is configurable with pin “PIXS”. When PIXS is Low, RGB data is output on 24 bits (QE[23:0]). When PIXS is High, RGB data is split odd/even on 48-bits. The 4 additional bits are VSYNC, HSYNC, DE, and ODCK.

1-Channel vs. 2-Channel

The choice between using a 1-channel or 2-channel LVDS transmitter depends on what the connecting panel uses. Most panels that receive LVDS that have a resolution of <1400x1050 use 1-channel, which consists of 3 or 4 LVDS data pairs (depending on 18-bit or 24-bit color). Most panels that have a resolution between 1400x1050 – 1920x1200 use a 2-channel receiver interface, with 6 or 8 LVDS data pairs.

The DVI RX

There are 3 recommended DVI receivers to choose from:

- TFP401A
- TFP401A-EP (extended temperature range)
- TFP501 (HDCP support)

The LVDS TX

For 1-channel LVDS, there are 3 recommended devices:

- SN75LVDS83B (supports 10-135MHz; TSSOP or BGA)
- SN75LVDS83C (supports 10-85MHz, and 13-23% lower power than 83B; BGA-only)
- SN65LVDS93A (supports 10-135MHz, and extended temperature range; TSSOP or BGA)

For 2-channel LVDS,

- DS90C387A is recommended.

Notes on Common Resolutions

- 1280x800 and 720p usually use 1-channel LVDS with a 70-75MHz pixel clock.
- 1080p usually uses 2-channel LVDS with a 74.25MHz clock.
- 1080p 120Hz often uses high frequency HDMI and 4-channel LVDS; this is not supported.

Design Guidelines

1. If using the 83B, 83C, or 93A, set power supply “IOVCC” to 3.3V. The DVI RX output is always 3.3V.

2. Set the same clock edge for the two devices. If DVI RX pin “OCK_INV” is High, set LVDS TX pin “CLKSEL” (83B/83C/93A) or “R_FB” (387A) also High. When using the 387A, set pin “DUAL” to High to set the 48:8 mode.

3. Place the two devices reasonably close together to minimize parallel trace length and EMR. Match the trace lengths of the 28-bit/52-bit parallel lines within 1 inch.

4. The incoming TMDS data must be DVI-compliant, and not contain HDMI island data (e.g. audio) or deep color (more than 24 color bits).

5. Here is the DVI RX reference design (the TFP403 is virtually the same as the TFP401A): http://focus.ti.com/lit/an/slla134/slla134.pdf

Pin Mapping Examples

The parallel pin mapping defines the sequence of bits in the LVDS lanes. It must match the bit sequence that the panel expects. The 1-channel and 2-channel examples below show common schemes, to serve as a reference.

There's an important caveat for 2-channel applications: different panels define "odd" versus "even" differently. Some say the first pixel (top-left) is odd, and some say it's even. The table on the next page follows the TFP401A's convention that the first pixel is even. If you use a panel that defines the first pixel as odd, then QO[0:23] and QE[0:23] must be swapped from what the table shows, and then Figure 4 will describe odd/even according to your panel's nomenclature.

DVI Output	Description	83B/83C/93A Input
QE[0]	B0 (LSB)	D15
QE[1]	B1	D18
QE[2]	B2	D19
QE[3]	B3	D20
QE[4]	B4	D21
QE[5]	B5	D22
QE[6]	B6	D16
QE[7]	B7 (MSB)	D17
QE[8]	G0 (LSB)	D7
QE[9]	G1	D8
QE[10]	G2	D9
QE[11]	G3	D12
QE[12]	G4	D13
QE[13]	G5	D14
QE[14]	G6	D10
QE[15]	G7 (MSB)	D11
QE[16]	R0 (LSB)	D0
QE[17]	R1	D1
QE[18]	R2	D2
QE[19]	R3	D3
QE[20]	R4	D4
QE[21]	R5	D6
QE[22]	R6	D27
QE[23]	R7 (MSB)	D5
HSYNC	HSYNC	D24
VSYNC	VSYNC	D25
DE	DATA EN	D26
	RSVD	D23
ODCK	CLK	CLKIN

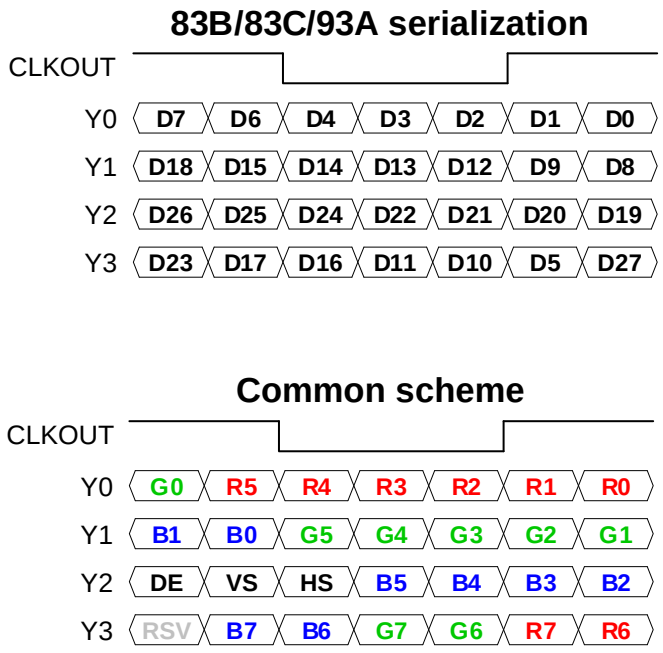

Figure 3. 1-Channel LVDS Connection Example

DVI Output	Description	387A Input
QO[0]	Odd B0 (LSB)	B10
QO[1]	Odd B1	B11
QO[2]	Odd B2	B12
QO[3]	Odd B3	B13
QO[4]	Odd B4	B14
QO[5]	Odd B5	B15
QO[6]	Odd B6	B16
QO[7]	Odd B7 (MSB)	B17
QO[8]	Odd G0 (LSB)	G10
QO[9]	Odd G1	G11
QO[10]	Odd G2	G12
QO[11]	Odd G3	G13
QO[12]	Odd G4	G14
QO[13]	Odd G5	G15
QO[14]	Odd G6	G16
QO[15]	Odd G7 (MSB)	G17
QO[16]	Odd R0 (LSB)	R10
QO[17]	Odd R1	R11
QO[18]	Odd R2	R12
QO[19]	Odd R3	R13
QO[20]	Odd R4	R14
QO[21]	Odd R5	R15
QO[22]	Odd R6	R16
QO[23]	Odd R7 (MSB)	R17
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC

DVI Output	Description	387A Input
QE[0]	Even B0 (LSB)	B20
QE[1]	Even B1	B21
QE[2]	Even B2	B22
QE[3]	Even B3	B23
QE[4]	Even B4	B24
QE[5]	Even B5	B25
QE[6]	Even B6	B26
QE[7]	Even B7 (MSB)	B27
QE[8]	Even G0 (LSB)	G20
QE[9]	Even G1	G21
QE[10]	Even G2	G22
QE[11]	Even G3	G23
QE[12]	Even G4	G24
QE[13]	Even G5	G25
QE[14]	Even G6	G26
QE[15]	Even G7 (MSB)	G27
QE[16]	Even R0 (LSB)	R20
QE[17]	Even R1	R21
QE[18]	Even R2	R22
QE[19]	Even R3	R23
QE[20]	Even R4	R24
QE[21]	Even R5	R25
QE[22]	Even R6	R26
QE[23]	Even R7 (MSB)	R27
DE	ENABLE	DE
ODCK	CLK	CLKIN

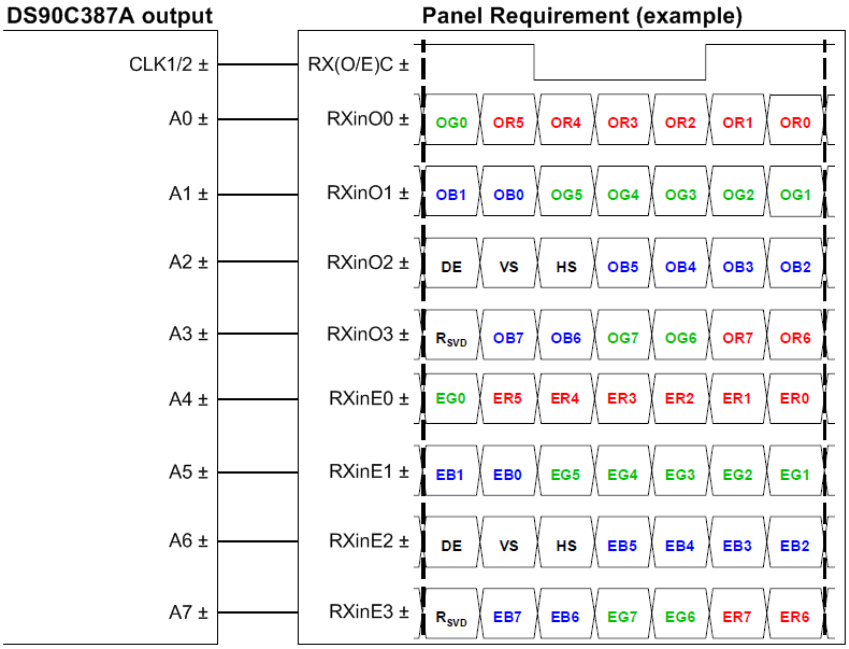

Figure 4. 2-Channel LVDS Connection Example

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