Application Note
DP83867 Troubleshooting Guide

TEXAS INSTRUMENTS

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1 Trademarks
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2 DP83867 Application Overview

The DP83867 is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support the 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols.

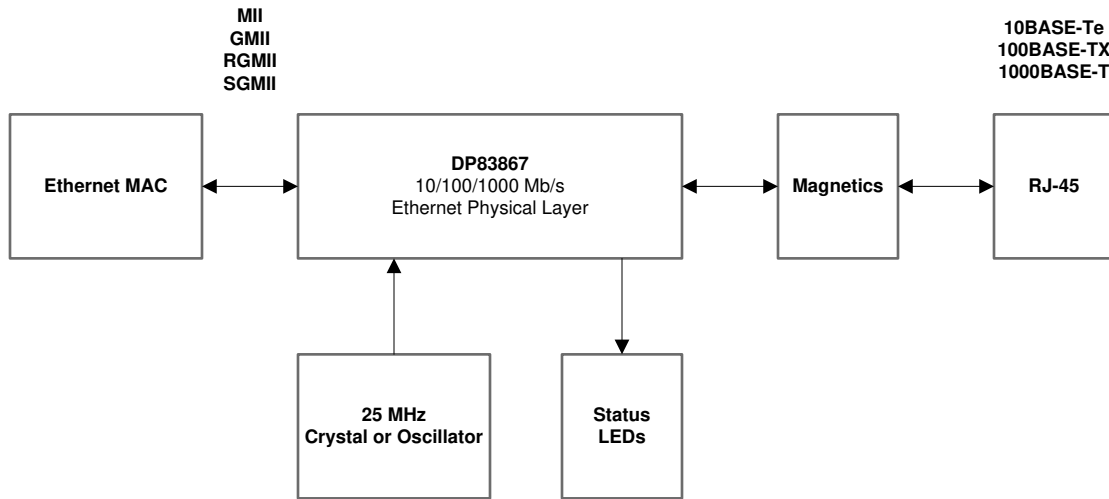Figure 2-1 is a high-level system block diagram of a typical DP83867 application.

Figure 2-1. DP83867 Block Diagram

The DP83867 will connect to an Ethernet MAC and to a media. The connection to the media is via a transformer and a connector.

3 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

3.1 Read and Check Register Values

Read the registers and verify the default values shown in the datasheet. Note that the initial values of some registers can vary based on strap options.

The expected register values for PHY operation and link in 1000 Mbps with auto-negotiation enabled are shown below.

Table 3-1. DP83867 Register Value References

Register Address	Register Value
0x0000	1140
0x0001	769D
0x0002	2000
0x0003	A231
0x0004 [1]	0061
0x0005 [2]	C1E1
0x0006	006F
0x0007	2001
0x0008	4806
0x0009	0300
0x000A	3C00
0x000D	401F
0x000E	0000
0x000F	3000
0x0010	5048
0x0011	BF02
0x0012	0000
0x0013	1C42
0x0014	29C7
0x0015	0000
0x0016	0000
0x0017	0040
0x0018	6150
0x0019	4444
0x001A	0002
0x001E	0002

With the PHY linked in a given speed, use these values as a reference to identify any variance from the expected operation.

(1) 1000 Mbps was forced by disabling the advertisements of other speeds in register 0x4.

(2) The value of register 0x5 will vary depending on link partner advertisements.

Example: After powering and linking the PHY in 10 Mbps, register 0x0001 is read at hex value 7969. Noting the difference in this value from the expected value of 796D, the equivalent binary values are used to identify which bits are distinct. In this case, bit[2] is low, while the expected value is high. Referencing the datasheet register map, bit[2] of register 0x0001 corresponds to link status. From this, it is known that the PHY is not linked.

Repeating this process for any values distinct from the expected values shown in the table will help diagnose the exact state of the PHY for any encountered issues.

For information about reading and writing registers using the USB-2-MDIO interface, refer to the Tools chapter.

3.2 Schematic and Layout Checklist

Reference and verify all of the noted schematic and layout recommendations in the following spreadsheet:

DP83867 Schematic and Layout Checklist

3.3 Component Checklist

Magnetics:

The following guidelines are the main specifications to reference for compatible magnetics:

Table 3-2. Magnetic Isolation Requirements

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Open Circuit Inductance	-	320 to 350	µH
Insertion Loss	1-100 MHz	-1	dB
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-100 MHz	-10	dB
Differential to Common Mode Rejection Ratio	1-50 MHz	-30	dB
	50-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Isolation	HPOT	1500	Vrms

If these exact requirements cannot be met, the following allowances can be made:
- Turns ratio
  - Ideally 2%, but 3% is tolerable.
- Inductance
  - High inductance is preferred. Usual numbers seen are around 350 µH.
- Insertion loss
  - As close to 0 dB as possible compared to specified value for each range stated in data sheet. If specification gives -1 dB as typical. finding a component with -1 dB, -0.9 dB, … is recommended.
- Return loss
  - At or lower than the magnitude specified in data sheet. If specification gives -16 dB as typical, finding a component with -16 dB, -17 dB, … is recommended.

Crystal / Oscillator

The following guidelines are the main specifications to reference for compatible crystals:

Table 3-3. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm

If opting for an oscillator:

Table 3-4. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	
Jitter RMS	Integration Band: 12 kHz to 5 MHz			11	ps

3.4 Peripheral Pin Checks

The following section details the expected values of various peripheral output pins of the PHY during operation - measure and compare the noted pin outputs to verify PHY operation.

3.4.1 Power Supplies

The power supplies are the first key item to check. Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in the *Recommended Operating Conditions* section of the datasheet.
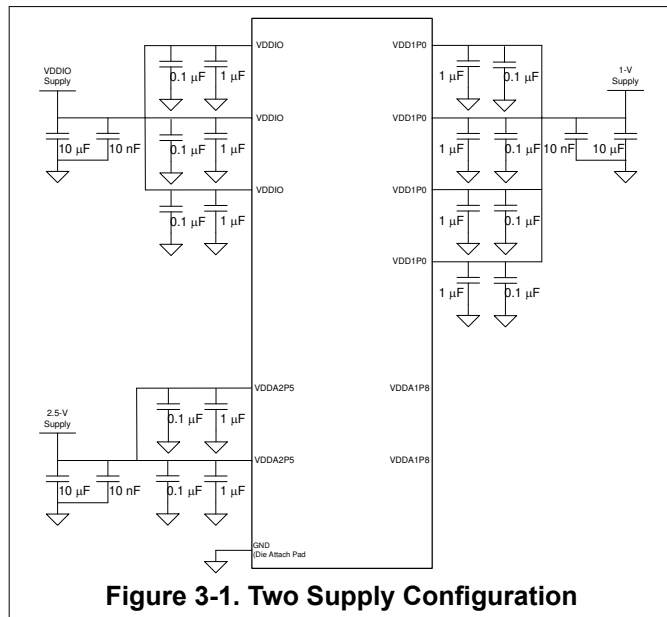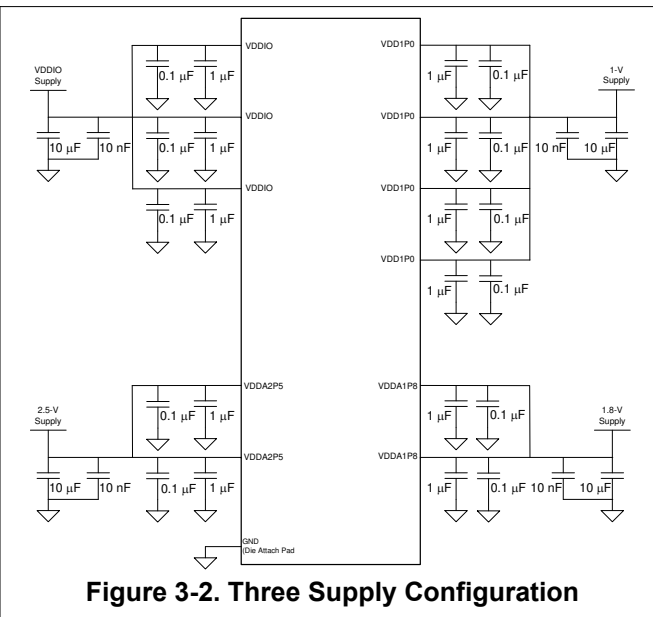

Figure 3-1. Two Supply Configuration　　**Figure 3-2. Three Supply Configuration**

The DP83867 supports two configurations for power supplies as shown in Figure 3-1 and Figure 3-2 above. It can operate with as few as two supplies. When operating in the three supply configuration, the VDDA1P8 supply must be stable within 25ms of the VDDA2P5 supply ramping up. There is no sequencing requirement for other supplies when operating in three supply mode. When powering down the DP83867, the VDDA1P8 supply should be brought down before the VDDA2P5 supply. Power up the board and verify the sequence of these supplies with an oscilloscope.

3.4.2 RBIAS Voltage and Resistance

The RBIAS resistor is used to develop the internal bias currents and voltages in the PHY. It is specified for 1% tolerance so that the PHY can meet the tightest IEEE 802.3 specifications.

Measure the DC value of the voltage across the RBIAS resistor and confirm that the voltage is 1 V.

Power down the board and verify that the RBIAS resistor value is 11 kΩ ±1%.

3.4.3 Probe the XI Clock

Verify the frequency and signal integrity. For link integrity the clock must be 25 MHz ±50 ppm.

If using a crystal as the clock source, probe the CLK_OUT signal. Probing the crystal can change the capacitive loading and therefore change the operational frequency. The default signal on CLK_OUT is a buffered version of the XI reference and will provide a representative measurement.

3.4.4 Probe the RESET_N Signal

The reset input is active low. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.

3.4.5 Probe the Strap Pins During Initialization

In some cases, other devices on the board (for example, the MAC) will pull or drive these pins unexpectedly. Confirm that these signals are in the range of the target voltages described in the datasheet. Measurements can be made during power up and after power up when the RESET_N signal is asserted.

For further confirmation, the strap values can be read from the registers. The values are available in register 0x006E (STRAP_STS1) and register 0x006F (STRAP_STS2).

3.4.6 Probe the Serial Management Interface Signals (MDC, MDIO)

MDIO should pull up to the I/O supply when undriven. Probe MDIO to confirm the default voltage.

Attempt to read the registers. Verify the MDIO data sequence with the datasheet to make sure the MDIO read access timing is correct. Probe the MDC/MDIO signals during read and write operations, referencing the expected waveforms below:
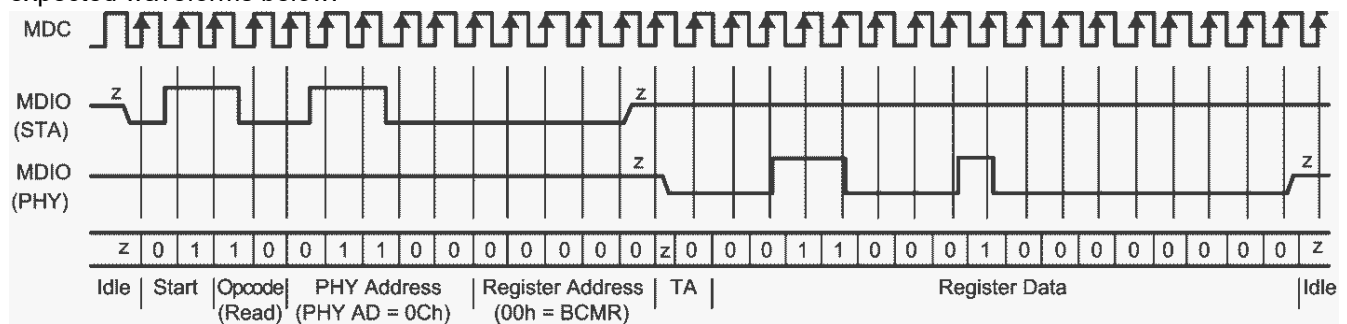

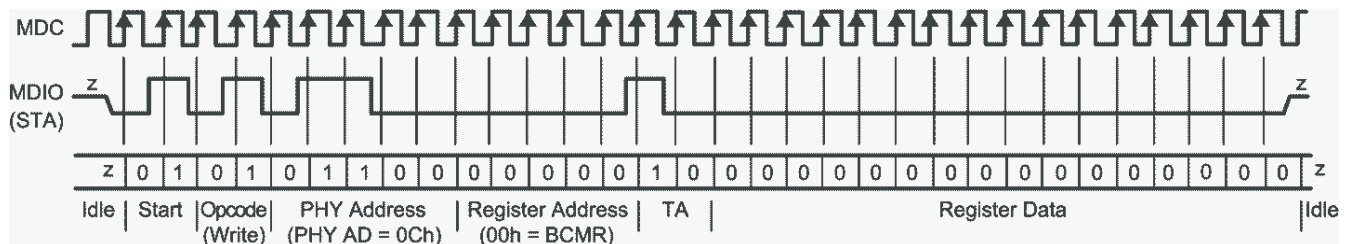**Figure 3-3. Typical MDC/MDIO Read Operation**

Figure 3-4. Typical MDC/MDIO Write Operation

3.4.7 Probe the MDI Signals

In the default configuration, Auto-negotiation and Auto-MDIX will be enabled. A link pulse should be visible on the channel A and channel B transmit and receive differential pairs (TD_P_A, TD_M_A, TD_P_B, TD_M_B).

A short Ethernet cable with 100 Ohm terminations can be used for measuring the MDI signals. A terminated cable is shown in Figure 3-5. A connection diagram for making measurements with the terminated cable is shown in Figure 3-6.
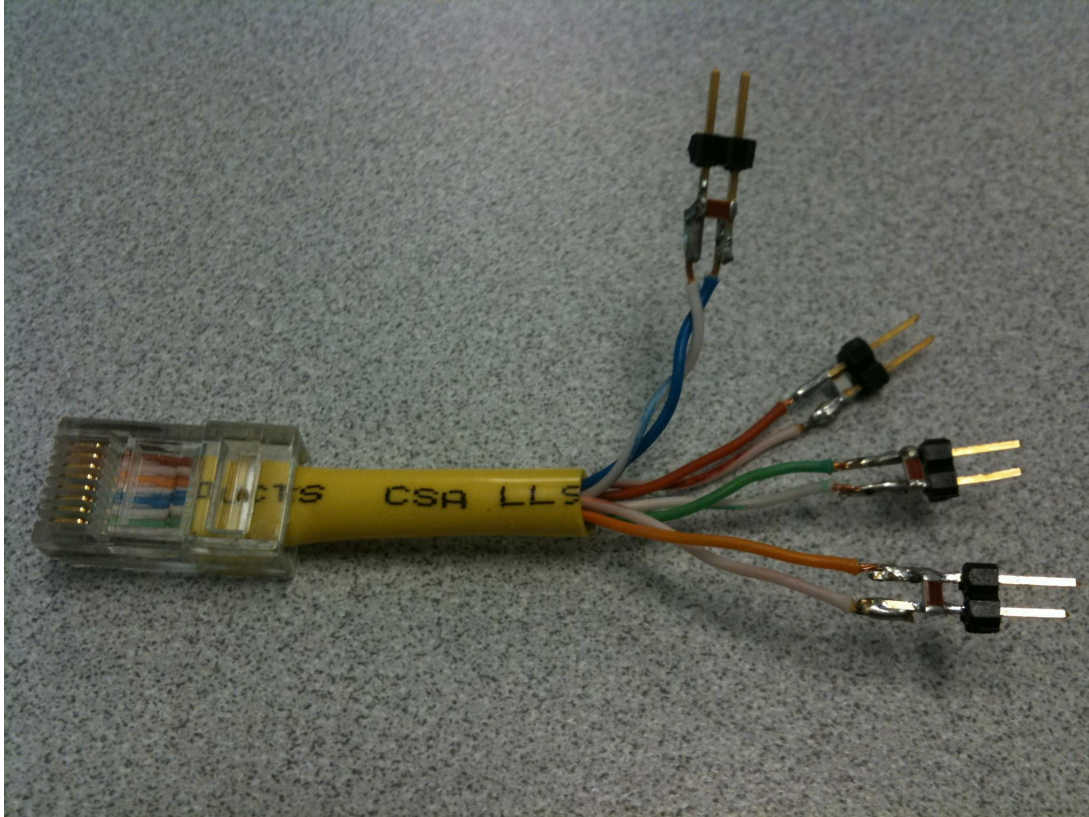

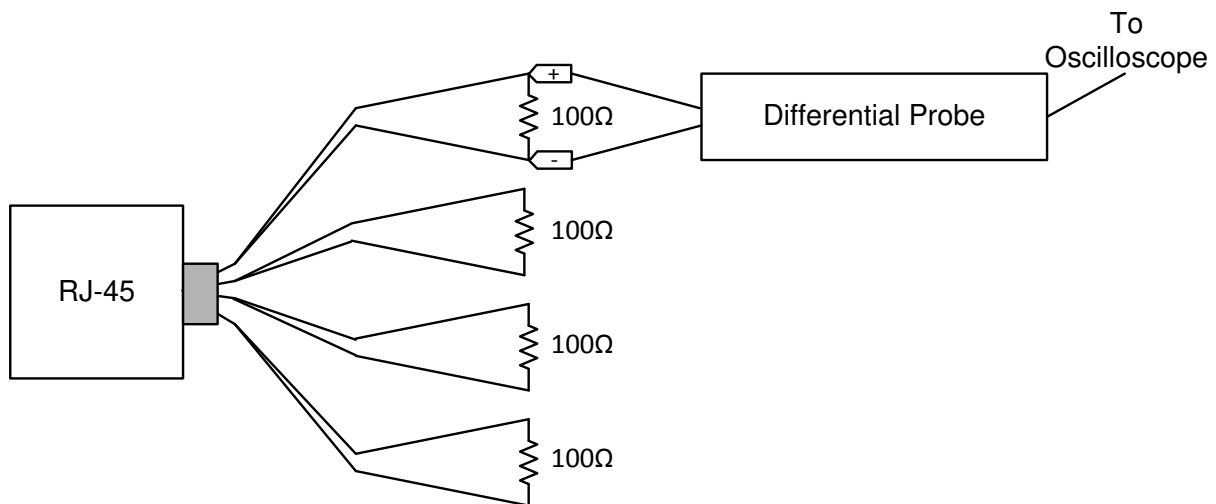**Figure 3-5. 100 Ohm Terminated Cable for MDI Signal Measurement**

Figure 3-6. Connection Diagram for 100M Terminated Cable

Auto-Negotiation link pulses are nominally 100ns wide. Pulses are spaced by 62µs or 125µs and are transmitted in bursts. The bursts are nominally 2ms in duration and occur every 16ms. An example link pulse is shown below in Figure 3-7
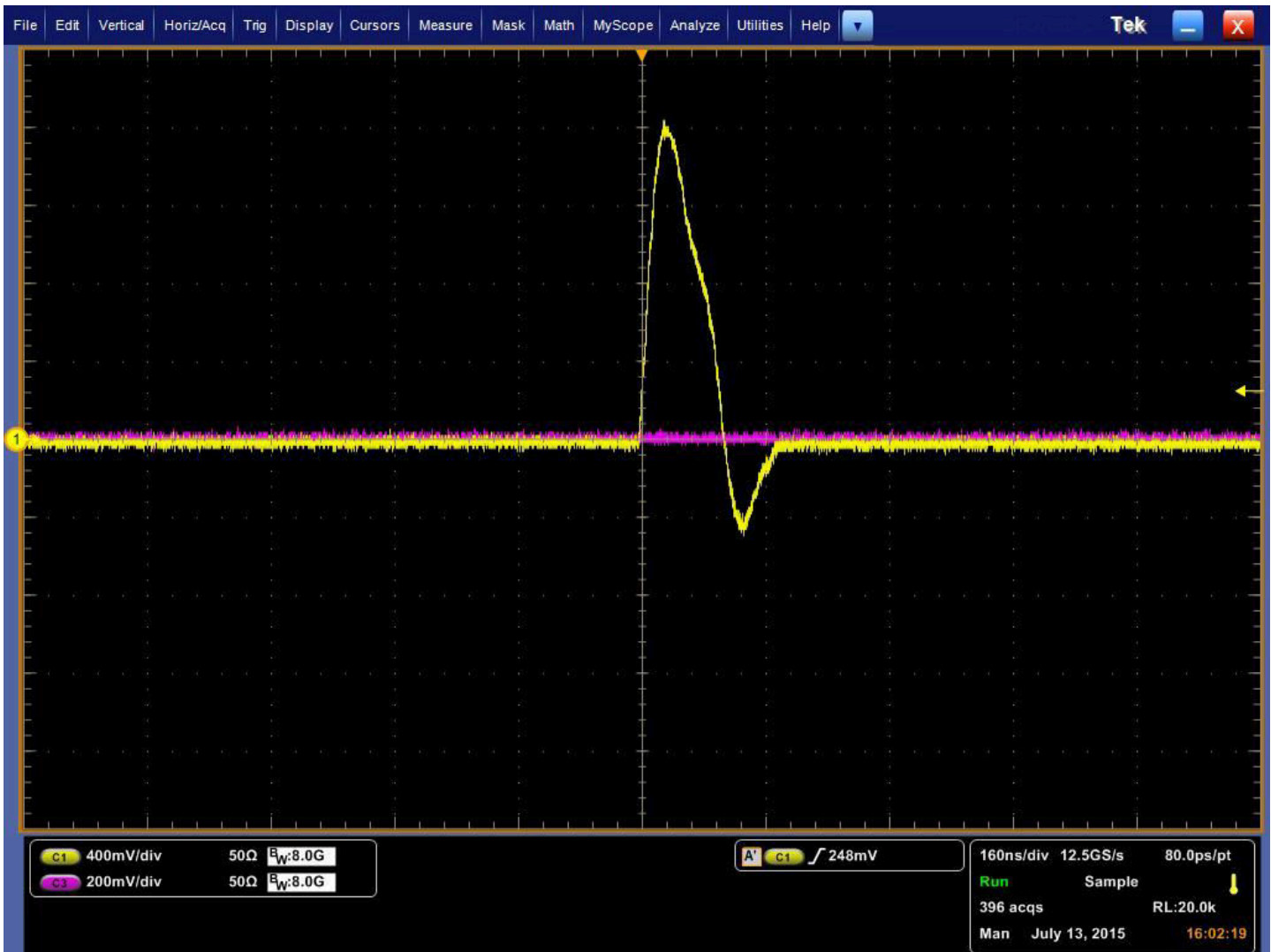
Figure 3-7. DP83867 Link Pulse

Observing this pulse confirms the PHY is on and attempting to link.

3.5 Link Quality Check

With the PHY powered and connected to a link partner, the following registers can be read from to determine the health of the link:

Table 3-5. Link Quality MSE Registers

Channel	Register Address
A	0x225
B	0x265
C	0x2A5
D	0x2E5

For a given channel, read the register value to determine the MSE (Mean Square Error), convert to decimal, and refer to the following table to determine link quality:

Table 3-6. MSE Link Quality Ranges

Link Quality	MSE Range
Excellent	< 522
Good	522 - 827
Poor	> 827

For information on how to read and write registers in the extended register space, please refer to Tools.

3.6 Built-in Self Test with Various Loopback Modes

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using various loopback modes to isolate any issues to specific parts of the data path. The BIST generates packetized data with variable content and IPG. The following diagrams illustrate the various data paths that each loopback mode can be used to verify:
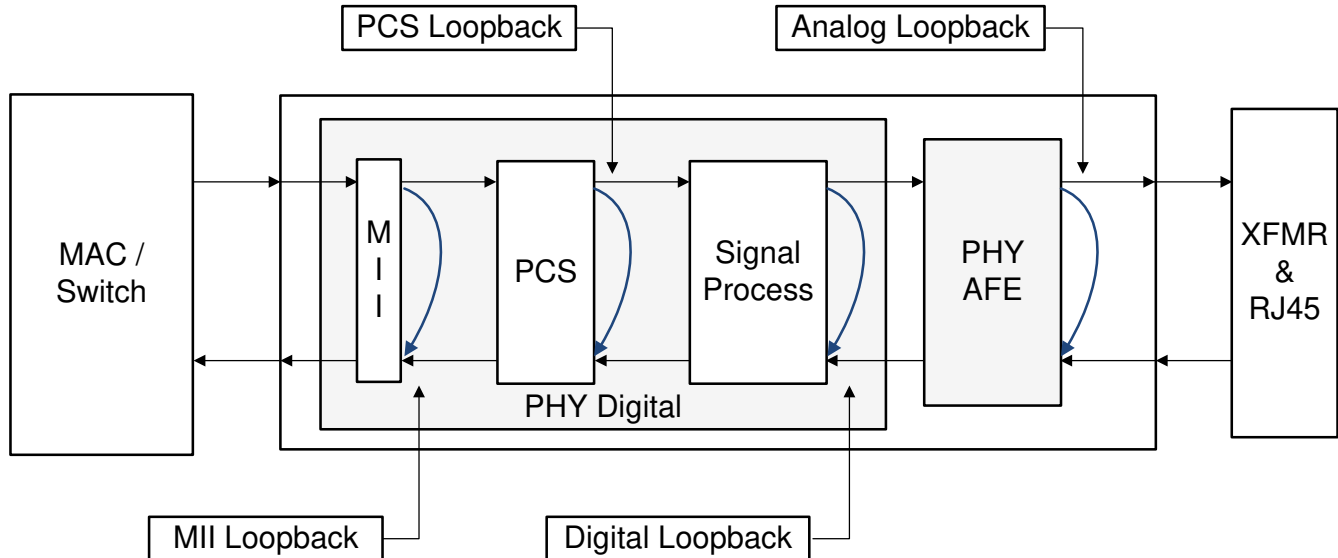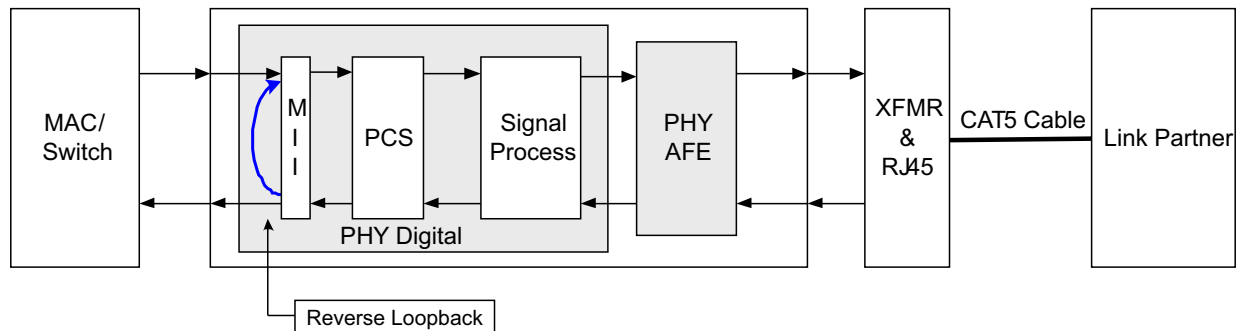

Figure 3-8. Block Diagram, Loopback Modes

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Figure 3-9. Block Diagram, Reverse Loopback Mode

Analog loopback is typically used to verify the PHY's full internal data path, while reverse loopback is used with a link partner to verify the data path along the MDI.

Transmitting and Receiving Packets with the MAC:

If generating and checking packets with the MAC is possible, and the PHY has a working link partner with reverse loopback capability, verify the full data path as follows:
1. Power and connect the PHY to the MAC and a working link partner.
2. Enable reverse loopback on the link partner (for DP83867 link partner, write 0x16 to 0020).
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receieves the same test packets.

If the MAC receives the same test packets transmitted without issue, the full data path through MAC → PHY → MDI is valid. If this test does not pass, perform analog loopback to isolate the issue along the data path:
1. Power and connect the PHY to the MAC.
2. Enable analog loopback on the PHY (write 0x16 to 0008).
3. Transmit test packets from the MAC to the PHY.

4.   Verify the MAC receives the same test packets.

If the MAC receives the same test packets, the data path through MAC → PHY is valid, and the issue has been isolated to the MDI data path. If this test does not pass, the issue could be on the MAC interface or the internal data path. To verify the MAC interface, refer to Debugging MAC Interface. To verify the internal data path, perform PRBS with analog loopback using the following script.

Transmitting and Receiving Packets with BIST:

If generating and checking packets with the MAC is not possible, use PRBS packet generation and checking functionalities to verify the data path. Perform reverse loopback with PRBS and a working link partner as follows:

1.   Power and connect the PHY to a link partner.
2.   Enable PRBS packet generation on the PHY (write 0x16 to 5000).
3.   Enable reverse loopback on the link partner (for DP83867 link partner, write 0x16 to 0020).
4.   Wait at least one second, then check PRBS lock status on the PHY (read register 0x17[11:10]).

If register 0x17[11] is high, the data path through PHY → MDI is valid. If this test does not pass, the issue could be on the PHY's internal data path or the MDI. To verify the internal data path, perform PRBS with analog loopback using the following script. If the internal data path is valid, then the issue is isolated to the MDI (assuming the link partner is working).

Below is an example sequence of register reads and writes to perform BIST with analog loopback in 10Mbps:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// hard reset
001F 8000
// disable auto-neg, force 10Mbps (1)
0000 0100
// enable analog loopback (2)
0016 0008
// force mdi mode for 10/100 Mbps (not relevant for 1000Mbps)
0010 5008
// loopback configuration register required
00FE E720
// enable packet gen, keep analog loopback (3)
0016 5008

// (1)
// for 100Mbps, write 0000 to 2100
// for 1000Mbps, write 0000 to 0140
// (2)
// for digital loopback, write 0016 to 0004
// for PCS loopback, write 0016 to 0003
// (3)
// for packet generation with digital loopback, write 0016 to 5004
// for packet generation with PCS loopback, write 0016 to 5003
end
```

Reference the annotated (1-3) register writes if testing in different loopback modes or speeds.
Wait at least one second before the following reads/writes to allow for PRBS to transmit packets.

```
begin
// lock byte count
0072 0201
// check lock status, # of packets received, and # of errors
0017
0071
0072
// enable continuous mode packet counting
0016 D004
// update packet counter with current value (4)
0072 0201
// read packet counter (5)
0071
// soft reset
001F 4000
// Repeat (4) and (5) as desired to verify packet count changing for each counter update
end
```

Register 0x17[11] indicates whether PRBS was able to successfully receive the same transmitted data through the given data path.

3.7 Debugging MAC Interface

Reference the waveforms in this section verify the expected MAC data and clock signals for RGMII in shift and align modes. To capture data and clock signals, measure close to the receiver end. Note the following requirements for selecting the correct delay mode:

Table 3-7. Selecting the Correct RGMII Delay Mode

If MAC's Configuration is:	Required PHY Configuration
RGMII Align Mode on TX side	RGMII Shift Mode on TX side
RGMII Align Mode on RX side	RGMII Shift Mode on RX side
RGMII Shift Mode on TX side	RGMII Align Mode on TX side
RGMII Shift Mode on RX side	RGMII Align Mode on RX side

RX_D[3:0] Data Aligned with RX_CLK

For the PHY set in RX align mode in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the reference waveforms shown below:
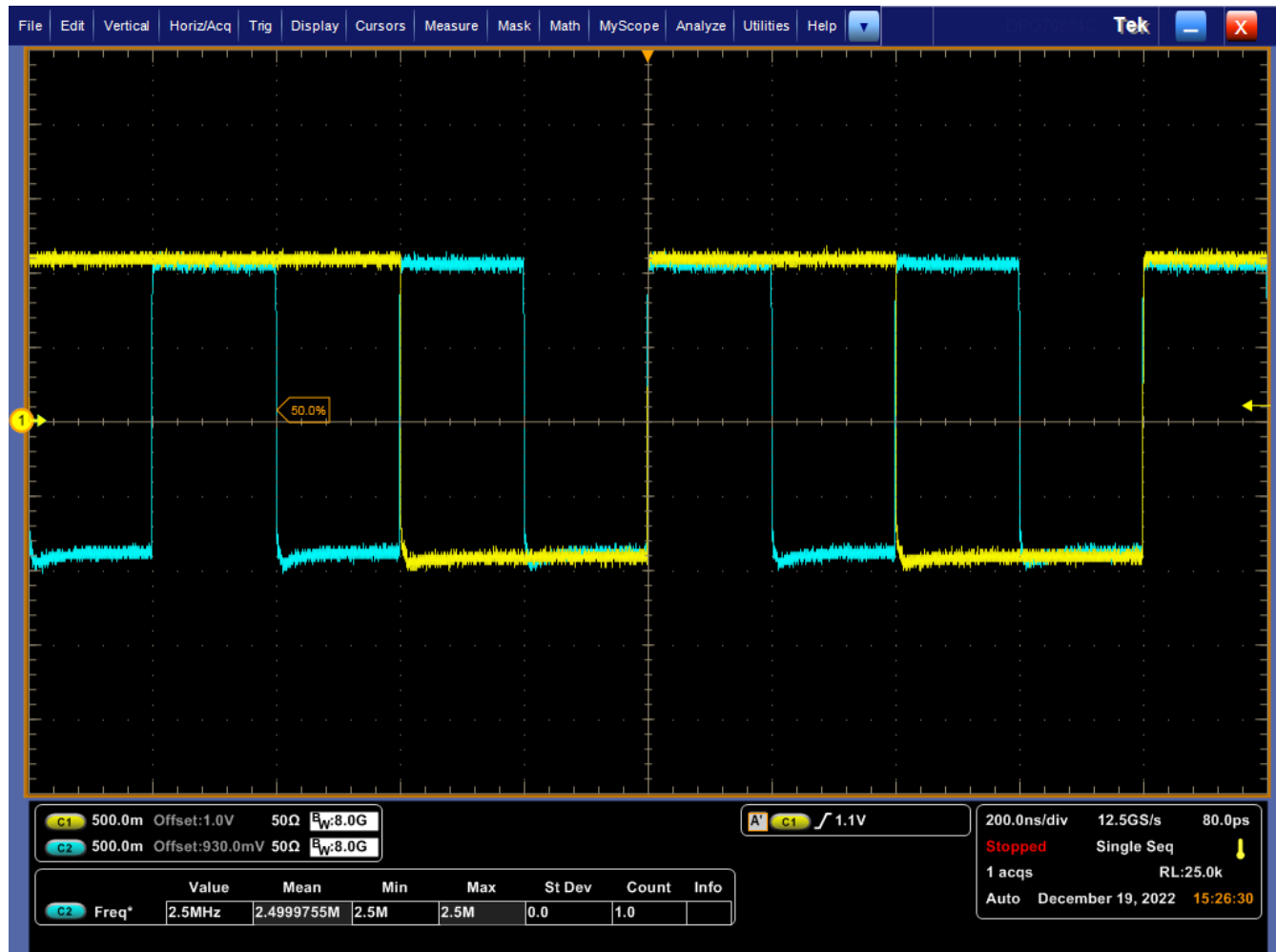

Figure 3-10. 10 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 2.5MHz, and the data (C1) being sampled at the rising edge of the clock.
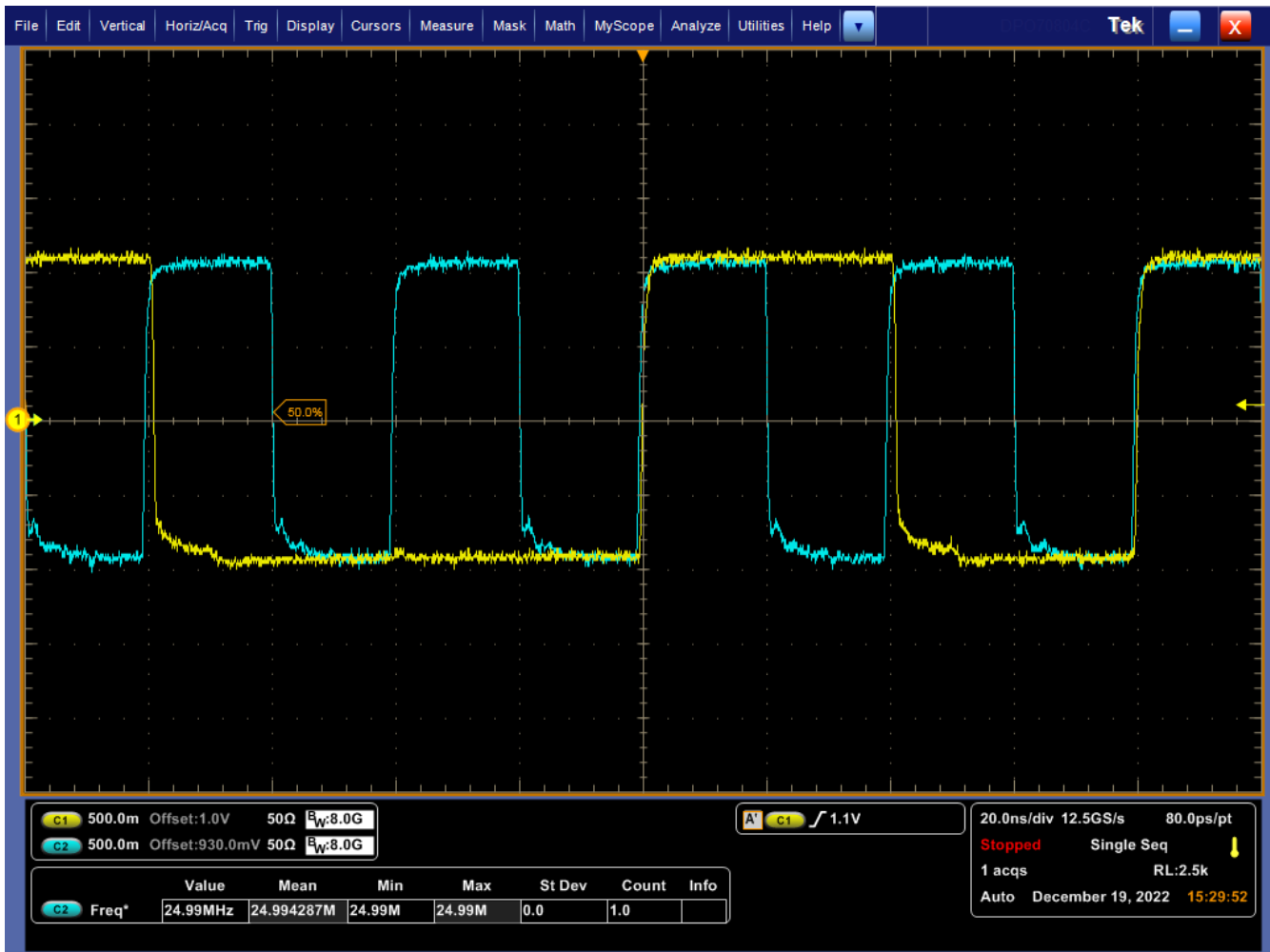
Figure 3-11. 100 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 25MHz, and the data (C1) being sampled at the rising edge of the clock.
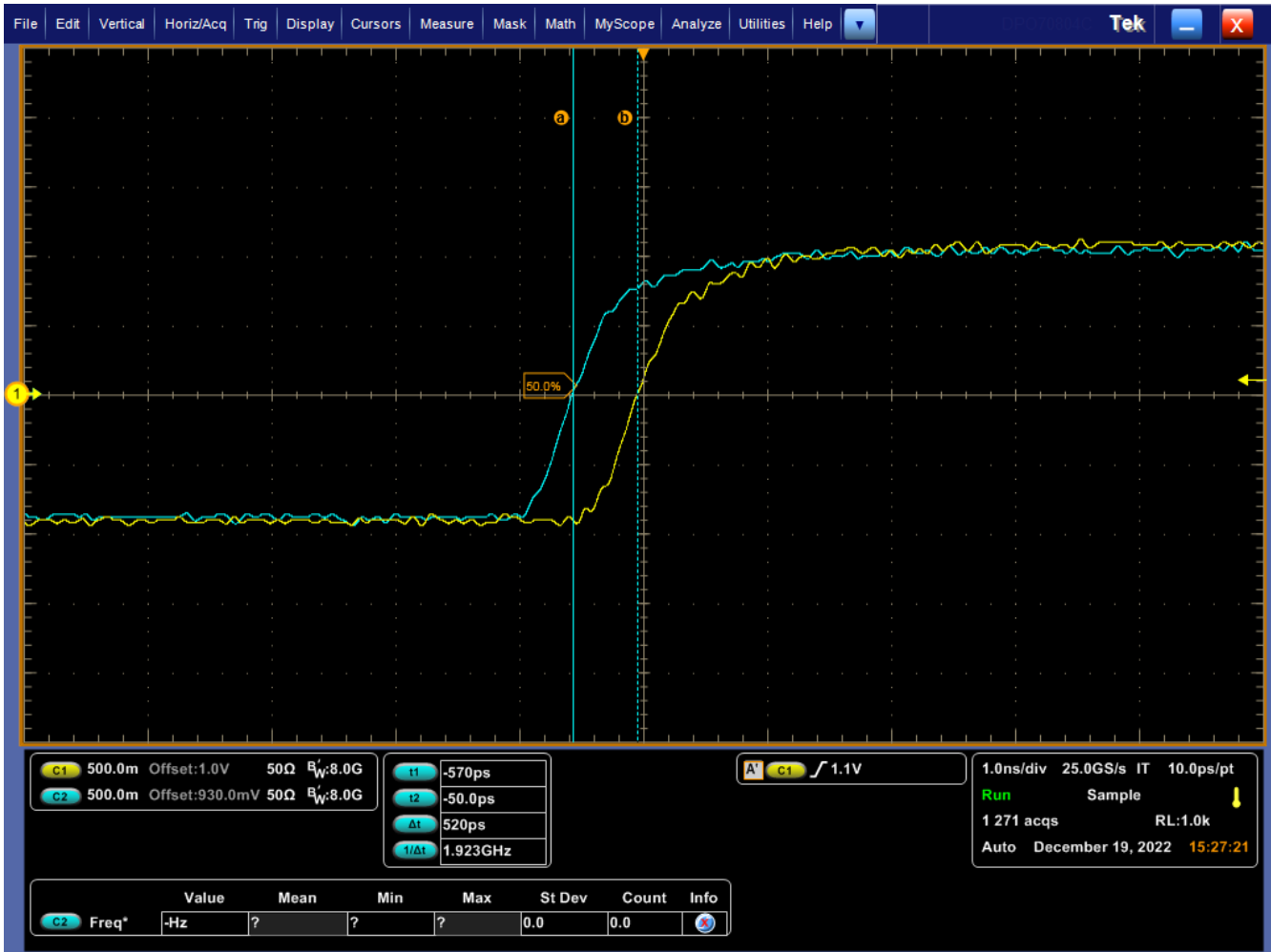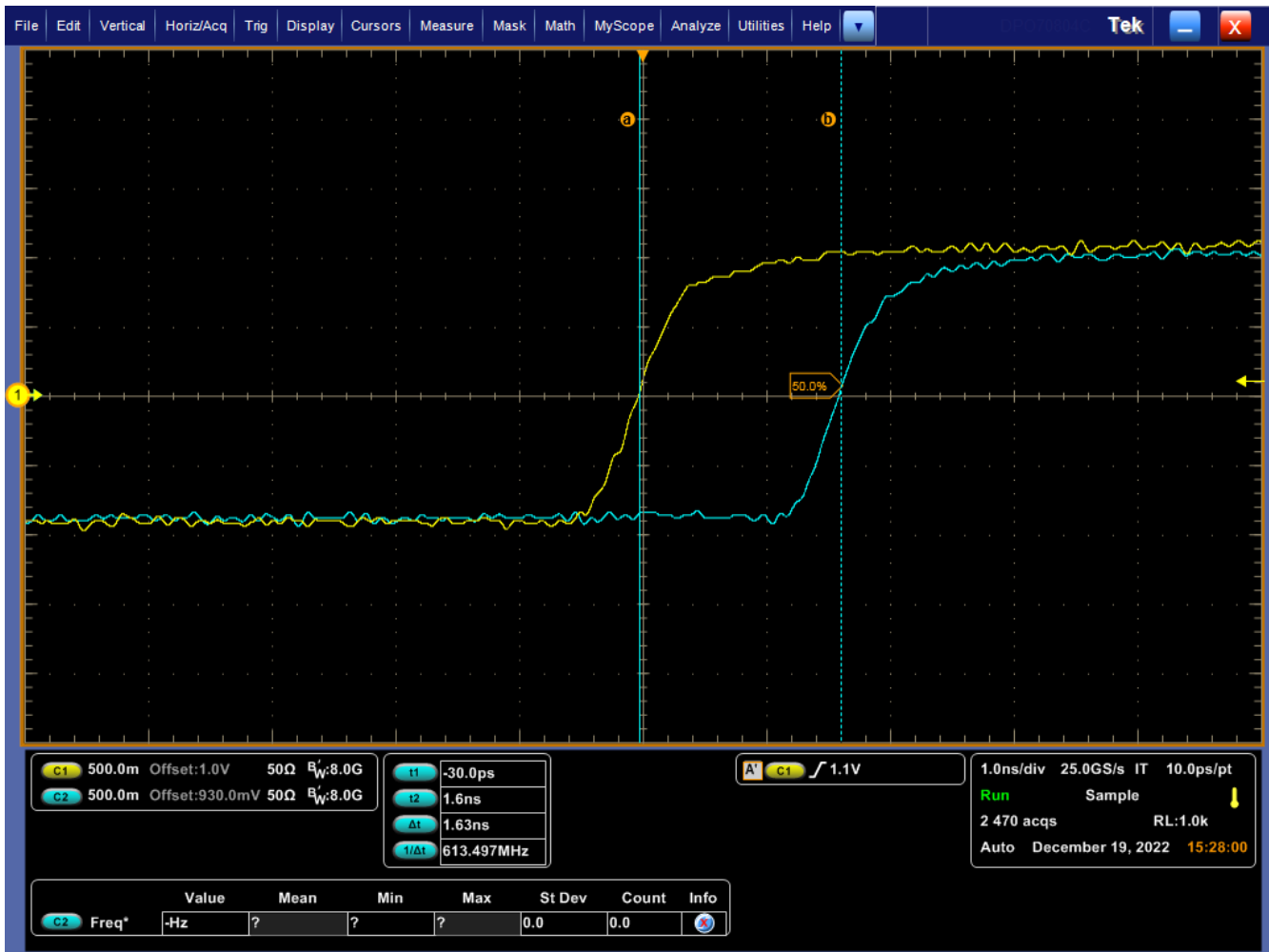
Figure 3-12. 10Mbps Data and Clock Delay in Align Mode

Verify the delay between clock and data is <500ps in align mode.

RX_D[3:0] Data and RX_CLK in Shift Mode

For the PHY set in RX shift mode (0x32) in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the following reference waveforms.

Figure 3-13. 10 Mbps Data and RX_CLK in Shift Mode (4ns Programmed Delay)

Verify the delay between clock and data is >1ns in shift mode. The programmed delay is relative to the clock's initial position in aligned mode. Measuring the difference in the clock's position before and after setting shift mode yields a value closer to the programmed delay.

TX_D[3:0] and TX_CLK in Shift and Align Mode

For the PHY set in TX shift or align mode, probe the data and clock signals on the PHY end and verify the timing requirements below are met:

PARAMETER		MIN	NOM	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	−500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
T_{setupT}	Data to Clock output Setup (at Transmitter – internal delay)	1.2	2		ns
T_{holdT}	Clock to Data output Hold (at Transmitter – internal delay)	1.2	2		ns
T_{setupR}	Data to Clock input Setup (at Reciever – internal delay)	1	2		ns
T_{holdR}	Clock to Data input Hold (at Receiver – internal delay)	1	2		ns

PARAMETER		MIN	NOM	MAX	UNIT
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55%	
Duty_T	Duty Cycle for 10/100T	40	50	60%	
T_R	Rise Time (20% to 80%)			0.75	ns
T_F	Fall Time (20% to 80%)			0.75	ns

3.8 Application Specific Debugs

Improving Link-up Margins for Short Cables:

If you are encountering an issue with packet loss or CRC errors while using the DP83867, please consider some of these items for debug when using short cables.

Short cables at 1m or less in length for your device may experience signal quality issues. One reason could be that the digital signal processing internally may take too long to converge or may converge to suboptimal filter values at shorter lengths which could result to a bad SNR - Signal to Noise Ratio. This then creates link dropping or potential packet losses which may require you to reset your device before beginning packet transfer again.

We have a register configuration below that can improve the SNR in applications where this marginality is observed. This script allows for a change in the timing bandwidths to ensure the DSP converges correctly:

```
begin
// Hard Reset
001F 8000
// Threshold for consecutive amount of Idle symbols for Viterbi Idle detector to assert Idle Mode
set to 5
0053 2054
// CAGC DC Compensation Disable
00EF 3840
// Master Training Timers - increasing time in different training states
0102 7477
// Master Training Timers - increasing time in different training states
0103 7777
// Master Training Timers - increasing time in different training states
0104 4577
// Timing Loop Bandwidth
010C 7777
// Timing Loop Bandwidth
01C2 7FDE
// Slave Timers - increasing time in different training states
0115 5555
// Slave Timers - increasing time in different training states
0118 0771
// Timing Loop Bandwidth
011D 6DB2
// Timing Loop Bandwidth
011E 3FFB
// Timing Loop Bandwidth
01C3 FFC6
// Timing Loop Bandwidth
01C4 0FC2
// Timing Loop Bandwidth
01C5 0FF0
// FFE Fix
012C 0E81
// Soft Reset
001F 4000
end
```

Improving Link Margins across Different Channels

The DP83867 uses an AGC gain convergence circuit (automatic gain control of MDI receiver) to provide faster linkup. There is a tradeoff between the linkup time and gain mismatch between pairs. In applications where

packet errors are observed, gain matching can be improved for more optimal link by increasing the gain convergence time with the following register writes:

```
begin
// Hard reset
001F 8000
// Increase time for AGC
0102 7477
// No AGC Re-train
00E4 0080
// Soft reset
001F 4000
end
```

3.9 Tools and References

The following chapter contains additional tools and references relevant for debugs.

3.9.1 DP83867 Register Access

If register access is not readily available in the application, USB-2-MDIO GUI is available from TI and can be used with an MSP430 Launchpad, purchasable through the TI eStore (https://store.ti.com/). The GUI supports reading and writing registers as well as running script files. It can be used with the DP83867 and the other devices in TI's Ethernet portfolio. The USB-2-MDIO User's Guide and GUI are available for download at: http://www.ti.com/tool/usb-2-mdio
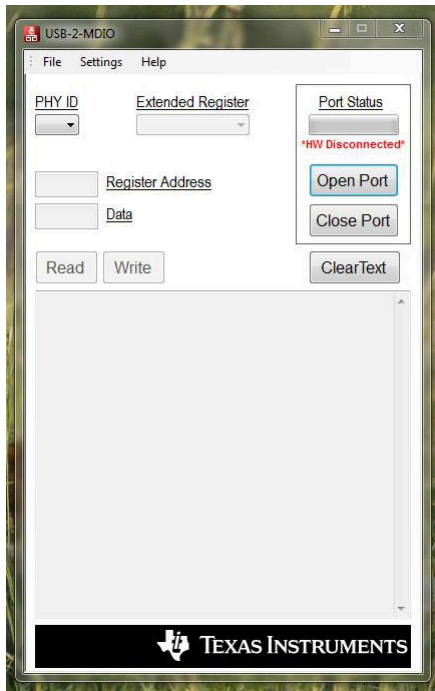
Figure 3-14. USB-2-MDIO GUI
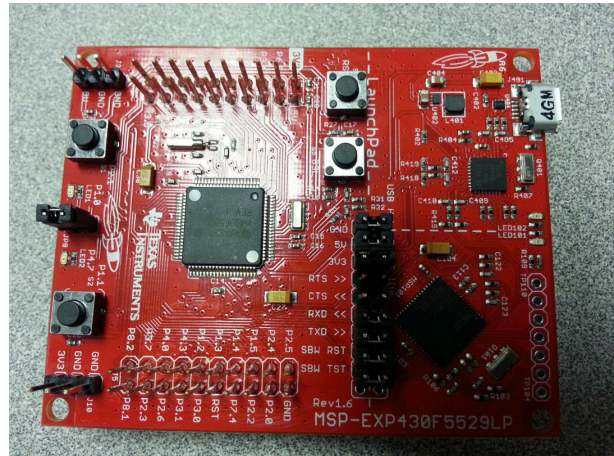
Figure 3-15. MSP430 LaunchPad

Below is an example script that can also be found in the USB-2-MDIO GUI in the Help menu:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// To read a register, all you need to do is put down the 4 digit
// HEX value of the registers (from 0000 to FFFF)
// Example to read registers 0001, 000A, and 0017
0001
000A
0017
// To write a register, all you need to do is put down the 4 digit
// HEX value of the register (from 0000 to FFFF) followed by the
// HEX you desire to configure the register to (from 0000 to FFFF)
// Example to write 2100 to register 0000 and
// Example to write 0110 to register 0016
0000 2100
0016 0110
// You must end the script by adding 'end' once you are finished
end
```

The Serial Management Interface defined by IEEE 802.3 is a single master bus. The MDC clock is generated by the bus master, typically an Ethernet MAC. To use the USB-2-MDIO GUI, connections must be made directly between the MSP430 Launchpad and the DP83867 MDIO and MDC pins. Specifically, pins 4.1 to MDC, 4.2 to MDIO, and any GND to the ground of the PHY will allow the MSP to read and write the PHY's registers via USB-2-MDIO.

3.9.2 Extended Register Access

To read and write registers in extended register space, refer to the following procedure:

Write procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

write reg<000E> = <value>

Read procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

read reg<000E>

Note : To read/write MMD "1" registers, replace 1F with 01.

Note : Above write and read procedure is normally used for registers with address greater than 0x001F. But it can also be used for any address in general.

3.9.3 Application Note References

Refer to the following application notes for information on hardware and software configurations for EMC/EMI compliance tests:

How to Pass IEEE Ethernet Compliance Tests

How to Configure DP838xx for Ethernet Compliance Testing

4 Conclusion

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations will help ease board bring up and initial evaluation of DP83867 designs.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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