KSZ8081MNX/RNB to DP83826 System Rollover

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ABSTRACT

This application report outlines the necessary and potential steps for replacing the Microchip KSZ8081MNX/RNB 10/100 Mb/s Ethernet PHY with TI's DP83826.

Contents

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1 Purpose

While the KSZ8081MNX/RNB and the DP83826 have many similarities, several features are included in the DP83826, improving performance and system optimization. This system rollover document outlines how to replace the Microchip KSZ8081MNX/RNB PHY with TI's DP83826 by comparing differences including required external components, pin functions, feature set, and register operation. The impact to a design is dependent on PHY configuration and features used.

2 Required Changes

This section describes the modifications required to transition from the KSZ8081MNX/RNB to the DP83826.

2.1 External Capacitor on Pin 2

The KSZ8081 requires two external decoupling capacitors on pin 2; 2.2uF and 0.1uF. The DP83826 only requires one external decoupling capacitor on pin 2 (CEXT); 2nF.

Table 1. Value of External Capacitor(s) on Pin 2

	DP83826	KSZ8081MNX/RNB
External Capacitor Value	2 nF	2.2 µF and 0.1 µF

2.2 Strap Resistor Value

The DP83826 supports either BASIC Mode or ENHANCED Mode. BASIC Mode supports the same bootstrap options as the KSZ8081. To set the DP83826 for BASIC Mode, pin 1, ModeSelect, must be tied to ground. In a KSZ8081 design, Pin 1 is already tied to GND so there is no change needed to select the correct mode. To understand the difference between DP83826 BASIC Mode and ENHANCED Mode, refer to the DP83826 Datasheet.

Both devices use a 2-level strap that may require a pull-up or pull-down resistor. The table below shows the difference in pull-up and pull-down resistor values between the DP83826 and the KSZ8081. Refer to the TI Precision Labs Video 'How Do Ethernet bootstraps work?' to properly calculate the correct strap resistors.

Table 2. Strap Resistor Values

	DP83826	KSZ8081MNX/RNB
Pull-Up Resistor Value	2.49 kΩ	4.7 kΩ
Pull-Down Resistor Value	2.49 kΩ	1.0 kΩ

For specific strap options, please refer to the Appendix of this Application Note.

2.3 Duplex Strap on Pin 16 (DP83826 Basic Mode)

- ❑ If using the KSZ8081 in Half-Duplex, populate a pull-down resistor on pin 16 when using the DP83826. If using the KSZ8081 in Full-Duplex, remove the pull-down resistor on Pin 16 when using the DP83826.

Table 3. Full/Half Duplex Comparison

Pin NO.	DP83826 Basic Mode	KSZ8081MNX/RNB
Pin 16	1: Full Duplex (Default) 0: Half Duplex	1: Half Duplex (Default) 0: Full Duplex

2.4 Speed Strap on Pin 31

Pin 31 on the KSZ8081 functions as LED1 by default. DP83826 in Basic Mode configures Pin 31 as TX_ER by default. Configuring Pin 31 to LED1 on the DP83826 requires a simple register change.

- ❑ Write 0x0008 to register 0x0304

2.5 Selecting 10M with Auto-Negotiation Enabled (DP83826 Basic Mode)

KSZ8081MNX and DP83826 default to 100M speed. To select 10M speed, KSZ8081 recommends a pull down on the strap along with a series resistor on LED. For DP83826 Basic Mode, 10M speed selection is done through register configuration and the strap resistor on Pin 31 shall be removed.

- ❑ Remove the strap resistor on Pin 31 for 10M selection
- ❑ Program register 0x0004 with 0x0061 to select 10M speed when Auto-Negotiation is enabled
- ❑ Program register 0x0000 with 0x3300 to restart Auto-Negotiation

2.6 Configuring LED_1 for Tx and Rx Activity for EtherCAT Slave (DP83826 Basic Mode)

The DP83826 and KSZ8081MNX/RNB can use LED_1 to indicate Tx and Rx activity from a host ASIC or FPGA. Extended register configurations are required for DP83826.

- ❑ Program register 0x0304 with 0x0008
- ❑ Program register 0x0460 with 0x0001 for the LED to stay high OR register 0x0460 with 0x0008 for a blinking LED

2.7 Physical Layer ID Register

The PHY Identifier Register #1 (PHYIDR1) and #2 (PHYIDR2) allow system software to determine applicability of device specific software based on the vendor model number. The Identifiers Register #1 and Register #2 can be found in sections 9.5.3 and 9.5.4 of the DP83826 Datasheet. The vendor model number is represented by bits 9 to 4 in PHYIDR2 (Address 0x3) outlined below.

Table 4. PHYID Comparison

Register Address	Register Name	Register Description	Device	
			DP83826	KSZ8081MNX/RNB
0x03	PHYIDR2	PHY ID 2	0x010001b - BASIC 0x010011b - ENHANCED	0x010110b

3 Potential Changes

The following section describes the specific changes that may need to be changed in converting to a DP83826 design. The default values for the DP83826 vs. KSZ8081MNX/RNB may be enough for transition between parts.

3.1 MDIO Pull-Up Resistor on Pin 11

KSZ8081 requires an external pull-up resistor on the MDIO pin of the PHY. This pin on DP83826 has an internal pull-up resistor of 10 kΩ. An additional external pullup resistor can be added if necessary.

3.2 MDIO Register Writes

The DP83826 and KSZ8081MNX/RNB have both standard and extended SMI/MIIM (MDIO) registers.

DP83826 can access the standard registers through the indirect method (using standard registers 0x000D and 0x000E as outline in IEEE 802.3). However, Microchip KSZ8081MNX/RNB can only access the standard register set through the direct method (without using 0x000D and 0x000E registers).

KSZ8081MNX/RNB also specifies the MMD address for all extended registers (for example “2 h”) while DP83826 only uses MMD address 31 (0x001F) for all extended register writes and reads.

3.3 Capacitors on Center Tap of Magnetics

KSZ8081MNX/RNB and DP83826 can use one 0.1uF capacitor on each center tap of magnetics if needed.

4 Informational Changes

This section describes feature differences between the DP83826 and KSZ8081.

Table 5. DP83826 vs. KSZ8081MNX/RNB Feature Set Comparison

Features	DP83826	KSZ8081MNX/RNB
VDDIO	1.8V, 3.3V	1.8V, 2.5V, 3.3V
NAND Tree Support	Not Supported	Supported
PHY Broadcast Address	Not Supported	Supported
MII Back-2-Back Mode	Supported in ENHANCED Mode for Repeater Functionality	Supported
Slow Oscillator Mode	Supported - known as Deep Power Down Mode	Supported

Pinout Mapping

A.1

The table below shows the pinout mapping between the DP83826 and KSZ8081MNX/RNB. For more details on the pin mapping as well as any updates made, please refer to the DP83826 Datasheet.

Table 6. Pinout Mapping

Pin No.	DP83826 BASIC Mode Pin Functions	KSZ8081MNX/RNB Pin Functions	DP83826 ENHANCED Mode Pin Functions
1	Mode Select	GND	Mode Select
2	CEXT	VDD_1.2	CEXT
3	VDDA3V3	VDDA_3.3	VDDA3V3
4	RD_M	RXM	RD_M
5	RD_P	RXP	RD_P
6	TD_M	TXM	TD_M
7	TD_P	TXP	TD_P
8	XO	XO	XO
9	XI/50MHzIn	XI	XI/50MHzIn
10	RBIAS	REXT	RBIAS
11	MDIO	MDIO	MDIO
12	MDC	MDC	MDC
13	RX_D3	PHYAD0 (RXD3)	RX_D3
14	RX_D2	PHYAD1 (RXD2)	RX_D2
15	RX_D1	RXD1/ PHYAD2	RX_D1
16	RX_D0	RXD0/ DUPLEX	RX_D0
17	VDDIO	VDDIO	VDDIO
18	RX_DV/CRS _DV	RXDV/ CONFIG2	RX_DV/CRS _DV
19	RX_CLK/50 MHz_Output	RXC/ B-CAST_OFF	RX_CLK/50 MHz_RMII
20	RX_ER	RXER/ ISO	RX_ER
21	INT	INTRP/ NAND_Tree#	PWRDN/INT
22	TX_CLK	TXC	TX_CLK
23	TX_EN	TXEN	TX_EN
24	TX_D0	TXD0	TX_D0
25	TX_D1	TXD1	TX_D1
26	TX_D2	TXD2	TX_D2
27	TX_D3	TXD3	TX_D3
28	COL	COL/ CONFIG0	COL/LED2/GPIO
29	CRS	CRS/ CONFIG1	CRS/LED3
30	LED0	LED0/ NWAYEN I	LED0
31	TX_ER/LED1	LED1/ SPEED	TX_ER/LED1
32	RST_N	RST#	RST_N

DP83826 Strap Configurations

B.1 Bootstrap Configurations

The tables below outline the DP83826 strap configurations in BASIC Mode. Unless stated otherwise in the previous subsections, the KSZ8081MNX/RNB strap configurations are analogous. This table and more details about the bootstrap configurations can be found in the DP83826 Datasheet.

Table 7. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D3	Strap7	13	1		PHY_ADD0
				0	0
				1	1
RX_D2	Strap8	14	0		PHY_ADD1
				0	0
				1	1
RX_D1	Strap9	15	0		PHY_ADD2
				0	0
				1	1

Table 8. MAC Mode Selection Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Strap 10	Strap 3	Strap4	Function
COL	Strap4	28	0	0	0	0	MII MAC Mode
				0	0	1	RMII Master Mode
				1	0	1	RMII Slave Mode
CRS	Strap3	29	0	Reserved			
RX_DV	Strap10	18	0				

Table 9. Auto Negotiation Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
LED0	Strap2	30	1	0	Auto Negotiation Disable
				1	Auto Negotiation Enable

Table 10. Speed Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
TX_ER/LED1	Strap1	31	1	0	Speed 10M
				1	Speed 100M

Table 11. Full/Half Duplex Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_D0	Strap0	16	1	0	Half Duplex
				1	Full Duplex

Table 12. MII Isolate Bootstraps

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	Mode	Function
RX_ER	Strap6	20	0	0	MII Isolate Disable
				1	MII Isolate Enable

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