Application Note

Wake-Up Circuit Design Guidelines

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ABSTRACT

A Wake-Up Circuit is an external circuit that can be applied to an FPD-Link channel to transmit a DC wake-up signal over an existing cable link. The DC wake-up signal can be used to power on a remote module, such as a display system, before active video transmission. This document discusses the design guidelines for implementing a Wake-Up Circuit across a cable link between Texas Instruments FPD-Link serializer and deserializer devices.

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1 Introduction

FPD-Link products generate a bidirectional control channel with a signal bandwidth from the MHz range to the GHz range between the paired serializer and deserializer devices. An external DC voltage can be applied to the channel and transmitted across the cable link as part of a wake-up command to a remote target device. A Wake-Up Circuit design implemented on the serializer and deserializer portion of the total channel link can allow for an external DC signal to be transmitted while minimizing interference in the bidirectional control channel. This document provides guidance on how to implement the serializer portion and the deserializer portion of the overall Wake-Up Circuit design in a system.

2 Wake-Up Circuit

A Wake-Up Circuit consists of two parts. There is an input circuit (WAKE_IN) implemented on the PCB that transmits the wake-up signal over the cable link. There is also an output circuit (WAKE_OUT) on the PCB that receives the wake-up signal to power on a target system.

The DC wake-up signal is expected to be sent when the FPD-Link channel is inactive and to be held constant during the operation of the FPD-Link devices. The wake-up signal can be brought LOW to power down the target system. Avoid toggling the wake-up signal during active FPD-Link transmission to prevent interference on the high speed channel link.

Refer to Section 3 for more details on the circuit implementation.

2.1 Wake-Up Input Circuit (WAKE_IN)

The purpose of the Wake-Up Input Circuit (WAKE_IN) is to allow a processor to control when a DC wake-signal can be transmitted over the cable link. This circuit typically consists of a load switch with its enable pin controlled by a processor's GPIO pin (WAKE_CTRL). A 2.15kΩ resistor is used to connect the WAKE_IN circuit to the FPD-Link channel to isolate the DC signal path from the high speed signal path. The load switch can output a stable and low-noise DC voltage onto the FPD-Link channel once the processor enables the switch.

Load switch component selection depends on the needs of the customer system. Load switch devices can include a variety of additional features, such as an internal soft-start circuit to adjust the rise time of the outputted DC wake-up signal or a quick output discharge (QOD) pin to prevent a floating output.

Refer to *Basics of Load Switches*, application note for support in choosing a load switch component. Also refer to the load switch data sheet for the recommended circuit implementation, which includes the number of load capacitors (C_L) and resistive loads (R_L) on the load switch output.

2.2 Wake-Up Output Circuit (WAKE_OUT)

The purpose of the Wake-Up Output Circuit (WAKE_OUT) is to make sure that the received wake-up signal is at the desired DC voltage level and is capable of driving the receiving device. This circuit typically consists of a pull-down resistor (R_{WAKE}) that sets the received voltage of the wake-up signal at the WAKE_OUT circuit, capacitors (C_{OUT}) for stable voltage, a zener diode for protection against over voltage, a current limiting series resistor (R_{SERIES}), and a voltage clamp circuit.

The resistors in the overall Wake-Up Circuit form a voltage divider that result in a WAKE_OUT voltage that is lower than the WAKE_IN voltage. The R_{WAKE} resistor can be 1% tolerance and the resistor value can be adjusted to change the WAKE_OUT voltage.

V_{CLAMP} is the clamp voltage applied to an optional voltage clamp circuit consisting of Schottky diodes that clamps the received WAKE_OUT voltage within a specific DC voltage range and protects against transient events, such as ESD strikes. The upper diode can turn on when the diode forward voltage ($V_{FORWARD-UPPER}$) is met. This limits the upper range of the received WAKE_OUT voltage to be (V_{CLAMP} + $V_{FORWARD-UPPER}$). The lower diode can turn on when the WAKE_OUT voltage is negative and the diode's forward voltage ($V_{FORWARD-LOWER}$) is met. This limits the lower range of the received WAKE_OUT voltage to be (GND - $V_{FORWARD-LOWER}$).

R_{SERIES} is an optional series resistor that limits the current draw from WAKE_OUT. This resistor is part of the voltage clamp circuit and is meant to protect the clamp diodes by limiting the current draw to be within the component's rated current specifications.

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If WAKE_OUT is being used to drive a BJT circuit, then an additional base resistor (R_{BASE}) is recommended to be added after the clamp circuit and before the BJT circuit. R_{BASE} is calculated based on the BJT circuit used. The recommendation is to use WAKE_OUT and a BJT circuit to drive a receiving device, due to the limited drive strength of the wake-up signal.

TINA-TI is a simulation software that can be used to recreate the Wake-Up Circuit and determine the appropriate R_{WAKE} resistor value for the system, based on the desired WAKE_IN and WAKE_OUT voltages.

2.3 Capacitor Considerations

FPD-Link devices require AC coupling capacitors along the DOUT± and RIN± paths. Select components that meet the required temperature rating and tolerance of the system. Refer to the FPD-Link device data sheet for the required capacitance value.

When a DC voltage is applied to a capacitor, the capacitance can derate by a substantial amount. A general guideline is to choose a capacitor component that has a voltage rating 2 or 3 times higher than the DC voltage expected to be applied to the component. Then, check the manufacturer's website to verify the component's DC Bias Characteristics. Derating characteristics are typically not available in the capacitor's data sheet. The recommendation is to choose a component that has a maximum of 20% derating when the expected DC voltage is applied.

3 Wake-Up Circuit Typical Implementation

The following section describes the general Wake-Up circuit implementations in a coaxial and shielded twisted pair connection between FPD-Link devices.

3.1 Coaxial (COAX) Implementation

In a coaxial link between the paired FPD-Link devices, the DOUT+/RIN+ pins on the serializer/deserializer devices are connected through PCB traces and a coaxial cable. The DOUT-/RIN- pins are terminated to GND through a 50-Ohms resistor. In this configuration, a wake-up signal can be transmitted in one direction on the channel. See Figure 3-1 for an example of a typical system implementation.

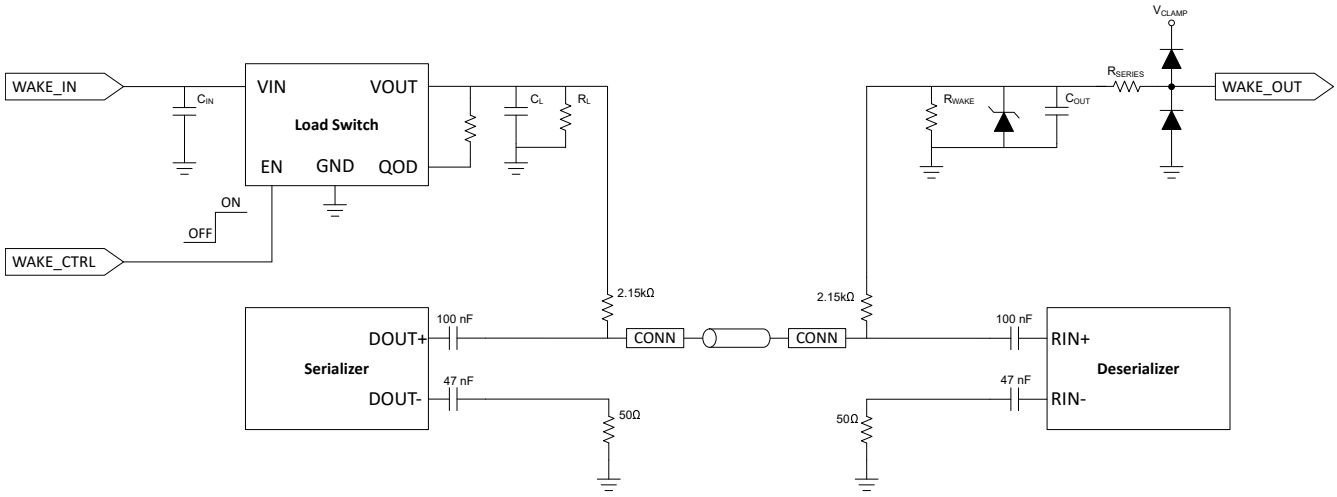

Figure 3-1. Wake-Up Circuit COAX Implementation

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3.2 Shielded Twisted Pair (STP) Implementation

In a shielded twisted pair link between the paired FPD-Link devices, the DOUT+/RIN+ pins and DOUT-/RIN- pins on the serializer or deserializer devices are connected through PCB traces and a STP cable. In this configuration, a wake-up signal can be transmitted in two directions on the channel. See Figure 3-2 for an example of a typical system implementation.

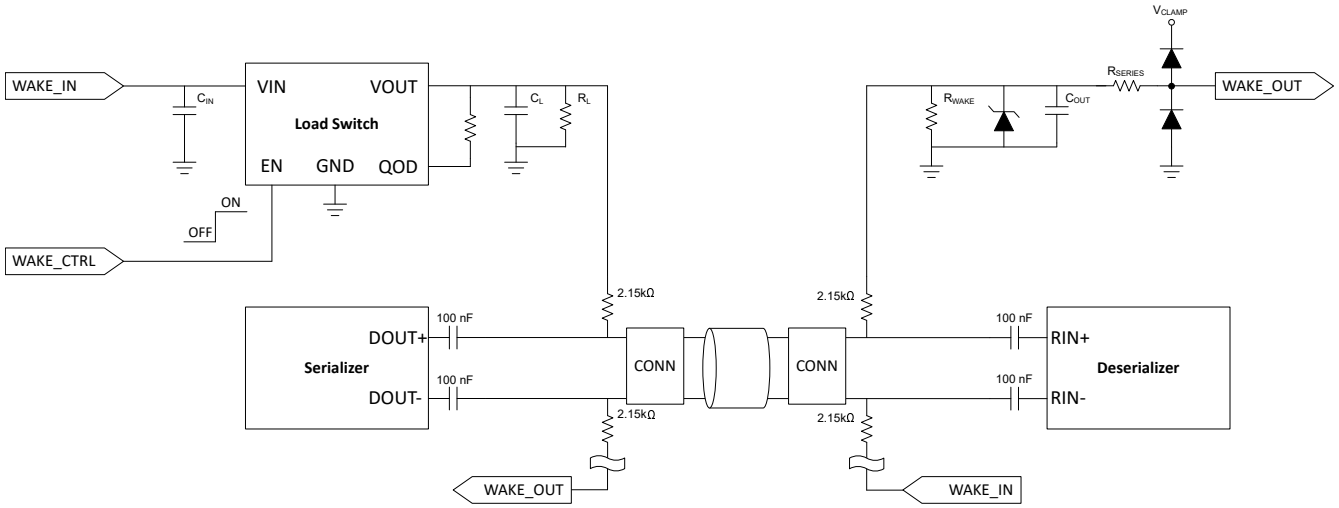

Figure 3-2. Wake-Up Circuit STP Implementation

TI recommends to keep the 2.15kΩ resistors populated on both the DOUT± and RIN± traces. If only one signal side (P or N) is used, then the 2.15kΩ resistors on the unused side can be terminated to ground. This process is done to keep the differential line balanced for noise rejection at the FPD-Link differential receiver.

4 Implementation Example

This section describes a Wake-Up Circuit implementation example between a DS90Ux981-Q1 and DS90Ux984-Q1 system.

4.1 Wake-Up Circuit Simulation

Simulations were performed in Keysight Advanced Design System (ADS), using the IBIS-AMI models of the DS90UH981-Q1 and DS90UH984-Q1 devices and S-Parameter files of PCB traces and a 5-meter cable, to evaluate the effects of the Wake-Up Circuit on the FPD-Link Eye Height and Eye Width. See Figure 4-1 for the schematic simulated in ADS.

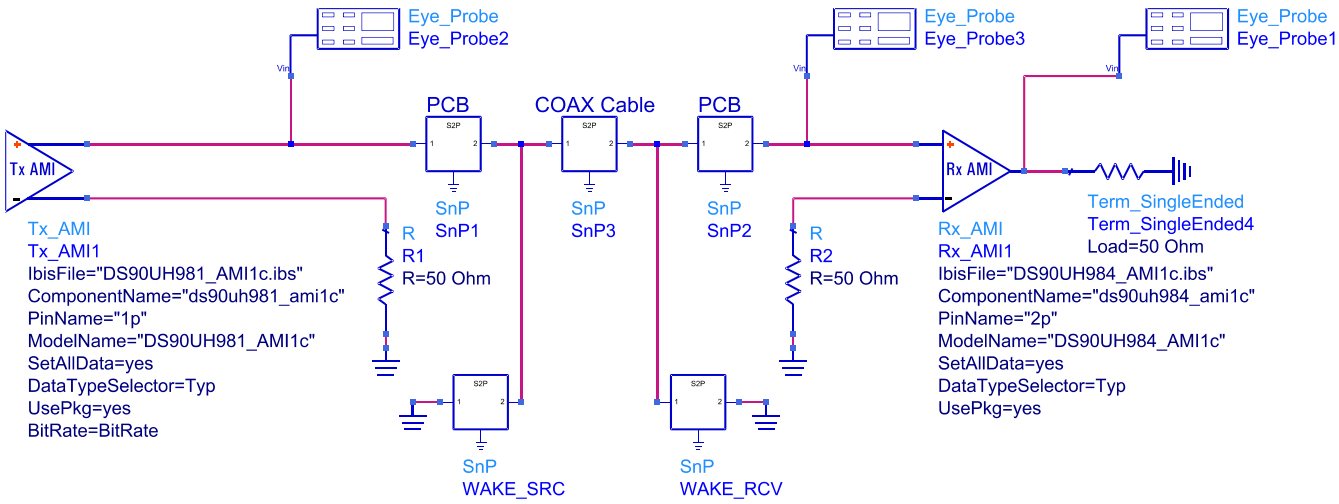

Figure 4-1. ADS Wake-Up Circuit Schematic

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Simulated Eye plots were generated with and without the WAKE_SRC and WAKE_RCV components in the schematic connected along the PCB path. The results show that the inclusion of the Wake-Up Circuit has minimal impact on the signal integrity of the FPD-Link channel. Eye Height and Eye Width are comparable in both test cases. Figure 4-2, Figure 4-3, and Figure 4-4 show the Eye plots simulated at data rates of 6.75Gbps, 10.8Gbps, and 13.5Gbps. Table 4-1 compares the Eye Height and Eye Width of the Eye plots with and without the Wake-Up Circuit.

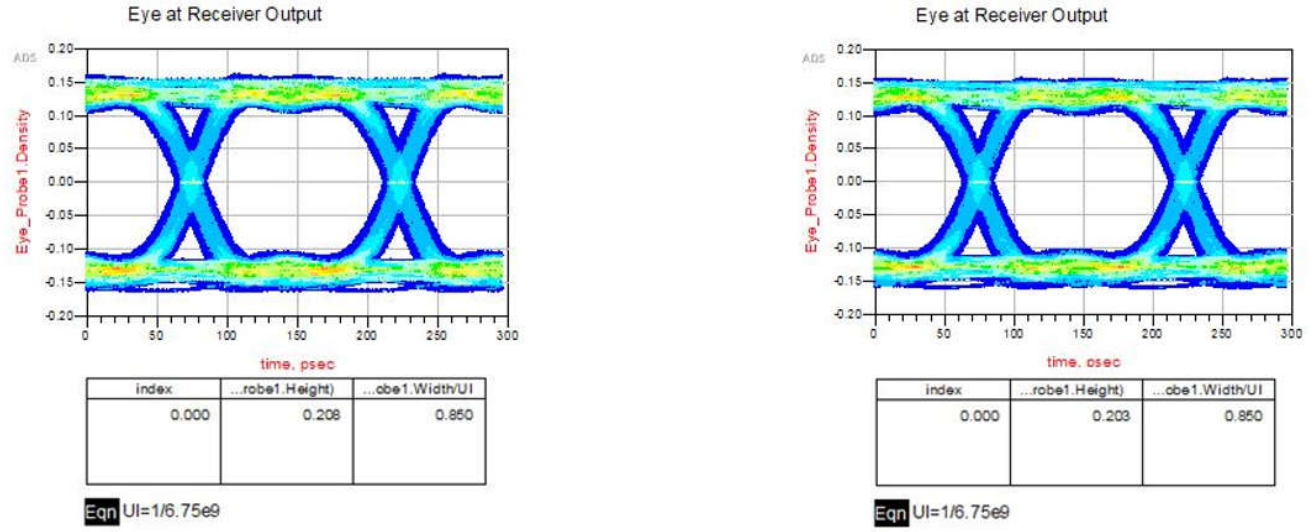

Figure 4-2. ADS Simulated Eye Plot With and Without the Wake-Up Circuit (6.75Gbps)

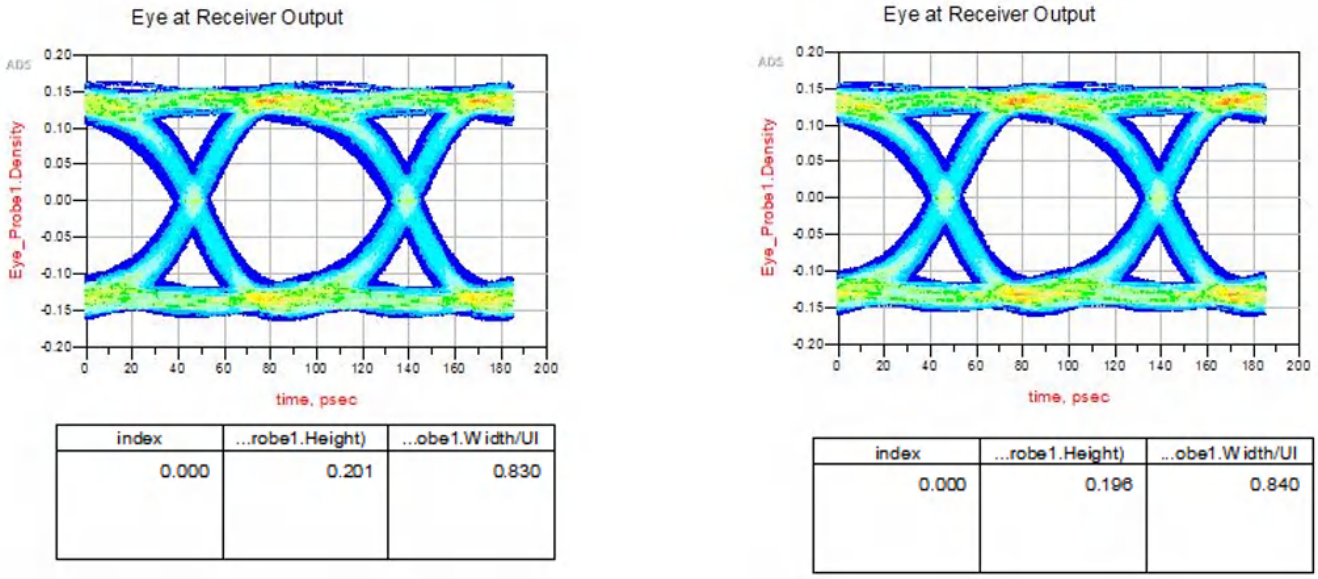

Figure 4-3. ADS Simulated Eye Plot With and Without the Wake-Up Circuit (10.8Gbps)

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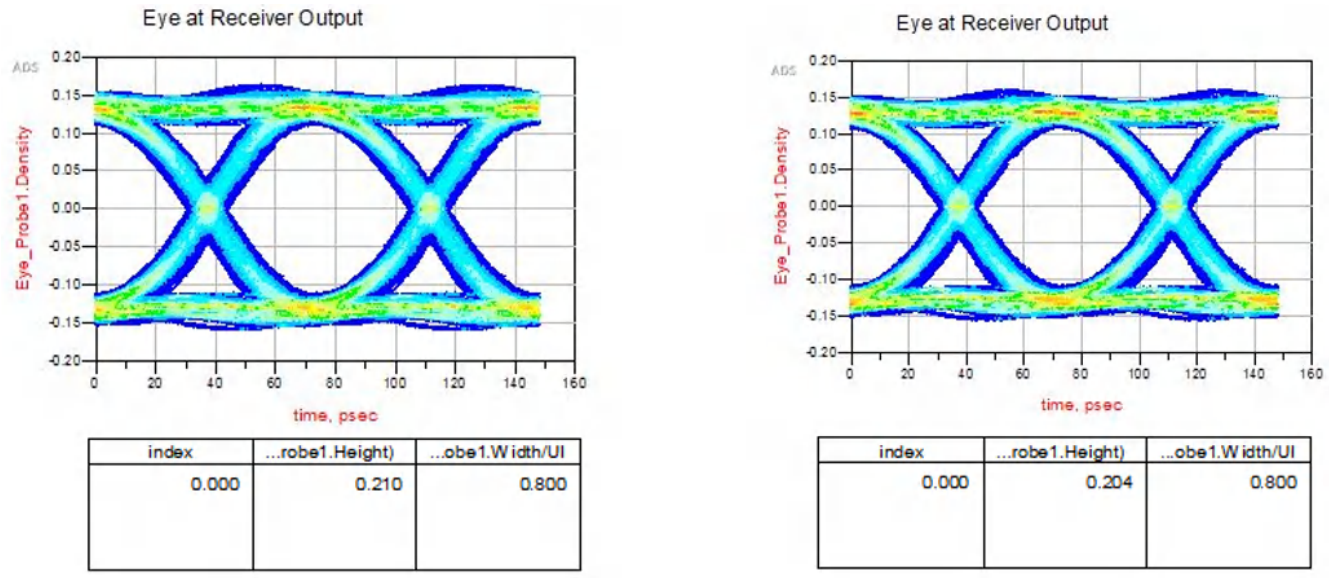

Figure 4-4. ADS Simulated Eye Plot With and Without the Wake-Up Circuit (13.5Gbps)

Table 4-1. Comparison of Simulated Eye Plots With and Without Wake-Up Circuit

Data Rate	Eye Height WITHOUT Wake-Up Circuit	Eye Height WITH Wake-Up Circuit	Eye Width WITHOUT Wake-Up Circuit	Eye Width WITH Wake-Up Circuit
6.75Gbps	0.208	0.203	0.850	0.850
10.8Gbps	0.201	0.196	0.830	0.840
13.5Gbps	0.210	0.204	0.800	0.800

Figure 4-5 demonstrates a Wake-Up Circuit schematic simulated in TINA-TI. A 5V WAKE_IN signal is inputted into the transmission line on the serializer PCB through a 2.15kΩ resistor and sent over an FPD-Link channel link. R_{WAKE} was set to 8.45kΩ to make sure a WAKE_OUT signal of 3.3V on the deserializer PCB. WAKE_OUT is then fed into a BJT circuit to drive a video receiver.

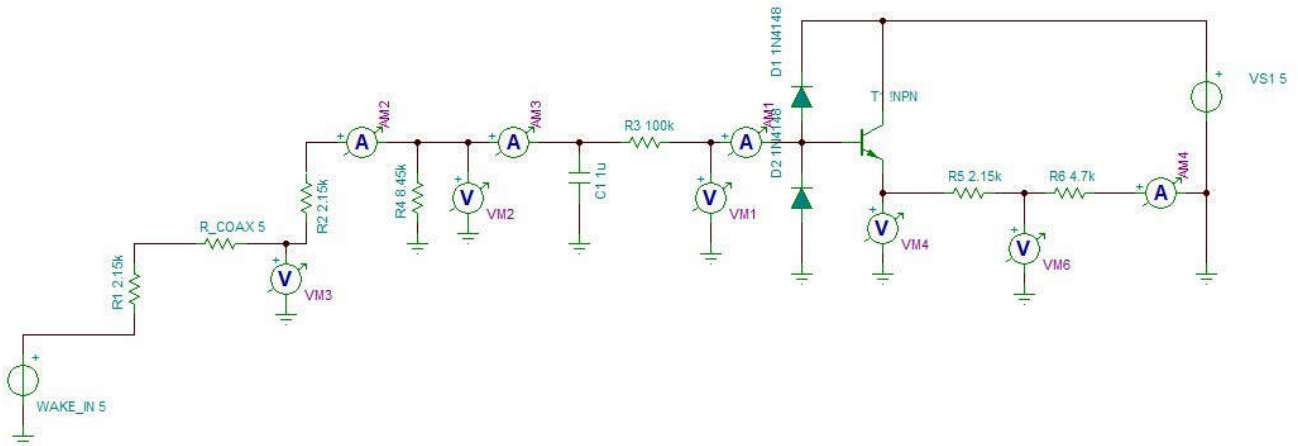

Figure 4-5. TINA-TI Wake-Up Circuit Simulation (WAKE_IN = 5V, WAKE_OUT = 3.3V)

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4.2 Wake-Up Circuit Measurements

The Wake-Up Circuit simulated in TINA-TI was tested using evaluation modules (EVMs) for the DS90Ux981-Q1, DS90Ux984-Q1, and TPS22810-Q1 devices. See Figure 4-6 for the measurements taken in the lab setup.

Figure 4-6. Wake-Up Circuit Lab Test Results

The yellow signal is the 5V rail that was input into the TPS22810-Q1 VIN pin. The blue signal is the 3.3V signal applied to the EN pin of the TPS22810-Q1 device. The purple signal is the 5V signal outputted by the VOUT pin of the TPS22810-Q1 load switch after the EN pin was pulled HIGH. VOUT was connected to the DOUT+ pin of the DS90Ux981-Q1EVM through a 2.15kΩ resistor. An 8.45kΩ resistor to ground was populated on the DS90Ux984-Q1EVM. The green signal is the 3.3V WAKE_OUT voltage measured on the DS90Ux984-Q1EVM that was used to drive a BJT circuit.

For individual customer systems, verify the intended Wake-Up Circuit implementation through simulations and tests on the physical system. Custom configurations can be used as long as the power specifications of the receiving device are met.

In addition, always verify that the Channel Specifications for the FPD-Link devices in the system are met (under worst-case temperature and current load operating conditions).

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5 Summary

Wake-Up Circuits are used in applications where a low power DC wake-up signal and the FPD-Link AC signal are transmitted over the same shared channel. In the context of FPD-Link, this Wake-Up Circuit is used to turn on a display that is currently in sleep mode before active transmission of video data. Careful selection of components in the Wake-Up Circuit can allow for the transmission of the desired DC wake-up signal with minimal interference on the high-speed signals on the channel.

6 References

- Texas Instruments, *TINA-TI*.
- Texas Instruments, *FPD-Link Learning Center*.
- Texas Instruments, *Basics of Load Switches*, application note.
- Texas Instruments, *DS90UB981-Q1 4K DSI to FPD-Link IV Bridge Serializer*, data sheet.
- Texas Instruments, *DS90UB984-Q1 4K FPD-Link IV to Embedded DisplayPort Bridge Deserializer*, data sheet.
- Texas Instruments, *TPS22810-Q1, 2.7-18-V, 79-mΩ On-Resistance Load Switch With Thermal Protection*, data sheet.

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