7.4 Device Functional Modes

7.4.1 Reset Implementation

When EN is deasserted (low), the SN65DSI83 device is in shutdown or reset state. In this state, CMOS inputs are ignored, the MIPI D-PHY inputs are disabled and outputs are high impedance. It is critical to transition the EN input from a low level to a high level after the V_{CC} supply has reached the minimum operating voltage, as shown in Figure 7-1. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

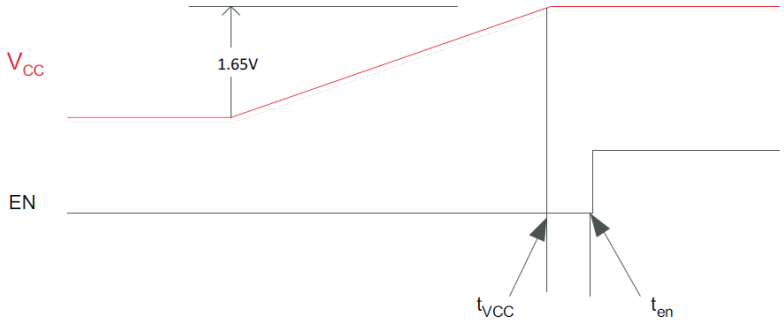

Figure 7-1. Cold Start V_{CC} Ramp up to EN

Fig 1 Start Vcc Ramp up to EN

EN, ULPS, RESET				
t_{en}	Enable time from EN or ULPS	$t_{c(o)}$ = 12.9 ns	1	ms
t_{dis}	Disable time to standby		0.1	
t_{reset}	Reset Time		10	ms

Fig 2 t_{en} spec

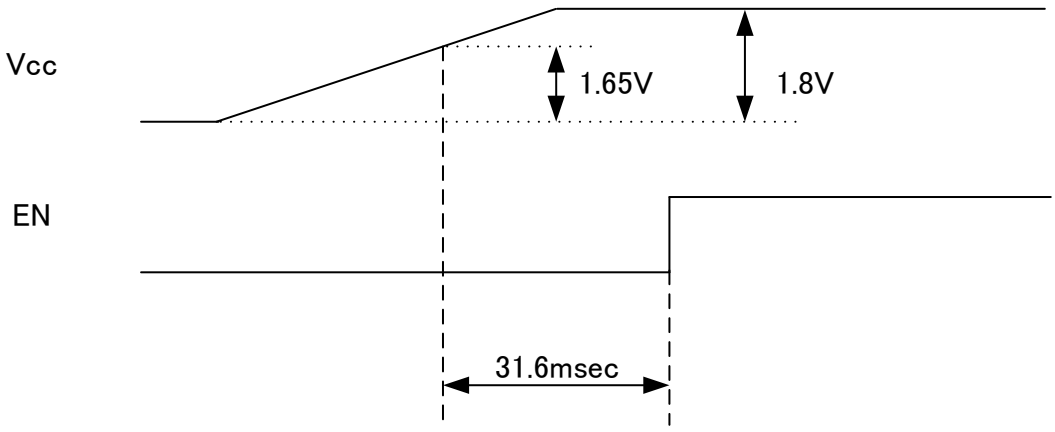

Fig 3 our system