TLK10034 Bring Up Procedures (Preliminary – subject to change)

ICP/CIF

ABSTRACT

This App Note includes several bring up procedures for the tlk10034 device. It covers device bring up in each of the 3 modes, 10G-KR, 1G-KX, and 10G with certain specific settings. The following list shows the specific bring up procedures.

- **KR with Auto Negotiation, Link Training, FEC, with 156.25 MHz / 312.5 MHz Refclk**
- **KR with Auto Negotiation, Link Training, HS Test Patterns, with 156.25 MHz / 312.5 MHz Refclk**
- **KR with Auto Negotiation, Link Training, LS Test Patterns with 156.25 MHz / 312.5 MHz Refclk**
- **KR using manual mode settings learned from Link Training, with 156.25 MHz / 312.5 MHz Refclk**
- **KR with Auto Negotiation negotiated to KX, with 156.25 MHz / 312.5 MHz Refclk**
- **KX with Auto Negotiation disabled, HS / LS Test Patterns, with 156.25 MHz / 312.5 MHz Refclk**
- **KX with Auto Negotiation disabled, HS / LS Test Patterns, with 156.25 MHz Refclk, Data Rate = 3.125Gbps**
- **10G in 4:1 or 2:1 mode, HS / LS Test Patterns, with 122.88 MHz Refclk , Data Rate = 9.8304Gbps**
- **10G in 1:1 mode, HS / LS Test Patterns, with 156.25 MHz Refclk, Data Rate = 3.125Gbps**
- **Appendix A. Initiating Next Page Exchange**
- **Appendix B. Link Partner Initiates Next Page Exchange**

KR with Auto Negotiation, Link Training, FEC, with 156.25 MHz / 312.5 MHz Refclk

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Reserved Register settings
  - Write 16'h0200 to 30.32800
  - Write 16'h006F to 30.32801
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- FEC enable / disable
  - If FEC enable, Write 1'b1 to 7.18.15 AN_FEC_REQUESTED
  - If FEC disable, Write 1'b0 to 7.18.15 AN_FEC_REQUESTED (default)

If next page exchange is needed, skip following step "Issue AN_RESTART", and refer to "Appendix A. Initiating Next Page Exchange" provisioning

- Issue AN_RESTART
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Wait for 1000ms

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Poll for Auto Negotiation Complete
  - Read 7.1.5 AN_COMPLETE to be 1'b1
  - Read 7.1.2 LINK_STATUS to be 1'b1 (TBD)
- Poll for Link Training Complete
  - Read 1.151.3 KR_TRAINING_FAIL to be 1'b0
  - Read 1.151.0 KR_RX_STATUS to be 1'b1
- Poll for 10GKR FEC mode
  - Read 7.48.4 AN_10G_KR_FEC to be 1'b1 (only valid if 7.18.15 was set)
  - Read 7.48.3 AN_10G_KR to be 1'b1

The following is the procedure to enable FEC

- Disable Sync Status Check
  - Write 1'b1 to 30.32801.4
- Override hardware generated core data path reset

    - Write 1'b1 to 30.33024.0 MC_SM_OVERRIDE[0]
- Override ENRX and RATE to HS Serdes
    - Write 1'b1 to both 30.32800.8 and 30.32800.12
- Set to Half Rate
    - Write 3'b101 to 30.3.2:0 HS_RATE_RX[2:0]
- Disable rxbclk by setting ENRX to 0
    - Write 1'b0 to 30.3.3 HS_ENRX
- Issue hardware generated core data path reset
    - Write 1'b1 to 30.33025.0 MC_SM_OVERRIDE_VAL[0]
    - Write 1'b0 to 30.33025.0 MC_SM_OVERRIDE_VAL[0]
- Enable rxbclk by setting ENRX to 1 (Rate is still half rate)
    - Write 1'b1 to 30.3.3 HS_ENRX
- Set to Full Rate (this step cannot be combined with the above step)
    - Write 3'b000 to 30.3.2:0 HS_RATE_RX[2:0]
- Remove the override of ENRX and RATE to HS Serdes
    - Write 1'b0 to both 30.32800.8 and 30.32800.12
- Enable Sync Status Check
    - Write 1'b0 to 30.32801.4

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Clear Latched Registers
    - Read 30.15 CHANNEL_STATUS_1 to clear
    - Read 30.16 HS_ERROR_COUNTER to clear
    - Read 30.17 LS_LN0_ERROR_COUNTER to clear
    - Read 30.18 LS_LN1_ERROR_COUNTER to clear
    - Read 30.19 LS_LN2_ERROR_COUNTER to clear
    - Read 30.20 LS_LN3_ERROR_COUNTER to clear
    - Read LS status registers for each lane to clear
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read 30.21 LS_STATUS_1 to clear
    - Read 1.1 PMA_STATUS_1 to clear
    - Read 1.8 PMA_STATUS_2 to clear
    - Read 3.1 PCS_STATUS_1 to clear
    - Read 3.8 PCS_STATUS_2 to clear
- Operational Mode Status
    - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C03)
    - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000)
    - Read Verify LS status register for each lane
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read Verify 30.21.10 LS_LOS (1'b0)
        - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
        - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
    - Read Verify 1.1.7 FAULT (1'b0)
    - Read Verify 1.1.2 RX_LINK (1'b1)
    - Read Verify 3.1.7 PCS_FAULT (1'b0)
    - Read Verify 3.1.2 PCS_RX_LINK (1'b1)

KR with Auto Negotiation, Link Training, HS Test Patterns, with 156.25 MHz / 312.5 MHz Refclk

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Reserved Register settings
  - Write 16'h0200 to 30.32800
  - Write 16'h006F to 30.32801
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue AN_RESTART
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Poll for Auto Negotiation Complete
  - Read 7.1.5 AN_COMPLETE to be 1'b1
  - Read 7.1.2 LINK_STATUS to be 1'b1
- Poll for Link Training Complete
  - Read 1.151.3 KR_TRAINING_FAIL to be 1'b0
  - Read 1.151.0 KR_RX_STATUS to be 1'b1
- Poll for 10GKR mode
  - Read 7.48.3 AN_10G_KR to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.18 LS_LN1_ERROR_COUNTER to clear
  - Read 30.19 LS_LN2_ERROR_COUNTER to clear
  - Read 30.20 LS_LN3_ERROR_COUNTER to clear
  - Read LS status registers for each lane to clear
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3

        - Read 30.21 LS_STATUS_1 to clear
    - Read 1.1 PMA_STATUS_1 to clear
    - Read 1.8 PMA_STATUS_2 to clear
    - Read 3.1 PCS_STATUS_1 to clear
    - Read 3.8 PCS_STATUS_2 to clear
- Operational Mode Status
    - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C03)
    - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000)
    - Read Verify LS status register for each lane
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read Verify 30.21.10 LS_LOS (1'b0)
        - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
        - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
    - Read Verify 1.1.7 FAULT (1'b0)
    - Read Verify 1.1.2 RX_LINK (1'b1)
    - Read Verify 3.1.7 PCS_FAULT (1'b0)
    - Read Verify 3.1.2 PCS_RX_LINK (1'b1)

The following instructions are for enabling HS test pattern generation / verification.

- Reserved Register settings
    - Write 16'h007F to 30.32801
- Select test pattern
    - Vendor Specific Test Patterns
        - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.10:8
        - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.10:8
        - 2^{7} – 1 PRBS pattern – Write 3'b101 to 30.11.10:8
    - KR Standard Test Patterns
        - 2^{31} – 1 PRBS pattern – Write 1'b1 to 3.42.4
        - Pseudo Random test pattern – Write 1'b0 to 3.42.1
        - Square Wave test pattern – Write 1'b1 to 3.42.1
- Enable KR HS test pattern generation
    - Vendor Specific Test Patterns
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Write 1'b1 to 30.11.13
    - KR Standard Test Patterns
        - 2^{31} – 1 PRBS pattern – enabled during test pattern select
        - Pseudo Random – Write 1'b1 to 3.42.3
        - Square Wave – Write 1'b1 to 3.42.3
- Enable KR HS test pattern verification
    - Vendor Specific Test Patterns
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Write 1'b1 to 30.11.12
    - KR Standard Test Patterns
        - 2^{31} – 1 PRBS – Write 1'b1 to 3.42.5 or Write 1'b1 to 30.11.12
        - Pseudo Random – Write 1'b1 to 3.42.2
        - Square Wave – Verification not supported
- Clear Error Counters
    - Vendor Specific Test Patterns
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Read 30.16 HS_ERROR_COUNTER to clear
    - KR Standard Test Patterns
        - 2^{31} – 1 PRBS / Pseudo Random – Read 3.43 PCS_TP_ERR_COUNT to clear
        - Square Wave – Verification not supported

- Check Error Counters
  - Vendor Specific Test Patterns
    - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - KR Standard Test Patterns
    - 2^{31} – 1 PRBS / Pseudo Random – Read Verify 3.43 PCS_TP_ERR_COUNT – (16'h0000)
    - Square Wave – Verification not supported

KR with Auto Negotiation, Link Training, LS Test Patterns with 156.25 MHz / 312.5 MHz Refclk

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Reserved Register settings
  - Write 16'h0200 to 30.32800
  - Write 16'h006F to 30.32801
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue AN_RESTART
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Poll for Auto Negotiation Complete
  - Read 7.1.5 AN_COMPLETE to be 1'b1
  - Read 7.1.2 LINK_STATUS to be 1'b1
- Poll for Link Training Complete
  - Read 1.151.3 KR_TRAINING_FAIL to be 1'b0
  - Read 1.151.0 KR_RX_STATUS to be 1'b1
- Poll for 10GKR mode
  - Read 7.48.3 AN_10G_KR to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.18 LS_LN1_ERROR_COUNTER to clear
  - Read 30.19 LS_LN2_ERROR_COUNTER to clear
  - Read 30.20 LS_LN3_ERROR_COUNTER to clear
  - Read LS status registers for each lane to clear
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
    - Read 30.21 LS_STATUS_1 to clear

    - Read 1.1 PMA_STATUS_1 to clear
    - Read 1.8 PMA_STATUS_2 to clear
    - Read 3.1 PCS_STATUS_1 to clear
    - Read 3.8 PCS_STATUS_2 to clear
- Operational Mode Status
    - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C03)
    - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000)
    - Read Verify LS status register for each lane
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read Verify 30.21.10 LS_LOS (1'b0)
        - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
        - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
    - Read Verify 1.1.7 FAULT (1'b0)
    - Read Verify 1.1.2 RX_LINK (1'b1)
    - Read Verify 3.1.7 PCS_FAULT (1'b0)
    - Read Verify 3.1.2 PCS_RX_LINK (1'b1)

The following instructions are for enabling LS test pattern generation / verification.
(Switching between CRPAT and CJPAT pattern verification requires a datapath reset)

- Enable KR LS test pattern generation / verification
    - Select test pattern
        - 2^{31} – 1 PRBS pattern – Write 3'b111 to {30.11.11, 30.11.5:4}
        - 2^{23} – 1 PRBS pattern – Write 3'b110 to {30.11.11, 30.11.5:4}
        - 2^{7} – 1 PRBS pattern – Write 3'b101 to {30.11.11, 30.11.5:4}
        - High Frequency – Write 2'b00 to 1.32770.5:4, Write 2'b00 to 1.32771.13:12
        - Mixed Frequency – Write 2'b10 to 1.32770.5:4, Write 2'b10 to 1..32771.13:12
        - Low Frequency – Write 2'b01 to 1.32770.5:4, Write 2'b01 to 1..32771.13:12
        - CRPAT / CJPAT – No need for selection
    - Enable KR LS test pattern generation
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Write 1'b1 to 30.11.7
        - High / Mixed / Low Frequency – Write 1'b1 to 1.32770.0
        - CRPAT – Write 1'b1 to 1.32770.3
        - CJPAT – Write 1'b1 to 1.32770.2
    - Enable KR LS test pattern verification
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Write 1'b1 to 30.11.6
        - High / Mixed / Low Frequency – Write 1'b1 to 1.32771.8
        - CRPAT – Write 1'b1 to 1.32771.11
        - CJPAT – Write 1'b1 to 1.32771.10
    - Clear Status and Error Counters
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Read 30.17, 18, 19, 20 LS_LN0/1/2/3_ERROR_COUNTER to clear
        - High / Mixed / Low Frequency – Read 1.32795 ,32796, 32797, 32798 KR_VS_TX_LN0/1/2/3_HLM_ERR_COUNT to clear
        - CRPAT / CJPAT –
            - Read 1.32792.15 TX_TPV_TP_SYNC to clear
            - Read 1.32793 KR_VS_TX_CRCJ_ERR_COUNT_1 to clear
            - Read 1.32794 KR_VS_TX_CRCJ_ERR_COUNT_2 to clear
    - Check Status and Error Counters
        - 2^{31} – 1 PRBS / 2^{23} – 1 PRBS / 2^{7} – 1 PRBS – Read Verify 30.17, 18, 19, 20 LS_LN0/1/2/3_ERROR_COUNTER – (16'h0000)

- High / Mixed / Low Frequency – Read Verify 1.32795 ,32796, 32797, 32798 KR_VS_TX_LN0/1/2/3_HLM_ERR_COUNT – (16'h0000)
- CRPAT / CJPAT –
  - Read Verify 1.32792.15 TX_TPV_TP_SYNC (1'b1)
  - Read Verify 1.32793 KR_VS_TX_CRCJ_ERR_COUNT_1 (16'h0000)
  - Read Verify 1.32794 KR_VS_TX_CRCJ_ERR_COUNT_2 (16'h0000)

**Note: Must always read KR_VS_TX_CRCJ_ERR_COUNT_1 before reading KR_VS_TX_CRCJ_ERR_COUNT_2.

KR using manual mode settings learned from Link Training, with 156.25 MHz / 312.5 MHz Refclk

1. **Start up in KR with Auto Negotiation and Link Training**
2. **Read Link Training Settings and store register values**
3. **Set in KR manual mode with Auto Negotiation and Link Training off**
4. **Write Link Training stored settings (step #2) into registers**
5. **Enable FEC**

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

Start up in KR with Auto Negotiation and Link Training

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Reserved Register settings
  - Write 16'h0200 to 30.32800
  - Write 16'h006F to 30.32801
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue AN_RESTART
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Wait for 1000ms
- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Poll for Auto Negotiation Complete
  - Read 7.1.5 AN_COMPLETE to be 1'b1
  - Read 7.1.2 LINK_STATUS to be 1'b1
- Poll for Link Training Complete
  - Read 1.151.3 KR_TRAINING_FAIL to be 1'b0
  - Read 1.151.0 KR_RX_STATUS to be 1'b1
- Poll for 10GKR mode
  - Read 7.48.3 AN_10G_KR to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.18 LS_LN1_ERROR_COUNTER to clear
  - Read 30.19 LS_LN2_ERROR_COUNTER to clear
  - Read 30.20 LS_LN3_ERROR_COUNTER to clear

    - Read LS status registers for each lane to clear
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read 30.21 LS_STATUS_1 to clear
    - Read 1.1 PMA_STATUS_1 to clear
    - Read 1.8 PMA_STATUS_2 to clear
    - Read 3.1 PCS_STATUS_1 to clear
    - Read 3.8 PCS_STATUS_2 to clear
- Operational Mode Status
    - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C03)
    - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000)
    - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000)
    - Read Verify LS status register for each lane
        - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
        - Read Verify 30.21.10 LS_LOS (1'b0)
        - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
        - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
    - Read Verify 1.1.7 FAULT (1'b0)
    - Read Verify 1.1.2 RX_LINK (1'b1)
    - Read Verify 3.1.7 PCS_FAULT (1'b0)
    - Read Verify 3.1.2 PCS_RX_LINK (1'b1)

Read Link Training Settings and store register values

- Read 30.32818.3:0 HS_FINAL_SWING [3:0]
- Read 30.32818.9 HS_FINAL_EQHLD
- Read 30.32817.15:14 HS_FINAL_AZCAL [1:0]
- Read 30.32818.11 HS_FINAL_ENRX
- Read 30.32818.10 HS_FINAL_ENTRACK
- Read 30.32818.8:4 HS_FINAL_TWCRF [4:0]
- Read 30.32817.13 HS_FINAL_FIRUPT
- Read 30.32817.12:8 HS_FINAL_TWPOST1 [4:0]
- Read 30.32817.7:4 HS_FINAL_TWPRE [3:0]
- Read 30.32817.3:0 HS_FINAL_TWPOST2 [3:0]

Set in KR manual mode with Auto Negotiation and Link Training off

- Device Pin Settings
    - Ensure ST input pin is Low
    - Ensure MODE_SEL input pin is Low
    - Ensure PRBSEN input pin is Low
    - Ensure REFCLK_SEL input pin is Low
- Reset Device
    - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
    - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
    - If using 312.5 MHz – Write 1'b1 to 30.29.12
    - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
    - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Disable Auto Negotiation and Link Training
    - Write 1'b0 to 7.0.12 to disable Auto negotiation
    - Write 16'h0000 to 1.150 KR_TRAIN_CONTROL to disable Link Training
- Reserved Register settings

- Write 16'h03FF to 30.32800
- Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)

Write Link Training stored settings (step #2) into registers

- Write 30.3.15:12 HS_SWING [3:0]
- Write 30.3.10 HS_EQHLD
- Write 30.3.5:4 HS_AZCAL [1:0]
- Write 30.3.3 HS_ENRX
- Write 30.3.2:0 HS_RATE_TX [2:0]
- Write 30.4.15 HS_ENTRACK
- Write 30.4.4:0 HS_TWCRF [4:0]
- Write 30.5.13 HS_FIRUPT
- Write 30.5.12:8 HS_TWPOST1 [4:0]
- Write 30.5.7:4 HS_TWPRE [3:0]
- Write 30.5.3:0 HS_TWPOST2 [3:0]

- Issue Data path Reset
  - Write 1'b1 to 30.14.3
- Wait for 1000ms

Device provisioning is complete at this point.

If FEC functionality is desired, follow these steps:

- Disable Sync Status Check
  - Write 1'b1 to 30.32801.4
- FEC enable
  - Write 1'b1 to 1.171.0 KR_FEC_EN
- Override hardware generated core data path reset
  - Write 1'b1 to 30.33024.0 MC_SM_OVERRIDE[0]
- Override ENRX and RATE to HS Serdes
  - Write 1'b1 to both 30.32800.8 and 30.32800.12
- Set to Half Rate
  - Write 3'b101 to 30.3.2:0 HS_RATE_RX[2:0]
- Disable rxbclk by setting ENRX to 0
  - Write 1'b0 to 30.3.3 HS_ENRX
- Issue hardware generated core data path reset
  - Write 1'b1 to 30.33025.0 MC_SM_OVERRIDE_VAL[0]
  - Write 1'b0 to 30.33025.0 MC_SM_OVERRIDE_VAL[0]
- Enable rxbclk by setting ENRX to 1 (Rate is still half rate)
  - Write 1'b1 to 30.3.3 HS_ENRX
- Set to Full Rate (this step cannot be combined with the above step)
  - Write 3'b000 to 30.3.2:0 HS_RATE_RX[2:0]
- Remove the override of ENRX and RATE to HS Serdes
  - Write 1'b0 to both 30.32800.8 and 30.32800.12
- Enable Sync Status Check
  - Write 1'b0 to 30.32801.4
- FEC provisioning is done at this time.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1

- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.18 LS_LN1_ERROR_COUNTER to clear
  - Read 30.19 LS_LN2_ERROR_COUNTER to clear
  - Read 30.20 LS_LN3_ERROR_COUNTER to clear
  - Read LS status registers for each lane to clear
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
    - Read 30.21 LS_STATUS_1 to clear
  - Read 1.1 PMA_STATUS_1 to clear
  - Read 1.8 PMA_STATUS_2 to clear
  - Read 3.1 PCS_STATUS_1 to clear
  - Read 3.8 PCS_STATUS_2 to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C03)
  - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000)
  - Read Verify LS status register for each lane
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
    - Read Verify 30.21.10 LS_LOS (1'b0)
    - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
    - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
  - Read Verify 1.1.7 FAULT (1'b0)
  - Read Verify 1.1.2 RX_LINK (1'b1)
  - Read Verify 3.1.7 PCS_FAULT (1'b0)
  - Read Verify 3.1.2 PCS_RX_LINK (1'b1)

KR with Auto Negotiation negotiated to KX, with 156.25 MHz / 312.5 MHz Refclk

Communicating system must be in 1GKX mode.

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Reserved Register settings
  - Write 16'h006F to 30.32801
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue AN_RESTART
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Poll for Auto Negotiation Complete
  - Read 7.1.5 AN_COMPLETE to be 1'b1
  - Read 7.1.2 LINK_STATUS to be 1'b1
- Poll for 1GKX mode
  - Read 7.48.1 AN_1G_KX to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.21 LS_STATUS_1 to clear
  - Read 1.161 KX_STATUS to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h1C03)
  - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.21.10 LS_LOS (1'b0)
  - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
  - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)

- Read Verify 1.161.11 – KX_TX_FAULT (1'b0)
- Read Verify 1.161.10 – KX_RX_FAULT (1'b0)

KX with Auto Negotiation disabled, HS / LS Test Patterns, with 156.25 MHz / 312.5 MHz Refclk

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- REFCLK input frequency and selection
  - If using 156.25 MHz – Write 1'b0 to 30.29.12 (default)
  - If using 312.5 MHz – Write 1'b1 to 30.29.12
  - If REFCLK_0_P/N used – Write 1'b0 to 30.1.1 (default)
  - If REFCLK_1_P/N used – Write 1'b1 to 30.1.1
- Mode selection
  - Write 1'b0 to 7.0.12 to disable Auto negotiation
  - Write 1'b0 to 30.1.11 to set device to 1G-KX manual mode
- Reserved Register settings
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue Data path Reset
  - Write 1'b1 to 30.14.3
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.21 LS_STATUS_1 to clear
  - Read 1.161 KX_STATUS to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h1C03)
  - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.21.10 LS_LOS (1'b0)
  - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
  - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
  - Read Verify 1.161.11 – KX_TX_FAULT (1'b0)
  - Read Verify 1.161.10 – KX_RX_FAULT (1'b0)

The following instructions are for enabling HS / LS test pattern generation / verification.

- Enable KX HS/LS test pattern generation / verification

- Select HS test pattern
  - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.10:8
  - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.10:8
  - 2^{7} – 1 PRBS pattern – Write 3'b101 to 30.11.10:8
  - High Frequency – Write 3'b000 to 30.11.10:8
  - Low Frequency – Write 3'b001 to 30.11.10:8
  - Mixed Frequency – Write 3'b010 to 30.11.10:8
  - CRPAT Long – Write 3'b011 to 30.11.10:8
  - CRPAT Short – Write 3'b100 to 30.11.10:8
- Enable KX HS test pattern generation
  - All Patterns – Write 1'b1 to 30.11.13
- Enable KX HS test pattern verification
  - Note: HLM Frequency verification not supported
  - All Other Patterns – Write 1'b1 to 30.11.12
- Check TP Sync Status
  - CRPAT – Read Verify 30.15.15 – HS_TP_STATUS (1'b1)
  - All Other Patterns – No need to check this bit
- Clear Error Counter
  - CRPAT Long/Short – Write 1'b1 to 30.11.6 and Write 3'b011 to {30.11, 30.11.5:4}
  - All Patterns – Read 30.16 HS_ERROR_COUNTER to clear
- Check Error Counter
  - All Patterns – Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
- Select LS test pattern
  - 2^{31} – 1 PRBS pattern – Write 3'b111 to {30.11.11, 30.11.5:4}
  - 2^{23} – 1 PRBS pattern – Write 3'b110 to {30.11.11, 30.11.5:4}
  - 2^{7} – 1 PRBS pattern – Write 3'b101 to {30.11.11, 30.11.5:4}
  - High Frequency – Write 3'b000 to {30.11.11, 30.11.5:4}
  - Low Frequency – Write 3'b001 to {30.11.11, 30.11.5:4}
  - Mixed Frequency – Write 3'b010 to {30.11.11, 30.11.5:4}
  - CRPAT Long – Write 3'b011 to {30.11.11, 30.11.5:4}
  - CRPAT Short – Write 3'b100 to {30.11.11, 30.11.5:4}
- Enable KX LS test pattern generation
  - All Patterns – Write 1'b1 to 30.11.7
- Enable KX LS test pattern verification
  - Note: HLM Frequency verification not supported
  - All Other Patterns – Write 1'b1 to 30.11.6
- Check TP Sync Status
  - CRPAT – Read Verify 30.15.14 – LS_TP_STATUS (1'b1)
  - All Other Patterns – No need to check this bit
- Clear Error Counter
  - All Patterns – Read 30.17 LS_LN0_ERROR_COUNTER to clear
- Check Error Counter
  - All Patterns – Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)

KX with Auto Negotiation disabled, HS / LS Test Patterns, with 156.25 MHz Refclk, Data Rate = 3.125Gbps

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is Low
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- Mode selection
  - Write 1'b1 to 30.29.13 to enable 1GKX manual setting
  - Write 1'b0 to 7.0.12 to disable Auto negotiation
  - Write 1'b0 to 30.1.11 to set device to 1G-KX mode
  - Write 4'b0111 to 30.2.3:0 to set HS PLL multiplier to 10x
- Reserved Register settings
  - Write to 30.3, 30.4 (Refer to "tlk10034 Link Training Optimization Guide" for recommended values)
- Issue Data path Reset
  - Write 1'b1 to 30.14.3
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.21 LS_STATUS_1 to clear
  - Read 1.161 KX_STATUS to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h1C03)
  - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.21.10 LS_LOS (1'b0)
  - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)
  - Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)
  - Read Verify 1.161.11 – KX_TX_FAULT (1'b0)
  - Read Verify 1.161.10 – KX_RX_FAULT (1'b0)

The following instructions are for enabling HS / LS test pattern generation / verification.

- Enable KX HS/LS test pattern generation / verification
  - Select HS test pattern
    - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.10:8
    - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.10:8

- 2^7 – 1 PRBS pattern – Write 3'b101 to 30.11.10:8
- High Frequency – Write 3'b000 to 30.11.10:8
- Low Frequency – Write 3'b001 to 30.11.10:8
- Mixed Frequency – Write 3'b010 to 30.11.10:8
- CRPAT Long – Write 3'b011 to 30.11.10:8
- CRPAT Short – Write 3'b100 to 30.11.10:8

- Enable KX HS test pattern generation
  - All Patterns – Write 1'b1 to 30.11.13
- Enable KX HS test pattern verification
  - Note: HLM Frequency verification not supported
  - All Other Patterns – Write 1'b1 to 30.11.12
- Check TP Sync Status
  - CRPAT – Read Verify 30.15.15 – HS_TP_STATUS (1'b1)
  - All Other Patterns – No need to check this bit
- Clear Error Counter
  - CRPAT Long/Short – Write 1'b1 to 30.11.6 and Write 3'b011 to {30.11, 30.11.5:4}
  - All Patterns – Read 30.16 HS_ERROR_COUNTER to clear
- Check Error Counter
  - All Patterns – Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
- Select LS test pattern
  - 2^{31} – 1 PRBS pattern – Write 3'b111 to {30.11.11, 30.11.5:4}
  - 2^{23} – 1 PRBS pattern – Write 3'b110 to {30.11.11, 30.11.5:4}
  - 2^7 – 1 PRBS pattern – Write 3'b101 to {30.11.11, 30.11.5:4}
  - High Frequency – Write 3'b000 to {30.11.11, 30.11.5:4}
  - Low Frequency – Write 3'b001 to {30.11.11, 30.11.5:4}
  - Mixed Frequency – Write 3'b010 to {30.11.11, 30.11.5:4}
  - CRPAT Long – Write 3'b011 to {30.11.11, 30.11.5:4}
  - CRPAT Short – Write 3'b100 to {30.11.11, 30.11.5:4}
- Enable KX LS test pattern generation
  - All Patterns – Write 1'b1 to 30.11.7
- Enable KX LS test pattern verification
  - Note: HLM Frequency verification not supported
  - All Other Patterns – Write 1'b1 to 30.11.6
- Check TP Sync Status
  - CRPAT – Read Verify 30.15.14 – LS_TP_STATUS (1'b1)
  - All Other Patterns – No need to check this bit
- Clear Error Counter
  - All Patterns – Read 30.17 LS_LN0_ERROR_COUNTER to clear
- Check Error Counter
  - All Patterns – Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)

10G in 4:1 or 2:1 mode, HS / LS Test Patterns, with 122.88 MHz Refclk , Data Rate = 9.8304Gbps

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low
  - Ensure MODE_SEL input pin is High
  - Ensure PRBSEN input pin is Low
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- Mode selection
  - 2:1 mode
    - Write 2'b00 to 30.1.9:8 to set 2:1 mode
    - Write 4'b1001 to 30.6.3:0 to set LS MPY to 20x
  - 4:1 mode
    - Write 2'b11 to 30.1.9:8 to set 4:1 mode (default)
- Issue Data path Reset
  - Write 1'b1 to 30.14.3
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.18 LS_LN1_ERROR_COUNTER to clear
  - Read 30.19 LS_LN2_ERROR_COUNTER to clear
  - Read 30.20 LS_LN3_ERROR_COUNTER to clear
  - Read LS status registers for each lane to clear
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
    - Read 30.21 LS_STATUS_1 to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h5C0F)
  - Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.18 LS_LN1_ERROR_COUNTER – (16'h0000)
  - Read Verify 30.19 LS_LN2_ERROR_COUNTER – (16'h0000) (if applicable)
  - Read Verify 30.20 LS_LN3_ERROR_COUNTER – (16'h0000) (if applicable)
  - Read Verify LS status register for each lane (if applicable)
    - Write 2'b00 / 2'b01 / 2'b10 / 2'b11 to 30.12.13:12 to access LS lane 0 / 1 / 2 / 3
    - Read Verify 30.21.10 LS_LOS (1'b0)
    - Read Verify 30.21.8 LS_CH_SYNC_STATUS (1'b1)

- Read Verify 30.21.3 LS_INVALID_DECODE (1'b0)

The following instructions are for enabling HS / LS test pattern generation / verification.

- Enable HS/LS test pattern generation
  - Select HS test pattern
    - 2^7 – 1 PRBS pattern – Write 3'b101 to 30.11.10:8
    - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.10:8
    - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.10:8
    - High Frequency – Write 3'b000 to 30.11.10:8
    - Low Frequency – Write 3'b001 to 30.11.10:8
    - Mixed Frequency – Write 3'b010 to 30.11.10:8
    - CRPAT Long – Write 3'b011 to 30.11.10:8
    - CRPAT Short – Write 3'b100 to 30.11.10:8
  - Enable HS test pattern generation
    - All Patterns – Write 1'b1 to 30.11.13
  - Enable HS test pattern verification
    - All Patterns – Write 1'b1 to 30.11.12
  - Check TP Status
    - PRBS – No need to check this bit
    - H/M/L and CRPAT – Read Verify 30.15.15 – HS_TP_STATUS (1'b1)
  - Clear Error Counter
    - All Patterns – Read 30.16 HS_ERROR_COUNTER to clear
  - Check Error Counter
    - All Patterns – Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
  - Select LS test pattern
    - 2^7 – 1 PRBS pattern – Write 3'b101 to 30.11.11,5:4
    - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.11,5:4
    - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.11,5:4
  - Enable LS test pattern generation
    - All Patterns – Write 1'b1 to 30.11.7
  - Enable LS test pattern verification
    - All Patterns – Write 1'b1 to 30.11.6
  - Clear Error Counters
    - All Patterns – Read 30.17/18/19/20 LS_LN0/1/2/3_ERROR_COUNTER to clear
  - Check Error Counters
    - All Patterns – Read Verify 30.17/18/19/20 LS_LN0/1/2/3_ERROR_COUNTER – (16'h0000) (if applicable)

10G in 1:1 mode, HS / LS Test Patterns, with 156.25 MHz Refclk, Data Rate = 3.125Gbps

***Note: Script only provisions 1 channel based on PHY address setting. To provision all channels at the same time, write 1'b1 to 30.0.11 GLOBAL_WRITE after device reset.**

- Device Pin Settings
  - Ensure ST input pin is Low.
  - Ensure MODE_SEL input pin is High.
  - Ensure PRBSEN input pin is Low.
  - Ensure REFCLK_SEL input pin is Low
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 30.0.15)
- Mode selection
  - Write 4'b0111 to 30.2.3:0 to set HS PLL multiplier to 10x
  - Write 2'b01 to 30.3.9:8 to set HS_RATE_TX to Half Rate
  - Write 3'b101 to 30.3.2:0 to set HS_RATE_RX to Half Rate
  - For 1:1 mode
    - Write 2'b11 to 30.1.13:12 to set mode
    - Write 2'b00 to 30.7.9:8 to set LS TX Serdes lane rate to Full rate
    - Write 2'b00 to 30.7.1:0 to set LS RX Serdes lane rate to Full rate
    - Write 2'b11 to 30.29.3:2 to bypass encoder / decoder on RX path
- Issue Data path Reset
  - Write 1'b1 to 30.14.3
- Wait for 1000ms

Device provisioning is complete at this point.

The following instructions are for latch clearing and polling status registers.

- Poll Serdes HS_AZ_DONE complete, HS_AGC_LOCKED locked, PLL Status locked
  - Read 30.15.12 HS_AZ_DONE to be 1'b1
  - Read 30.15.11 HS_AGC_LOCKED to be 1'b1
  - Read 30.15.1,0 LS_PLL_LOCK / HS_PLL_LOCK both to be 1'b1
- Clear Latched Registers
  - Read 30.15 CHANNEL_STATUS_1 to clear
  - Read 30.16 HS_ERROR_COUNTER to clear
  - Read 30.17 LS_LN0_ERROR_COUNTER to clear
  - Read 30.21 LS_STATUS_1 to clear
- Operational Mode Status
  - Read Verify 30.15 CHANNEL_STATUS_1 – (16'h1803)
  - Read Verify 30.21.10 LS_LOS (1'b0)

The following instructions are for enabling HS / LS test pattern generation / verification.

- Enable HS/LS test pattern generation
  - Select HS test pattern
    - 2^{31} – 1 PRBS pattern – Write 3'b111 to 30.11.10:8
    - 2^{23} – 1 PRBS pattern – Write 3'b110 to 30.11.10:8
    - 2^{7} – 1 PRBS pattern – Write 3'b101 to 30.11.10:8
  - Enable HS test pattern generation
    - All Patterns – Write 1'b1 to 30.11.13
  - Enable HS test pattern verification
    - All Patterns – Write 1'b1 to 30.11.12

- Clear Error Counter
  - All Patterns – Read 30.16 HS_ERROR_COUNTER to clear
- Clear Error Counter
  - All Patterns – Read Verify 30.16 HS_ERROR_COUNTER – (16'h0000)
- Select LS test pattern
  - 2^{31} – 1 PRBS pattern – Write 3'b111 to {30.11.11, 30.11.5:4}
  - 2^{23} – 1 PRBS pattern – Write 3'b110 to {30.11.11, 30.11.5:4}
  - 2^{7} – 1 PRBS pattern – Write 3'b101 to {30.11.11, 30.11.5:4}
- Enable LS test pattern generation
  - All Patterns – Write 1'b1 to 30.11.7
- Enable LS test pattern verification
  - All Patterns – Write 1'b1 to 30.11.6
- Clear Error Counter
  - All Patterns – Read 30.17 LS_LN0_ERROR_COUNTER to clear
- Check Error Counter
  - All Patterns – Read Verify 30.17 LS_LN0_ERROR_COUNTER – (16'h0000)

Appendix A. Initiating Next Page Exchange

***Note: Can be executed during initial bring up or after provisioning is complete.**

- Provision Base Page
  - Write 1'b1 to 7.16.15 AN_NEXT_PAGE
  - Provision the rest of the Base Page, 7.16, 7.17 and 7.18
- Clear Page Received status
  - Read 7.1.6 AN_PAGE_RCVD
- Issue Auto-Negotiation Restart
  - Write 1'b1 to 7.0.9 AN_RESTART
  - Read 7.0 AN_CONTROL
- Poll for Base Page Received
  - Read 7.1.6 AN_PAGE_RCVD until value is 1'b1
- Read the Link Partner Base Page
  - Read 7.19 AN_LP_ADVERTISEMENT_1
  - Read 7.20 AN_LP_ADVERTISEMENT_2
  - Read 7.21 AN_LP_ADVERTISEMENT_3
- Write the Next Page to send to the Link Partner
  - Write to 7.24 with the desired value. Not needed for Null Message Code.
  - Write to 7.23 with the desired value. Not needed for Null Message Code.
  - If this is the last Next Page, clear the Next Page bits in Base Page and Next Page, and clear the Reserved Register.
    - Write 1'b0 to 7.16.15 AN_NEXT_PAGE
    - Write 1'b0 to 7.22.15 AN_XNP_NEXT_PAGE
    - If this page is not valid and the Link Partner is still sending valid Next Pages, write Null Message Code, 11'b000_0000_0001 to 7.22.10:0 AN_CODE_FIELD
  - If there is another Next Page,
    - Write 1'b1 to 7.22.15. Update all other bits in 7.22 in the same write transaction. Note that writing to 7.22 can only be done one time and it is the final write to transmit Next Page.
- Poll for Next Page Received
  - Read 7.1.6 AN_PAGE_RCVD until value is 1'b1
  - If not found in expected time frame TBD, issue AN_RESTART and start back at beginning of order.
- Read the Link Partner Next Page
  - Read 7.25 AN_LP_XNP_ABILITY_1
  - Read 7.26 AN_LP_XNP_ABILITY_2
  - Read 7.27 AN_LP_XNP_ABILITY_3
- Continue sending Next Pages until there are no more Next Pages to send. If the Link Partner has another Next Page to send when the local devices has no more Next Pages to send, then continue to exchange Next Pages by writing Null Message Code into register 7.22.
- When both local and partner channel have no more Next Pages to send (7.22.15 = 1'b0 and 7.25.15 = 1'b0), confirm that the device is configured for 10GKR or 1GKX according to the Operational Mode Status procedure found in the appropriate Bring Up procedure.

Appendix B. Link Partner Initiates Next Page Exchange

***Note: If Link is lost and Auto-Negotiation is enabled, check if the Link Partner has initiated Next Page exchange.**

- Poll for Base Page Received
  - Read 7.1.6 AN_PAGE_RCVD until value is 1'b1
- Read the Link Partner Base Page
  - Read 7.19 AN_LP_ADVERTISEMENT_1
    - If bit 15 is 1'b1, Next Page exchange has been requested.
  - Read 7.20 AN_LP_ADVERTISEMENT_2
  - Read 7.21 AN_LP_ADVERTISEMENT_3
- Write the Next Page to send to the Link Partner. Since the Link Partner initiated the Next Page exchange, this value is typically Null Message Code. If a value other than Null Message Code needs to be sent, the Next Page bit should be set to 1'1 in 7.22.15.
  - Write to 7.24 with the desired value. Not needed for Null Message Code.
  - Write to 7.23 with the desired value. Not needed for Null Message Code.
  - If this is the last Next Page, or there are no Next Pages to be sent, clear the Next Page bit in Next Page.
    - Write 1'b0 to 7.22.15. Write 11'b000_0000_0001 to 7.22.10:0 AN_CODE_FIELD for Null Message Code. Only one write transaction is given to this register.
  - If there is another Next Page,
    - Write 1'b1 to 7.22.15. Update all other bits in 7.22 in the same write transaction.
- Poll for Next Page Received
  - Read 7.1.6 AN_PAGE_RCVD until value is 1'b1
  - If not found in expected time frame TBD, issue AN_RESTART and start back at beginning of order.
- Read the Link Partner Next Page
  - Read 7.25 AN_LP_XNP_ABILITY_1
  - Read 7.26 AN_LP_XNP_ABILITY_2
  - Read 7.27 AN_LP_XNP_ABILITY_3
- Continue sending Next Pages until there are no more Next Pages to send. If the Link Partner has another Next Page to send when the local devices has no more Next Pages to send, then continue to exchange Next Pages by writing Null Message Code into register 7.22.
- When both local and partner channel have no more Next Pages to send (7.22.15 = 1'b0 and 7.25.15 = 1'b0), confirm that the device is configured for 10GKR or 1GKX according to the Operational Mode Status procedure found in the appropriate Bring Up procedure.