Understanding Jitter and Bit Error for the TLK2500

Richard Prentice *Mixed Signal Products*

ABSTRACT

This document addresses questions about jitter and bit errors when used in conjunction with the Texas Instruments TLK2500IRCP serializer deserializer device.

What is Jitter?

The TLK2500 device is designed to maintain a full-duplex communication link over a controlled impedance media with another TLK2500 device. In other words, two TLK2500s are meant to send data to each other at the same time over two unidirectional channels. Looking at only one direction of the system we see:

- The transmitter, which does the parallel to serial conversion
- The physical media, which may be copper or fiberoptic
- The receiver, which does the serial to parallel conversion

In an ideal system there would be no jittering of the positions of the data bits and no jittering of the clock edges in the system. In such an ideal system the error rate would be exactly zero; there would be no errors.

There is no such thing as an ideal system, however. The edges of the clocks involved do jitter around, and the positions of the data bits do jitter around. It is useful to think of jitter in three places in the system. The transmitter logic is not perfect, and so the positions of the bits jitter around. The media is not perfect, and so the edge transitions that define the bit positions get smeared and jittered around more. The clock strobe in the receiver is not perfect and jitters around, requiring that the data have a certain minimum stability (called the eye opening) so that the receiver can sample the data correctly. All of these jitter components add up to form what is called the jitter budget.

Jitter at the Transmitter

The transmitter converts a parallel data word into a serial data stream at 20 times the speed of the parallel bus. The transmitter generates the serial data stream from an internal high-speed clock. The transmitter generates the internal high-speed clock from the user-supplied GTX_CLK using an internal phase locked loop (PLL). Any PLL will have a certain amount of inherent jitter. In addition, power supply noise will cause PLL jitter. Some of the jitter on the GTX_CLK will also pass through the PLL into the output jitter.

In the TLK2500, the transmit jitter is specified to be less than 0.2 UI (unit intervals) or less if the power supply is clean and the GTX_CLK has less than 40 ps peak-to-peak jitter max.

It was mentioned above that only some of the GTX_CLK jitter will pass through the PLL. In fact, PLLs act like a low-pass filter to input jitter. If a jitter component on the input clock is very sudden, such as one clock cycle to the next clock cycle jitter, the PLL will be too sluggish to respond to the sudden change in the input clock, and the output will have very little jitter passed through from the input jitter event. On the other hand, if the input clock has a low-frequency wander, then the PLL will track that phase wander and all of the input jitter will pass through the PLL to the output. In the TLK2500, the apparent bandwidth of the PLL is approximately 4 to 6 MHz. Input jitter above this frequency will be attenuated and will have a lesser contribution to output jitter.

It was mentioned that the power supply must be clean. In fact, the PLL will act like a high-pass filter to noise on the power supply. A very sudden jump in supply will cause jitter in the output. A very low frequency noise on the power supply will be tracked by the PLL itself and will have negligible effect on the output. The TLK2500 takes care to filter the supply pins to the PLL internally and to compensate for noise as well as possible, but it is still recommended that the one supply pin for the PLL be filtered externally. This filter will be designed to filter out any noise that is dominant in the system, such as ripple from a switching power supply or a strong repeating noise due to a digital bus switching at a certain frequency.

Jitter at the Receiver

The receiver must strobe in the serial data without error. To do this the receiver must internally generate a high-speed clock that is phase-locked to the incoming data stream. As with the transmitter, this internal clock will have some jitter components. As with the transmitter, noise on power supply or reference clock will add jitter to the high-speed clock. (For the TLK2500, the reference clock is also GTX_CLK.) The total jitter on this internal high-speed clock will determine how stable the incoming data must be in order to sample it correctly. Thus the receiver must itself consume some of the jitter budget of the system. This is called the receiver jitter tolerance of the system and sets what the eye opening of the data stream at the receiver must be. The TLK2500 is specified to recover data with up to 50% UI eye closure.

Jitter Induced by Media

The physical media of the system will add jitter. Usually this jitter is in the form of intersymbol interference (ISI). ISI is also called data-dependent jitter because it depends on the exact data pattern that is being transmitted. It is also called deterministic jitter (DJ), because it is determined by the data pattern transmitted. ISI is predominantly a result of the bandwidth of the media, of loss effects of the media, and of the fact that different frequency components of the data may have different propagation velocities through the media.

ISI is generally linear with the length of the media; twice the length of the media means twice as much ISI. There may also be other jitter components in the media, such as in the case of a fiber media. The fiber optic converters at each end of the fiber may contribute a random jitter component as well.

Types of Jitter

Jitter itself may be counted in two ways. There is the deterministic jitter such as ISI. This is perhaps the easiest type of jitter to account for in a system and to add up through the transmitter and media. The fact that it is deterministic means that it is bounded for a particular system and data pattern. Deterministic jitter in the transmitter and media add linearly.

The other type of jitter in a system is random jitter. This type of jitter follows the normal distribution out to many standard deviations. This type of jitter follows the classic *bell jar* shaped distribution.

Random jitter may be characterized by its standard deviation, but that number is not useful in determining the margin in the jitter budget. Random jitter is usually counted as a peak-to-peak number, for a given desired error rate.

The TLK2500 specifies the combination of random jitter and deterministic jitter as *total jitter* from the transmitter.

For example, a desired error rate of 1 bit error out of 10^{12} bits means that the random jitter components be measured as a peak-to-peak value out to 14 standard deviations.

Random jitter components throughout the system are added up by the sum-of-squares method, not linearly. This reflects the fact that if a random jitter event in the transmitter were to jitter a data bit out to the peak in one direction, it is unlikely that a random event in the fiber optic transceiver would also jitter the data bit out to the peak in the same direction at the same time.

If jitter events throughout a system are characterized as random and deterministic, then the total of the random jitter (added by sum of squares) is added to the total of the deterministic jitter (added linearly). This total jitter in the system must be less than the jitter budget. If the jitter budget is just met using peak-to-peak jitter measurements, assuming the peak-to-peak random jitter measurements contain all but 1 out of 10^{12} jitter events, then an error rate of 1 out of 10^{12} for the system can be expected.

Jitter Budget

When the baud rate for a system is chosen, the jitter budget has been chosen. For example, at 2.5 Gbaud the jitter budget is the time allocated for one bit of data, which is 400 ps. This is also called the unit interval or UI. If at any instantaneous point the jitter components in the system add up to more than the unit interval, then there will be an error in the received data. For example, if at a particular point in time the transmitter jittered a bit 110 ps late and the physical media added 210 ps of jitter in that direction and the receiver clock also jittered 110 ps early, then the bit will be sampled incorrectly with a UI = 400 ps.

(110 ps + 210 ps + 110 ps = 430 ps > 400 ps).

In a standardized system such as Fibre Channel, jitter specifications are set for each component of the system so that components from different vendors may be guaranteed to interoperate. In fact, it really does not matter to the receiver how the jitter numbers add up; if the sum of the jitter components is larger than the UI, then there will be an error. It does not matter if most of the jitter came from the transmitter or the media or the receiver; the sum must still be less than the UI.

In a proprietary system designed around two TLK2500s, the system designer has the freedom to choose the UI and to budget the jitter appropriately. If a better error rate is desired, the designer will be more conservative in allocating the jitter budget.

For example, suppose the UI = 400 ps. Suppose the transmitter is specified to contribute 80 ps max of jitter with a clean power supply and a clean GTX_CLK. (A clean GTX_CLK has less than 40 ps max jitter peak to peak). Suppose the receiver is specified to require 200 ps eye opening with clean power supply and clean GTX_CLK. Further suppose that the distance of the media is known to be 20 meters. (We only assume 20 m because it can be considered a long link that requires a very high-grade copper or a fiber optic link. For the purposes of this example, it would be easy to have too much jitter for the jitter budget with a 20 m copper link at this baud rate.)

In this example see Figure 1, the jitter budget requires that the media contribute less than 120 ps of jitter max. Any more jitter than 120 ps, the error rate will suffer. If the jitter from the media is much less than 120 ps, then the error rate will approach zero. If a low error rate were desired, then the designer might choose a fiber optic media or a very high-grade copper media.

Suppose the designer chose a type of media that only contributed 70 ps of jitter over the maximum length of media. In the above example, there is 50 ps of margin in the jitter budget, and the error rate would be very low. If error rate were a prime concern, then this would be a good system design. If cost were a prime concern, then the designer might prefer to use the margin in the jitter budget to reduce cost. The designer might find a cheaper grade of media that had more jitter. The designer might find a cheaper clock source for GTX_CLK that caused more transmit jitter. Or the designer might spend less on the power supply filtering and cause more transmit jitter and less receive jitter tolerance.

Conclusion

In short, the designer has the flexibility to set the budget for the jitter when he picks the baud rate and he has the flexibility to spend that jitter budget as he sees fit. For a better error rate, allow less jitter in the system by using better media and better clock sources and better power supplies, and design for shorter lengths of media, if possible. For cheaper systems, make provision for slower baud rate, or shorter lengths, or higher error rates. There are few absolutes, and they are:

- You can not allow more jitter in a system than the UI, or errors will result.
- The transmitter in the TLK2500 is specified to consume 0.16 to 0.2 UI (date rate dependent) of the budget, but could be worse if data sheet conditions for GTX_CLK and power supply are not met.
- The receiver of the TLK2500 is specified to consume 0.50 UI of the budget (will recover up to 50% eye closure), but could be worse if data sheet conditions for GTX_CLK and power supply are not met.

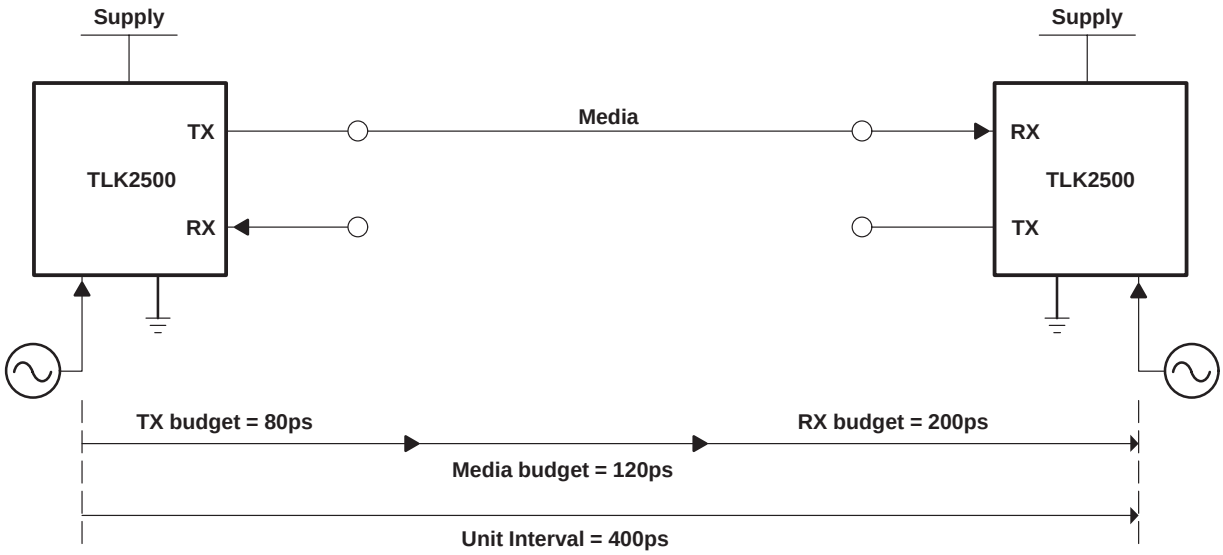

Figure 1. Jitter Example

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