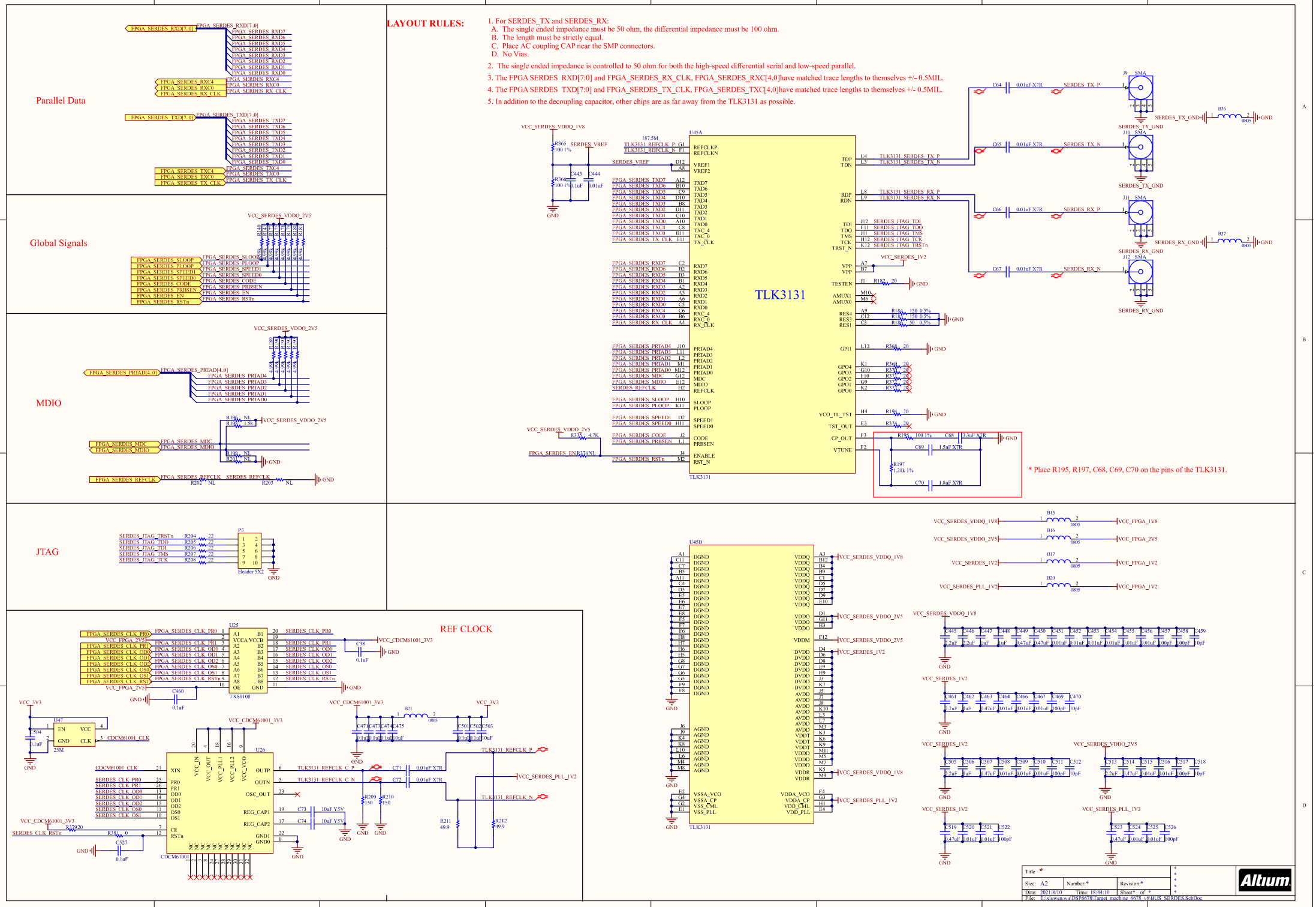
Parallel Data
Global Signals
MDIO
JTAG
REF CLOCK
LAYOUT RULES:
1. For SERDES_TX and SERDES_RX:
A. The single ended impedance must be 50 ohm, the differential impedance must be 100 ohm.
B. The length must be strictly equal.
C. Place AC coupling CAP near the SMP connectors.
D. No Vias.
2. The single ended impedance is controlled to 50 ohm for both the high-speed differential serial and low-speed parallel.
3. The FPGA SERDES RXD[7:0] and FPGA_SERDES_RX_CLK, FPGA_SERDES_RXC[4,0]have matched trace lengths to themselves +/- 0.5MIL.
4. The FPGA SERDES TXD[7:0] and FPGA_SERDES_TX_CLK, FPGA_SERDES_TXC[4,0]have matched trace lengths to themselves +/- 0.5MIL.
5. In addition to the decoupling capacitor, other chips are as far away from the TLK3131 as possible.
TLK3131
* Place R195, R197, C68, C69, C70 on the pins of the TLK3131.
Title *
Size: A2
Number:*
Revision:*
Date: 2021/8/10
Time: 18:44:10
Sheet* of *
File: E:\xiuwen.wu\DSP\6678\Target_machine_6678_v6\BUS_SERDES.SchDoc
Altium