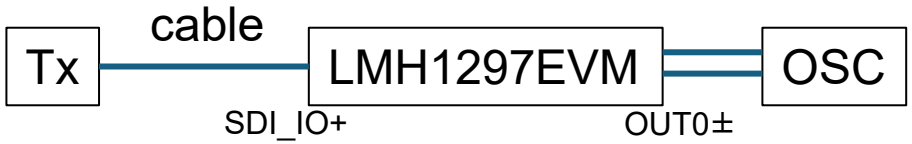


Step1: check the CEI(EQ adaptation result)

Setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0025	2C	1	CHECK | ConfigIO | Cable EQ Index(default=0x00)
END					

Status check

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0001	13	1	CHECK | EQ Observation Status
RD8	2D	0002	C8	1	CHECK | Rate and Driver Observation Status
END					

[2]=0 ➡ not sleep mode

OUT0's eye is opening.

Step2: EQ manual setting

Setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0000	08	1	CHECK | ConfigIO/reg_power_save(default=0x08)
WR8	2D	0000	48	1	SET | ConfigIO | Disable EQ adaptation
RD8	2D	0000	48	1	CHECK
RD8	2D	0024	00	1	CHECK | ConfigIO/Reserved(delault=0x00)
WR8	2D	0024	2C	1	SET | ConfigIO | Write to the EQ value
RD8	2D	0024	2C	1	CHECK
RD8	2D	0025	2C	1	CHECK | ConfigIO/Read back CEI value
END					

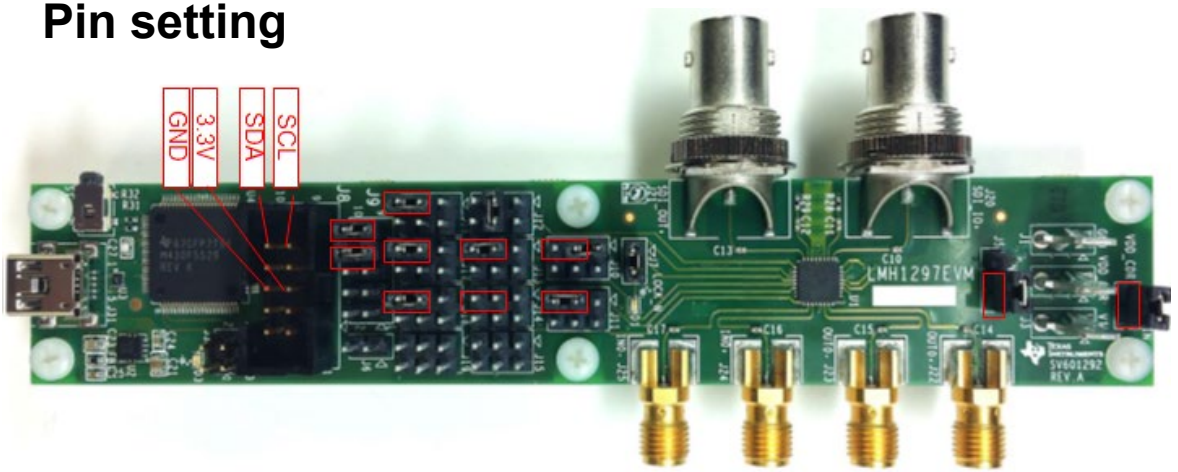
Status check

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0001	12	1	CHECK | EQ Observation Status
RD8	2D	0002	CB	1	CHECK | Rate and Driver Observation Status
END					

[2]=0 ➡ not sleep mode

OUT0's eye is closing. The signal level is 0V.

Pin setting



Step3: Sequence of "OUT0 Raw Data"

(outlined in 3.13.2.4 in LMH1297 programming guide)

Setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select
WR8	2D	00FF	04	1	SET | Share/page_select | CTLE/CDR Register Page
RD8	2D	00FF	04	1	CHEK
RD8	2D	0009	00	1	CHECK | Enable Independent Output Control Override (default=0x00)
RD8	2D	001C	18	1	CHECK | OUT_CTRL functionality to default settings (default=0x18, [3:2]=[10])
RD8	2D	001E	09	1	CHECK | Output Raw data (EQ only) on OUT0 (default=0x09, [7:4]=[0000], [3:0]=[1001])
WR8	2D	0009	20	1	SET | [5]=1
WR8	2D	001C	18	1	SET | [3:2]=[10]
WR8	2D	001E	09	1	SET | [7:5]=000
RD8	2D	0009	20	1	CHECK
RD8	2D	001C	18	1	CHECK
RD8	2D	001E	09	1	CHECK
END					

Status check

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	04	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0001	16	1	CHECK | EQ Observation Status
RD8	2D	0002	CB	1	CHECK | Rate and Driver Observation Status
END					

[2]=0 ➡ not sleep mode

OUT0's eye is closing. The signal level is 0V.

Step1: Reset (power off ->on)

Step2: Check the CEI(EQ adaptation result)

Setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0025	2C	1	CHECK | ConfigIO | Cable EQ Index(default=0x00)
END					

Status check

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0001	13	1	CHECK | EQ Observation Status
RD8	2D	0002	C8	1	CHECK | Rate and Driver Observation Status
END					

[2]=0 ➡ not sleep mode

OUT0's eye is opening.

Step3: Sequence of "Force Carrier Detect Power Down" (outlined in 3.3 in LMH1297 programming guide)

Setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	00	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	Set | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	001D	00	1	CHECK | ConfigIO | EQ Carrier Detect(default=0x00)
WR8	2D	001D	80	1	SET | ConfigIO | EQ Carrier Detect/ Enable Override for
WR8	2D	001D	C0	1	SET | ConfigIO | EQ Carrier Detect/ Detect Off for SDI
RD8	2D	001D	C0	1	CHECK
END					

Status check

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select(default=0x00)
WR8	2D	00FF	05	1	SET | Share/page_select | ConfigIO Page
RD8	2D	00FF	05	1	CHECK
RD8	2D	0001	80	1	CHECK | EQ Observation Status
RD8	2D	0002	C7	1	CHECK | Rate and Driver Observation Status
END					

[2]=1 ➡ sleep mode

OUT0's eye is closing. The signal level is 0V.

Before EQ manual setting

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	00	1	CHECK | Share/page_select
WR8	2D	00FF	04	1	SET | Share/page_select | CTLE/CDR Register Page
RD8	2D	00FF	04	1	CHEK
RD8	2D	0054	80	1	CHECK | Interrupt Status Register Override (default=:0x00)
END					

0x54[7] is 1.

After

Command	Dev. Addr	Reg. Addr	Data	# of Byte	コメント
RD8	2D	00FF	05	1	CHECK | Share/page_select
WR8	2D	00FF	04	1	SET | Share/page_select | CTLE/CDR Register Page
RD8	2D	00FF	04	1	CHEK
RD8	2D	0054	00	1	CHECK | Interrupt Status Register Override (default=:0x00)
END					

0x54[7] is 0.

It seems that some settings related to Carrier Detect are being changed by the EQ manual setting sequence, which is causing OUT0 to be disabled.

4.2 CTLE/CDR Register Page

0x54	Interrupt Status Register	7	cardet	0x00	R	0 = Carrier Detect from the selected input deasserted 1 = Carrier Detect from the selected input asserted
		6	cdr_lock_int		R	0 = No interrupt from CDR Lock 1 = CDR Lock Interrupt Note: Clears when Reg 0x54 is read-back.
		5	carrier_det0_int		R	0 = No interrupt from IN0 Carrier Detect 1 = IN0 Carrier Detect Interrupt Note: Clears when Reg 0x54 is read-back.
		4	carrier_detIO_int		R	0 = No interrupt from SDI_IO Carrier Detect 1 = SDI_IO Carrier Detect Interrupt Note: Clears when Reg 0x54 is read-back.
		3	heo_veo_int		R	0 = No interrupt from HEO/VEO 1 = HEO/VEO Threshold Reached Interrupt Note: Clears when Reg 0x54 is read-back.
		2	cdr_lock_loss_int		R	0 = No interrupt from CDR Lock 1 = CDR Loss of Lock Interrupt Note: Clears when Reg 0x54 is read-back.
		1	carrier_det0_loss_int		R	0 = No interrupt from IN0 Carrier Detect Loss 1 = IN0 Carrier Detect Loss Interrupt Note: Clears when Reg 0x54 is read-back.
		0	carrier_detIO_loss_int		R	0 = No interrupt from SDI_IO Carrier Detect Loss 1 = SDI_IO Carrier Detect Loss Interrupt Note: Clears when Reg 0x54 is read-back.