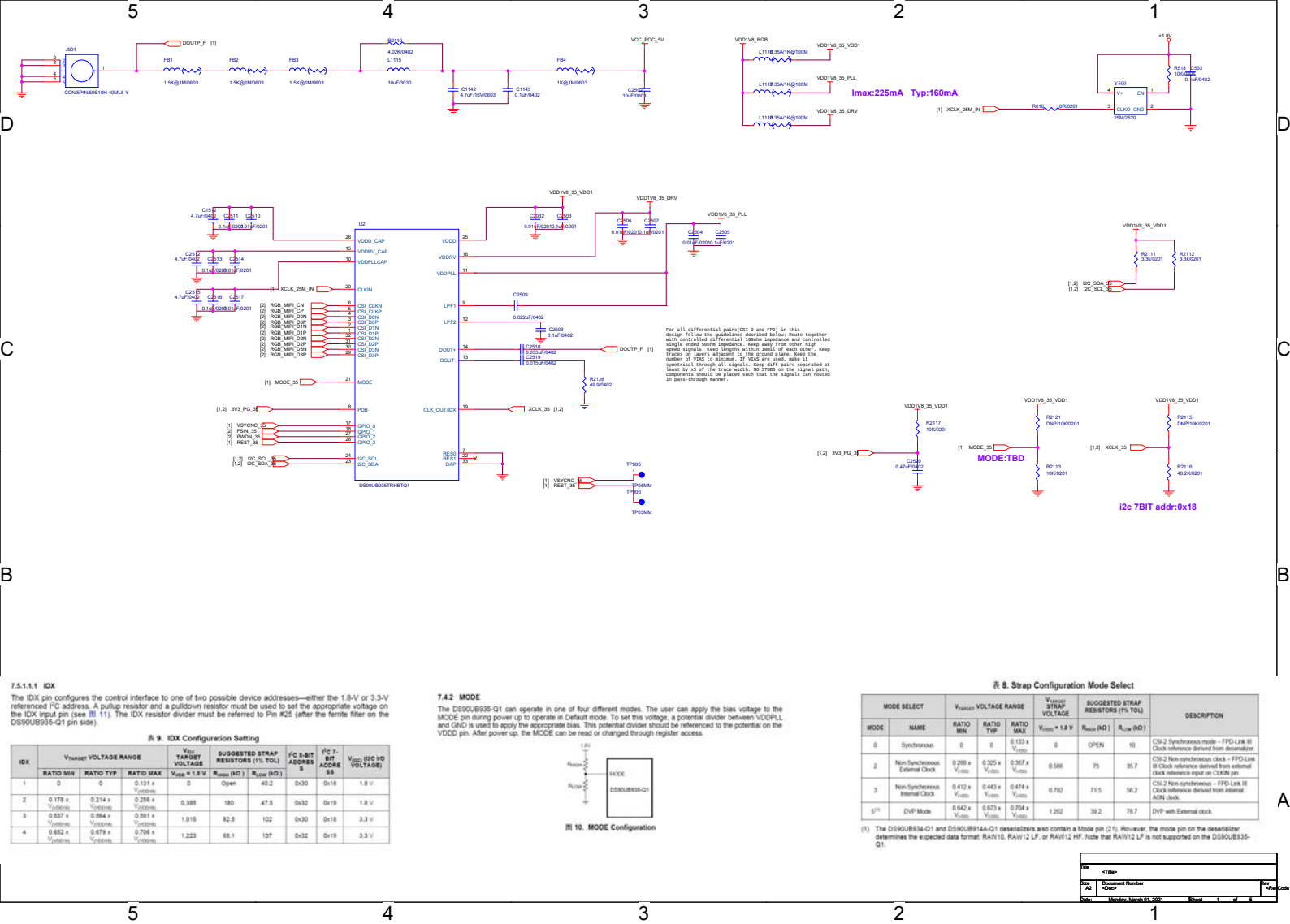


7.5.1.1.1 IDX

The IDX pin configures the control interface to one of two possible device addresses—either the 1.8-V or 3.3-V referenced I²C address. A pullup resistor and a pulldown resistor must be used to set the appropriate voltage on the IDX input pin (see 图 11). The IDX resistor divider must be referred to Pin #25 (after the ferrite filter on the DS90UB935-Q1 pin side).

表 9. IDX Configuration Setting

IDX	V_{TARGET} VOLTAGE RANGE			V_{DD} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		I²C 8-BIT ADDRESS	I²C 7-BIT ADDRESS	V_{IDD} (I2C I/O VOLTAGE)
	RATIO MIN	RATIO TYP	RATIO MAX	V_{DD} = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)			
1	0	0	0.131 x $V_{VDD(1V8)}$	0	Open	40.2	0x30	0x18	1.8 V
2	0.178 x $V_{VDD(1V8)}$	0.214 x $V_{VDD(1V8)}$	0.256 x $V_{VDD(1V8)}$	0.385	180	47.5	0x32	0x19	1.8 V
3	0.537 x $V_{VDD(1V8)}$	0.564 x $V_{VDD(1V8)}$	0.591 x $V_{VDD(1V8)}$	1.015	82.5	102	0x30	0x18	3.3 V
4	0.652 x $V_{VDD(1V8)}$	0.679 x $V_{VDD(1V8)}$	0.706 x $V_{VDD(1V8)}$	1.223	68.1	137	0x32	0x19	3.3 V

7.4.2 MODE

The DS90UB935-Q1 can operate in one of four different modes. The user can apply the bias voltage to the MODE pin during power up to operate in Default mode. To set this voltage, a potential divider between VDDPLL and GND is used to apply the appropriate bias. This potential divider should be referenced to the potential on the VDDD pin. After power up, the MODE can be read or changed through register access.

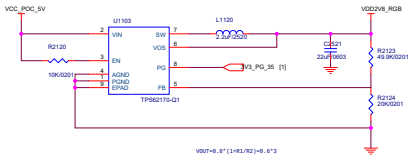
图 10. MODE Configuration

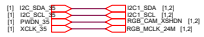
表 8. Strap Configuration Mode Select

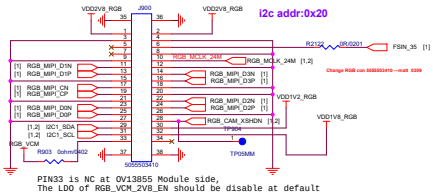
MODE SELECT		V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		DESCRIPTION
MODE	NAME	RATIO MIN	RATIO TYP	RATIO MAX	$V_{VDD(1V8)}$ = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	Synchronous	0	0	0.133 x $V_{VDD(1V8)}$	0	OPEN	10	CSI-2 Synchronous mode – FPD-Link III Clock reference derived from deserializer.
2	Non-Synchronous External Clock	0.288 x $V_{VDD(1V8)}$	0.325 x $V_{VDD(1V8)}$	0.367 x $V_{VDD(1V8)}$	0.586	75	35.7	CSI-2 Non-synchronous clock – FPD-Link III Clock reference derived from external clock reference input on CLKIN pin.
3	Non-Synchronous Internal Clock	0.412 x $V_{VDD(1V8)}$	0.443 x $V_{VDD(1V8)}$	0.474 x $V_{VDD(1V8)}$	0.792	71.5	56.2	CSI-2 Non-synchronous – FPD-Link III Clock reference derived from internal AON clock.
5(1)	DVP Mode	0.642 x $V_{VDD(1V8)}$	0.673 x $V_{VDD(1V8)}$	0.704 x $V_{VDD(1V8)}$	1.202	39.2	78.7	DVP with External clock.

(1) The DS90UB934-Q1 and DS90UB914A-Q1 deserializers also contain a Mode pin (21). However, the mode pin on the deserializer determines the expected data format: RAW10, RAW12 LF, or RAW12 HF. Note that RAW12 LF is not supported on the DS90UB935-Q1.

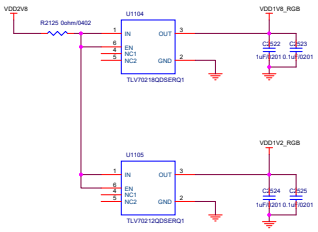
Title	<Title>		
Size A2	Document Number <Doc>		Rev <RevCode>
Date: Monday, March 01, 2021	Sheet 1 of 5		







PIN33 is NC at OV13855 Module side,
The LDO of RGB_VCM_2V8_EN should be disable at default



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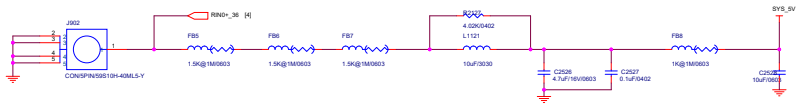
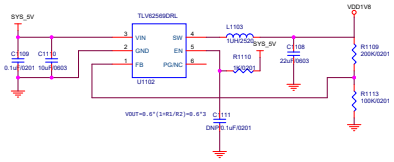
Date: Monday, March 01, 2021	Sheet 2 of 5		





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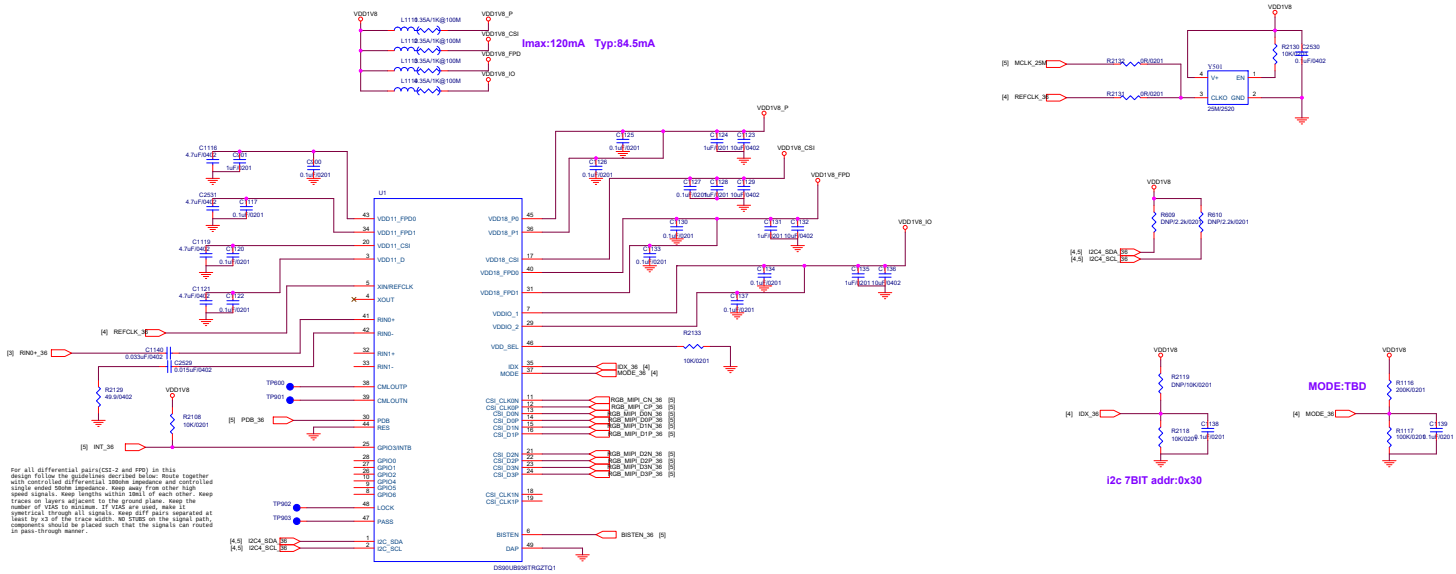
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, March 01, 2021	Sheet 3 of 5	



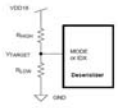


图 14. Strap Pin Connection Diagram

表 2. Strap Configuration Mode Select

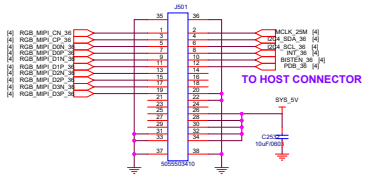
MODE NO.	V_{TARGET} VOLTAGE RANGE			V_{TARGET} STRAP VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		RX MODE
	V_{MIN}	V_{TYP}	V_{MAX}	VDD18 = 1.8 V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	CSI-2 non-synchronous back channel
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	RAW12 LF
	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	RAW12 HF
	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	RAW10
	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	CSI-2 synchronous back channel

The strapped values can be viewed and modified in the following locations:

- RX Mode – Port Configuration FPD3_MODE (Register 0x6D[1:0])
- Clock Mode – Device Status and CSI_PLL_CTL (Register bits 0x04[4] and 0x1F[3])

表 15. Serial Control Bus Addresses for IDX

NO.	V_{IDX} VOLTAGE RANGE			V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% TOL)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{MIN}	V_{TYP}	V_{MAX}	(V): VDD1P8 = 1.80V	R_{HIGH} (kΩ)	R_{LOW} (kΩ)	7-BIT	8-BIT
0	0	0	0.131 × $V_{(VDD18)}$	0	OPEN	10.0	0x30	0x60
1	0.179 × $V_{(VDD18)}$	0.213 × $V_{(VDD18)}$	0.247 × $V_{(VDD18)}$	0.374	88.7	23.2	0x32	0x64
2	0.296 × $V_{(VDD18)}$	0.330 × $V_{(VDD18)}$	0.362 × $V_{(VDD18)}$	0.582	75.0	35.7	0x34	0x68
3	0.412 × $V_{(VDD18)}$	0.443 × $V_{(VDD18)}$	0.474 × $V_{(VDD18)}$	0.792	71.5	56.2	0x36	0x6C
4	0.525 × $V_{(VDD18)}$	0.559 × $V_{(VDD18)}$	0.592 × $V_{(VDD18)}$	0.995	78.7	97.6	0x38	0x70
5	0.642 × $V_{(VDD18)}$	0.673 × $V_{(VDD18)}$	0.704 × $V_{(VDD18)}$	1.202	39.2	78.7	0x3A	0x74
6	0.761 × $V_{(VDD18)}$	0.792 × $V_{(VDD18)}$	0.823 × $V_{(VDD18)}$	1.420	25.5	95.3	0x3C	0x78
7	0.876 × $V_{(VDD18)}$	$V_{(VDD18)}$	$V_{(VDD18)}$	1.8	10.0	OPEN	0x3D	0x7A



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Size A2	Document Number <Doc>	Rev <RevCode>
Date: Monday, March 01, 2021	Sheet 5 of 5	