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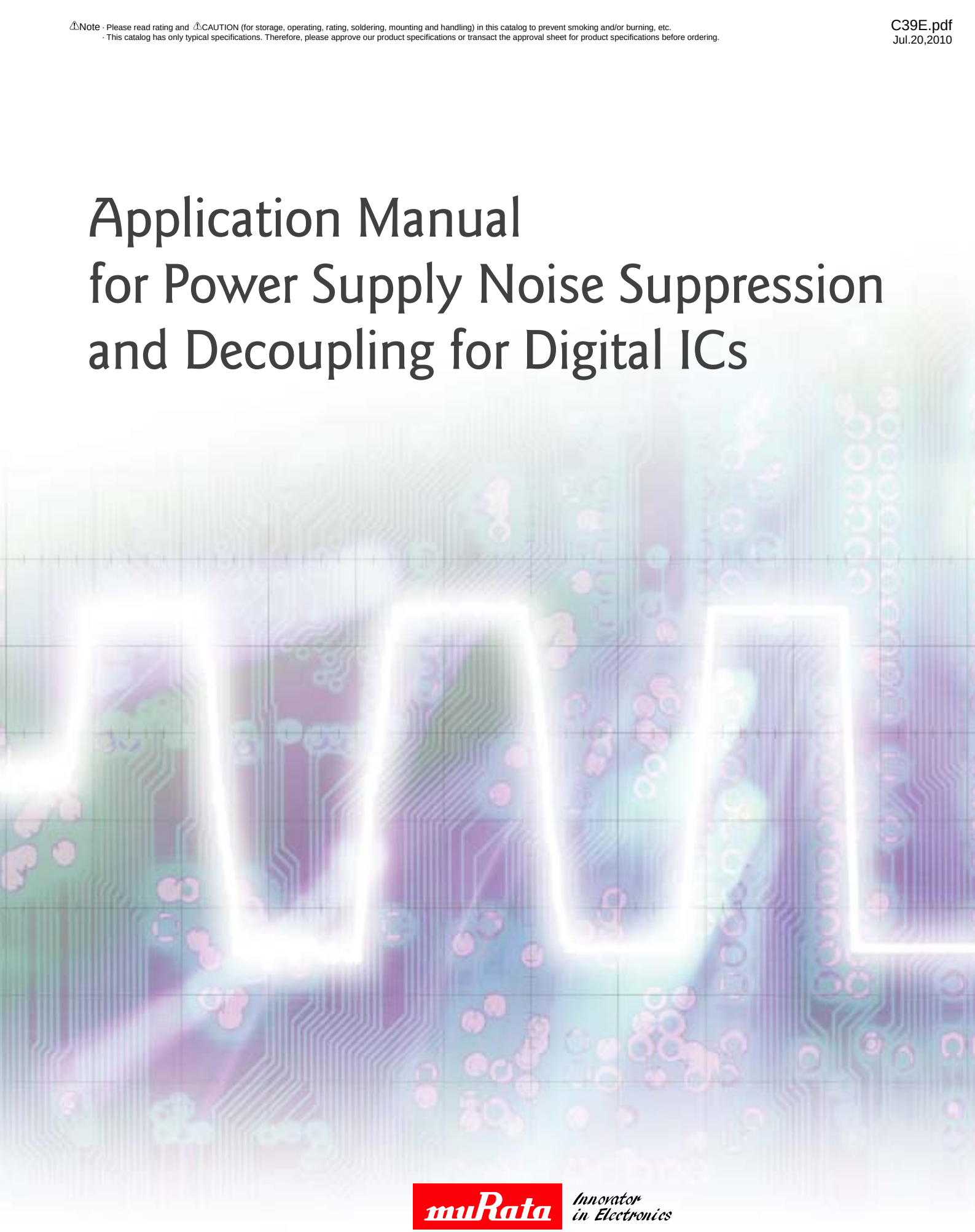
Application Manual for Power Supply Noise Suppression and Decoupling for Digital ICs



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Contents

1. Introduction

Various capacitors and EMI suppression filters are used for power supplies connected to digital ICs as shown in Figure 1-1. By forming a decoupling circuit acting as a filter as shown in Figure 1-2, at the junction connecting an IC's power source terminal and power distribution network (PDN), power integrity (PI) can be improved. [1) 2)]

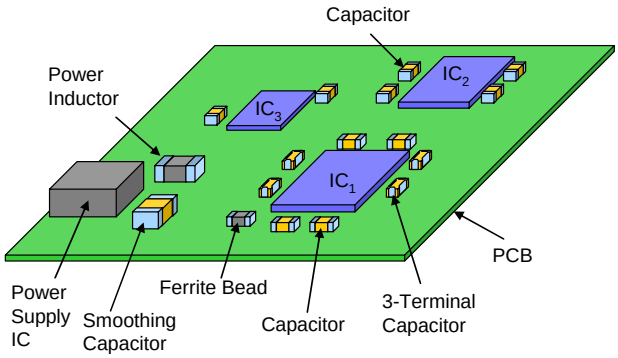


Figure 1-1 An example of noise suppression products used for digital IC power supply

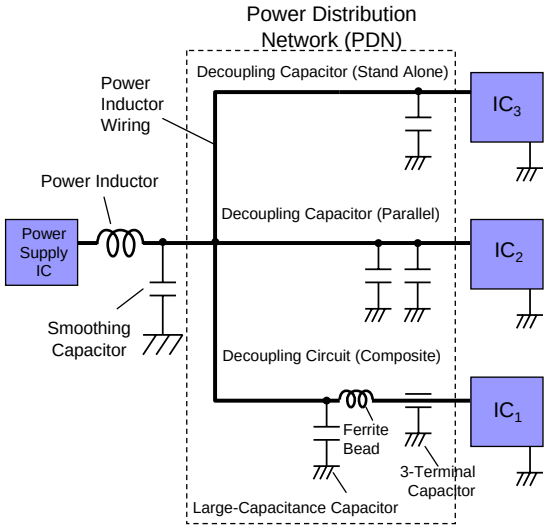


Figure 1-2 An example of wiring connection for digital IC power supply

As shown in Figure 1-3, this decoupling circuit performs functions such as:

(1) suppressing noise generated by or entering an IC,
(2) providing transient current associated with IC operations and maintaining voltage and
(3) becoming a part of signal path. [3) 4) 5)]

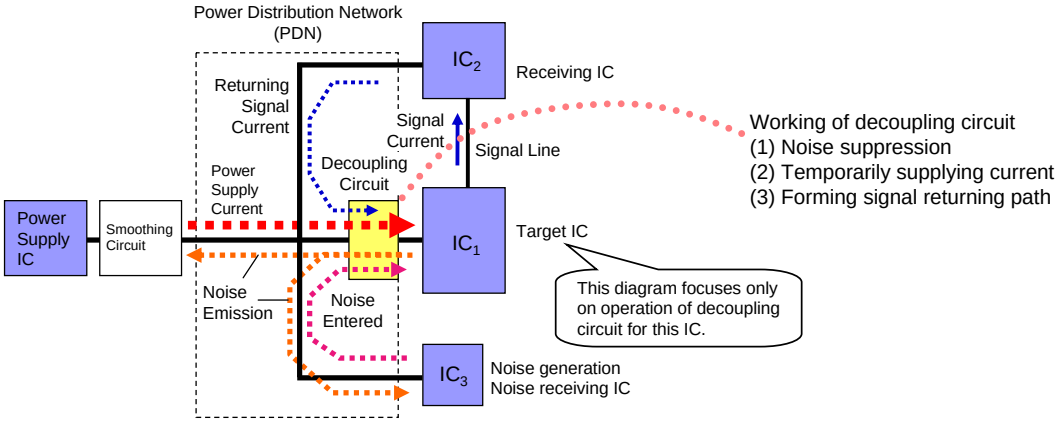
When this circuit is not fully functional, the following problems may occur, as shown in Figure 1-4:

(1) interference with other circuits (such as IC_3) or increasing the noise emission of the equipment due to noise leakage,
(2) intrusion of noise from an external source causing problems with IC operation,
(3) power supply voltage fluctuation, interfering with IC operations, lowering signal

integrity, and increasing the noise superimposing over signals, and

(4) reduced signal integrity due to insufficient return circuit of the signal current.

Therefore, formation of an appropriate decoupling circuit is important for both noise suppression and circuit operations.



Working of decoupling circuit	Main performance indicators	Target frequencies 1kHz 1MHz 1GHz	Examples of noise problem and evaluation criteria
(1) Noise suppression	Insertion loss (Permeability constant/attenuation)		Noise measurement (Terminal voltage, radiated electric field, near magnetic field distribution)
(2) Current supply	Impedance (reflection coefficient)		Voltage fluctuation, transient voltage response
(3) Signal path			Signal waveform (eye diagram)

Figure 1-3 Working of the power supply filter (decoupling circuit) when focusing on IC_1

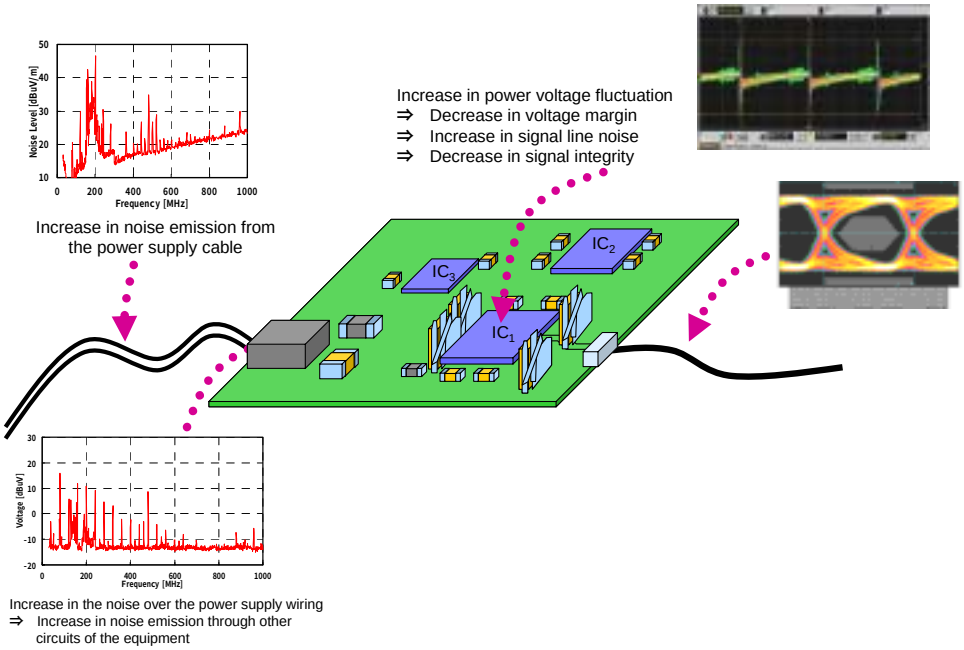


Figure 1-4 An example of influence by power supply noise

With a circuit with relatively low clock speed, or a circuit with a large margin against noise, this decoupling circuit can be easily formed by locating a bypass capacitor, connecting the power supply to the ground near the power supply terminal. In this manual, this bypass capacitor is called a decoupling capacitor. However, a more sophisticated decoupling circuit is needed for ICs with higher clock speed, ICs generating large amounts of noise, and noise-sensitive ICs.

This manual aims to explain the workings of components for power supplies and how you may appropriately select components, in order to design this high-performance decoupling circuit. (However, the smoothing circuit in Figure 1-3 is excluded.)

Typically, performance of a decoupling circuit is assessed mainly with insertion loss from the viewpoint of noise suppression in Figure 1-3 (1), and with impedance from the viewpoint of (2) current supply, and (3) signal path formation. Since these two viewpoints differ, the first half of this manual (Chapters 2 through 5) will focus on noise suppression performance, and offer explanations based on insertion loss as an indicator. The second half of this manual (Chapters 6 through 8) will focus on current supply performance, and offer explanations based on impedance as an indicator.

2. Generation of power supply noise from digital ICs and configuration of decoupling circuits

We will first describe the mechanism of power supply noise generation for digital ICs, configuration of general decoupling circuits for handling such noise, and provide an overview of the circuit characteristics pertaining to decoupling circuits (power supply filters) covered in this manual.

2.1 Mechanism of power source noise generation

A simplified model of a C-MOS circuit mainly used for digital ICs is shown in Figure 2-1. For the purpose of simplicity, the working of the C-MOS transistor on the driver side is represented as a switch, and gate capacitance of the C-MOS transistor on the receiver side is represented as a capacitor connected to a ground. With a C-MOS digital IC, by this switch on the driver side connecting the signal line with either the power supply side (VDD) or the ground side (GND), the signal output level can be set to be “1” or “0” respectively.[6)]

Normally, if the signal level does not change for the power supply of the C-MOS digital circuit, there is hardly any current flow. However, if charge current at the gate capacitance (when the signal level switches from “0” to “1”) and discharge current (when the signal level switches from “1” to “0”) pulsates through the signal line as shown in Figure 2-1, current consequently flows through the power supply and ground. Further, aside from this current, a so-called through current flows from the driver power supply to the ground briefly when the signal switches. Through current also becomes a cause for the pulsating current flowing through power supplies and grounds.

Since these currents pulsate very acutely, they contain a very wide range of frequency components causing noise failures when a part of its energy is radiated externally. Also, since an acute change in current causes variance in power supply voltage due to inductance of the power supply and the ground patterns, it causes instability in the operations of peripheral circuits sharing the common power supply. [7) 8)]

Therefore, it is necessary to seal the current around ICs (to decouple ICs with peripheral circuits) so that noise emission can be suppressed and voltage fluctuation would not affect peripheral circuits. Meanwhile, since fluctuation in power supply voltage would make the operation of the IC emitting the noise itself unstable, it is necessary to contain noise-related power supply voltage fluctuation to an acceptbale level. The decoupling circuit illustrated in Figure 1-3 is used for such a purpose.

Although the model used for Figure 2-1 considers gate capacitance with regard to the ground for the purpose of simplicity, and charge current and discharge current are considered to flow through the ground, in actuality gate capacitance occurs with regard to the power supply as well, necessitating consideration of the case where charge current and discharge current flow through the power supply.

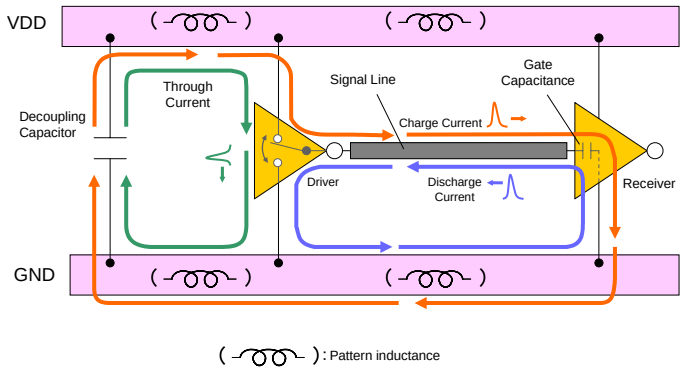


Figure 2-1 Simplified model of a digital IC

Ordinarily, in order to contain the current flowing through the power supply around the IC, a bypass is formed (an inductor may be combined as described later) by mounting a capacitor between the power supply and the ground as seen in Figure 2-1. This capacitor is called a decoupling capacitor. In order to form an effective decoupling circuit it is important to:

(1) form a bypass that can function under high frequency (using a capacitor with small impedance),

(2) strictly limit the range current flows through (by placing the capacitor near the IC), and

(3) keep the pattern inductance small (especially between the IC and the capacitor).

An example of capacitor location and power source pattern configuration that take these points into consideration are shown in Figure 2-2. (With this example, it can be wired in a single layer under the IC.)

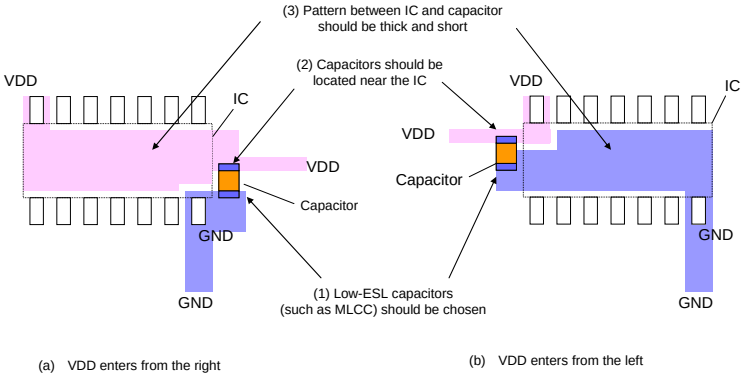


Figure 2-2 An example of decoupling capacitor positioning

Wiring rules for the cases where such an ideal placement is difficult or a higher performance decoupling circuit is necessary are described in Chapter 3 and later in this manual.

2.2 Various ways to view the noise and evaluation criteria

There are several measuring methods for evaluating performance of decoupling circuits, depending on the specific purpose. As described in Figure 1-3 of Chapter 1, decoupling circuits have three roles, namely (1) noise suppression, (2) temporarily supplying current

and (3) forming the signal returning path.

Out of these roles, “(1) noise suppression” pertains to the filtering out of noise leaking from the power supply from the IC and shutting off the noise coming in from an external source. A measurement taken at the opposite side of the noise source of the decoupling circuit is used to evaluate this performance as shown in Figure 2-3. In other words, when questioning the noise leaking out of the IC, measurement is taken on the PDN (point A) side, and when questioning the noise coming in to ICs from an external source, measurement is taken at the power supply terminal for the IC (point B).

Measurement criteria include a voltage waveform observed by an oscilloscope and voltage spectrum measured by a spectrum analyzer. This manual indicates data obtained in an empirical fashion. Meanwhile, when focusing on comparing decoupling circuit performances, insertion loss characteristics are used as opposed to measuring voltage and spectrum in actual circuits. [9] A network analyzer is used to measure insertion loss. Since measurement conditions are predetermined, results are highly reproducible, making this method suitable for comparing component performances. Decoupling circuit performances are compared mainly with these insertion loss characteristics in this manual. The measurement method of this insertion loss will be described in Section 2.3.

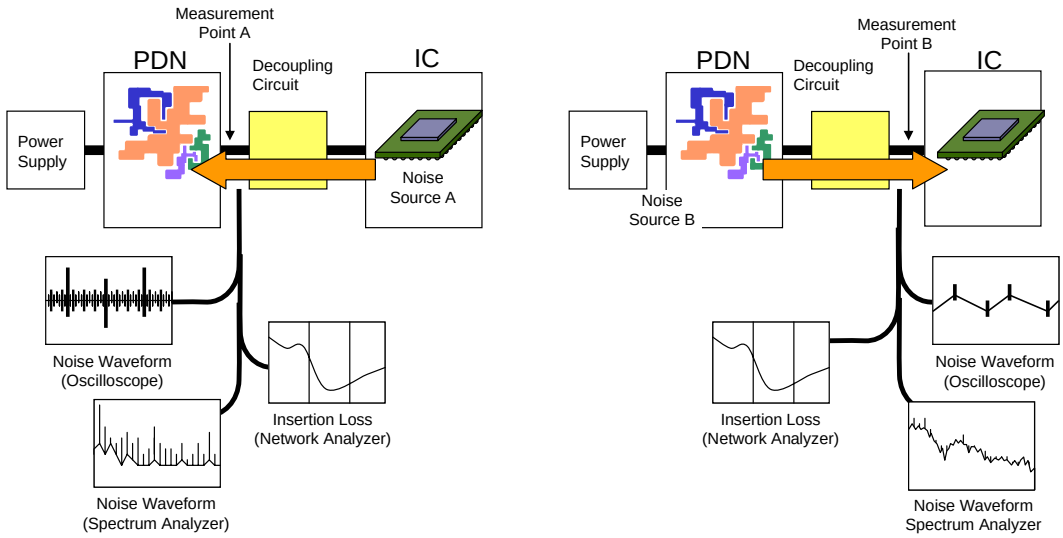


Figure 2-3 Various measurement criteria for observing noise suppression performance

On the other hand, there are cases where filter performance is evaluated from the viewpoints of (2) temporarily supplying current and (3) forming signal returning path as shown in Figure 1-3. In these cases, stabilizing the power supply voltage when IC current fluctuates or securing the signal integrity are the issues as shown in Figure 2-4. Therefore, measurement point B’ on the power supply terminal side of the IC and measurement point C at the signal output terminal are used for measurement locations as indicated in Figure 2-4.

Measurement criteria for point B’, located at the power supply, include noise waveform, spectrum, and impedance, and for point C, located where the signal is, include jitter and

spectrum. When focusing on comparing decoupling circuit performances, highly reproducible impedance characteristics are used. Impedance is the criterion covered mainly in this manual.

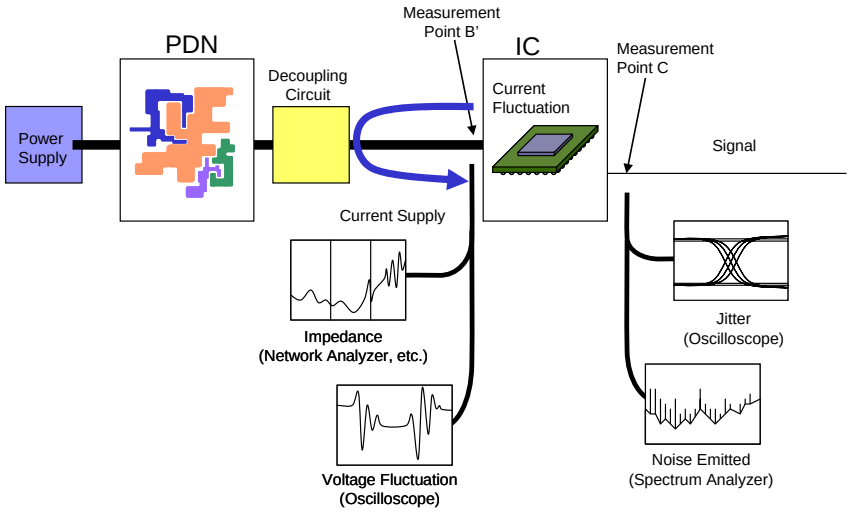


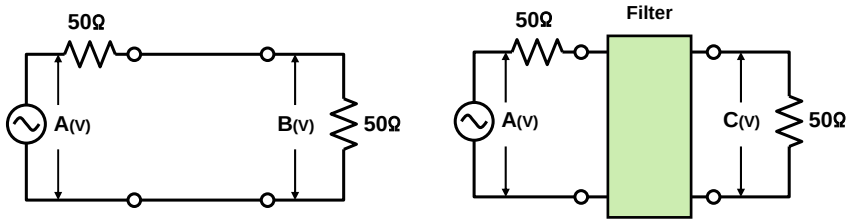
Figure 2-4 Measurement to evaluate current supply performance

2.3 Measurement method for insertion loss

Normally, noise filter performance is expressed in terms of insertion loss. [6] Since decoupling circuits used for power supplies are a type of noise filter, their noise suppression performance can be described in terms of their insertion loss.

The measurement circuit for insertion loss is indicated in Figure 2-5. Insertion loss (I.L.) is described by the effect of a filter mounted on a circuit with 50Ω impedance observed as the difference in output voltage before and after mounting the filter in dB. The larger the insertion loss, the more effective the noise suppression is.

Insertion loss may be substituted by the oscillation of transmission coefficient (S_{21}) for S parameter measured for the 50Ω system. (Note that insertion loss and S_{21} will have the opposite positive and negative sign.)



$$\text{Insertion Loss} = 20 \log \left| \frac{B}{C} \right| (\text{dB}) \qquad (2\text{-}1)$$

Figure 2-5 Insertion Loss Measurement Circuit

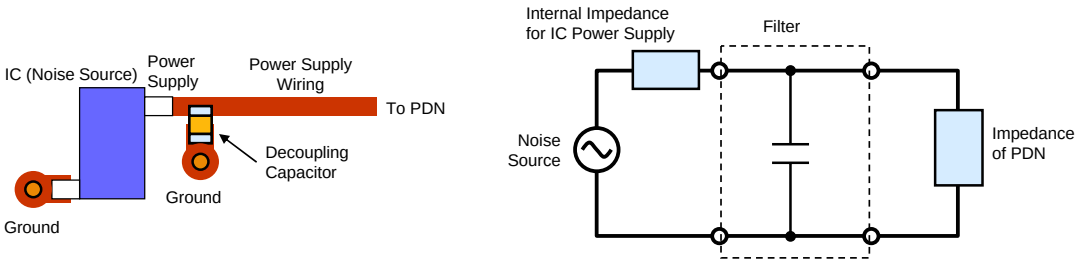
2.4 Bypass (decoupling) capacitor

Next, a basic configuration of a decoupling circuit is introduced. One of its components is a decoupling capacitor shown in Figure 2-1.

When a decoupling capacitor is used for the power supply terminal of an IC, as shown in Figure 2-6 (a), a bypass capacitor from the power supply to the ground is formed as a filter, as seen in Figure 2-6 (b). We will assume that this will be used on a multilayer substrate, and the ground for the IC and the capacitor will be connected to the ground plane with a via.

Insertion loss, in this case, would be greater as capacitor impedance becomes less. Since capacitor impedance decreases inversely in proportion to frequency, this filter becomes a low pass filter where insertion loss is large at high frequency.

Filter characteristics shown in Figure 2-6, vary depending on the internal impedance of IC power supply or PDN impedance in an actual circuit. Since impedance must be fixed when comparing filter performances, it is common to set impedance at 50Ω when taking the measurement, as shown in Figure 2-5. The filter's characteristics when mounted on an actual circuit are estimated from the measurement result at 50Ω.



(a) Decoupling capacitor (b) Filter circuit

Figure 2-6 Filter circuit with decoupling capacitor

Theoretical value of a bypass capacitor's insertion loss characteristics measured at 50Ω is shown in Figure 2-7. As the capacitance of a capacitor becomes larger, or the frequency becomes higher, the capacitor's insertion loss increases linearly. This corresponds with the fact that the capacitor impedance decreases inversely in proportion to frequency, therefore indicating that capacitors with larger capacitance would basically show a superior noise suppression effect.

Insertion loss is expressed in dB as shown in figure 2-5. When frequency or capacitance is increased tenfold, the insertion loss would increase by 20dB.

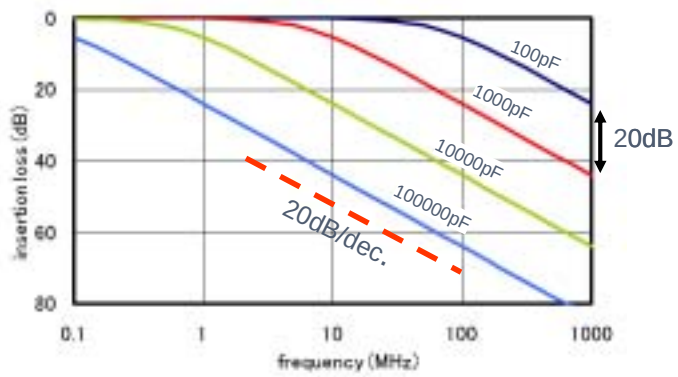


Figure 2-7 Insertion loss characteristics of capacitor (theoretical values)

The actual characteristics of the capacitor's insertion loss are as indicated in Figure 2-8. In the high frequency range over 10MHz, insertion loss decreases as frequency increases. This is considered to be due to the fact that insertion loss is limited by a minute inductance component (ESL) and resistance component (ESR) contained in the capacitor, as described later. This indicates that in order to form a decoupling circuit with excellent noise suppression performance at high frequency, we must use a capacitor with small ESL and ESR.

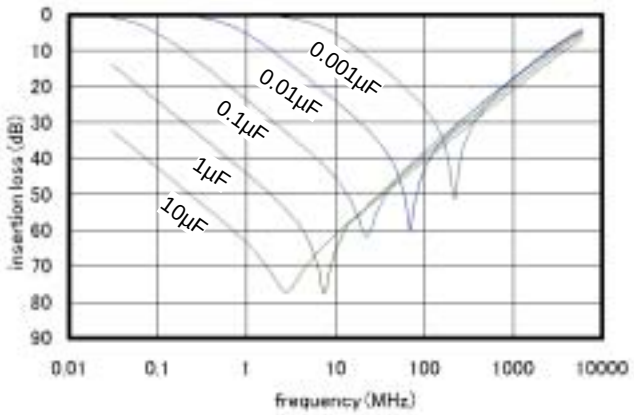


Figure 2-8 Insertion loss characteristics of capacitor (Converted from Data in Murata Chip S-Parameter & Impedance Library)

2.5 Inductors, ferrite beads

In addition to the bypass capacitor described above, inductors such as ferrite beads can be inserted serially with the wiring to form a common noise suppression filter. [9] Inductors are also used for decoupling circuits for power supplies.

However, when only inductors are used for the power supply of an IC, although it may suppress the noise properly, impedance relative to the power supply terminal becomes high causing problems for IC operations, or interfering with the signal's return current, making it difficult to maintain signal integrity. Therefore, capacitors and inductors are normally used in combination, placing capacitors in the vicinity of ICs as shown in Figure 2-9 (b) and (c). (Although inductors are placed on the IC side of high-frequency amplifiers in order to block specific frequency, for digital ICs, the combinations in Figure 2-9 are generally used.)

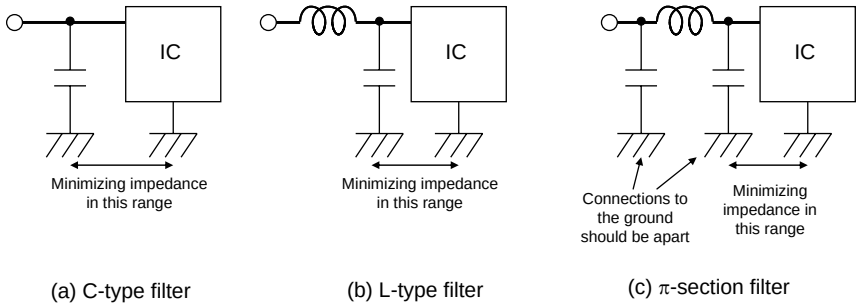


Figure 2-9 Filter configurations used for IC power supplies (C-type, L-type and π-section)

When capacitors and inductors are combined as seen in Figure 2-9 (b) and (c), the slope for the characteristics curve of insertion loss can be made more acute compared with using only a capacitor as in (a). Since the insertion loss in the decay area can be increased simultaneously this way, it is more advantageous when the noise must be greatly attenuated. An example of the change in insertion loss when inductors are combined is shown in Figure 2-10.

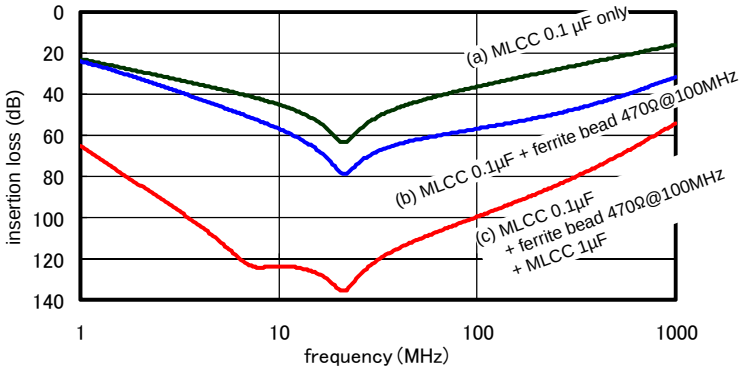


Figure 2-10 An example of insertion loss fluctuation when an inductor is combined (calculated values)

Since, in Figure 2-9, the IC ground and the ground for the closest capacitor become return paths for the noise, they should be made as short as possible to minimize impedance. Also when a π-section filter is formed as shown in Figure 2-9 (c), it is more desirable to use a ground separate to the capacitor (with a via, etc.) so as to prevent noise from bypassing the inductor (when conditions of the grounds are not desirable) going through the ground (the ground plane is shared, however).

The decoupling circuit shown in Figure 2-9 can be applied to noise entering from outside, in addition to noise emitted by the IC. For example, with circuits exposed to strong high frequency energy such as those in mobile phones, a decoupling circuit with capacitor and inductor combination to achieve larger insertion loss is more suitable.

2.6 Capacitance necessary for a capacitor

When an inductor is used for the decoupling circuit as shown in Figure 2-9 (b) and (c), the capacitor's capacitance must be greater than the circuit without an inductor, as shown in Figure 2-9 (a). When multiple ICs are connected to a power supply, each of the decoupling capacitors operate in parallel, effectively expanding capacitance, and impedance relative the power supply terminal is relatively low due to the support given by the power supply module. In contrast, when an inductor is used, capacitors supporting the power supply of the corresponding IC are limited to those inside the inductors.

A method of roughly estimating necessary capacitance, when an inductor is mounted as shown in Figure 2-9 (b), is introduced here as an example. The capacitor's capacitance necessary inside the inductor may be established using the following equation:

$$C \geq \frac{L}{Z_T{}^2} \qquad (2\text{-}2)$$

In this case, C is capacitance (F) of the capacitor that is necessary, L is inductance (H) of the inductor and Z_T is the power supply impedance necessary for IC: target impedance (Ω).

Although there are many approaches to determining Z_T, it can be determined by using instantaneous transient current ΔI (A) and allowable voltage fluctuation ΔV (V) of an IC. [10)]

$$Z_T = \frac{\Delta V}{\Delta I} \qquad (2\text{-}3)$$

Let us estimate the capacitance necessary for the capacitor when using an inductor with L =1μH (approximately 600Ω@100MHz) for the IC's decoupling circuit at ΔI=0.1A and ΔV=200mV using the equation above, for example. First, we can derive Z_T=2Ω from equation (2-3). By introducing this value to equation (2-2) we can obtain $C \geqq$0.25μF. In this case it can be seen that the IC's decoupling capacitor needs at least 0.25μF capacitance.

From equation (2-2), we can see that the higher the inductance is, the greater the necessary capacitance becomes. We can assume that as inductance becomes greater, impedance will become greater than the lower frequency, expanding the frequency range, necessitating the lowering of impedance for the capacitor on the low-frequency side.

Since equation (2-2) only gives a rough estimate, capacitance may be insufficient in some cases when applying this calculation result to an actual circuit. Amply sufficient capacitance should be chosen when applying this value to circuit design.

3. Noise suppression with a capacitor

Ideally, the noise suppression effect when using capacitors and inductors in a decoupling circuit improves as frequency becomes higher. However, in reality, it becomes less effective in the high-frequency region over 10MHz. Although the cause of becoming less effective may be due to the characteristics of the capacitor itself, it may also be due to the way the capacitor is used on the printed circuit. In this chapter, we will describe the causes for fluctuation in frequency characteristics of capacitors used in a decoupling circuit and how it may affect noise suppression effect.

3.1 Frequency characteristics of the capacitor

Multilayer ceramic capacitors (MLCC) are widely used as capacitors offering excellent frequency characteristics. However, they contain small amounts of intrinsic resistance and inductance causing less than ideal characteristics when used under high frequency. A typical equivalent circuit of a capacitor is shown in Figure 3-1. [1)] In Figure 3-1, ESR represents the intrinsic resistance and ESL represents the intrinsic inductance. Because of these elements, capacitor impedance indicates a V-shaped frequency characteristic, as shown in Figure 3-2.

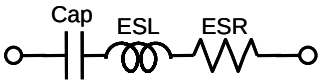


Figure 3-1 Equivalent circuit of the capacitor

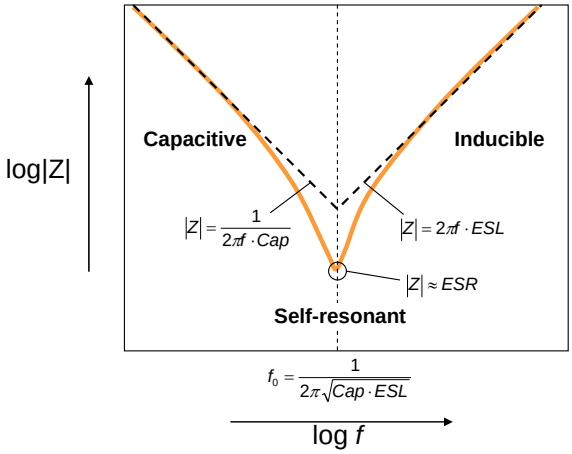


Figure 3-2 Frequency characteristics of the capacitor

The impedance of a capacitor decreases almost linearly, showing characteristics similar to an ideal capacitor on the left side in low frequency range in Figure 3-2 (marked “capacitive”). After reaching the minimum value (marked “self-resonant”), it then increases almost linearly past that point (marked “inducible”). Impedance in the capacitive zone corresponds with ESR while in the inducible zone corresponds with ESL. Therefore, in order to use a capacitor with low impedance in the high frequency range, it becomes

important to choose a capacitor with low ESR and ESL.

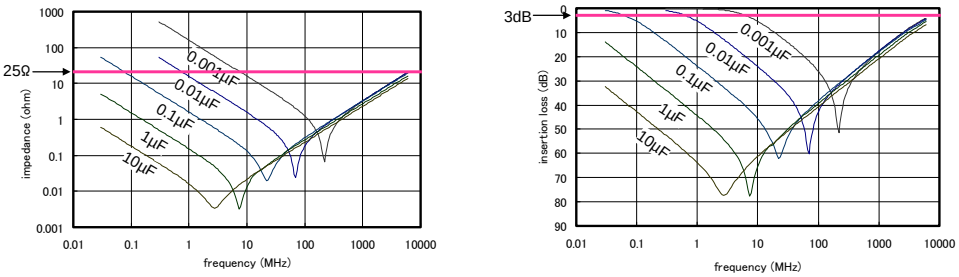
Noise suppression effect of a capacitor being used as a bypass capacitor corresponds with this impedance (The smaller the impedance, the larger the noise suppression effect.). Therefore, its insertion loss characteristic is charted as a V-shaped frequency characteristic similarly to Figure 3-2. An example of comparison between MLCC's impedance and insertion loss is indicated in Figure 3-3.

In this example, characteristic curves are compared using a 2.0x1.25mm-size (GRM21 series) capacitor for both cases while varying its capacitance. The two curves show virtually the same curve, and at the frequency where the capacitor's impedance is almost 25Ω, a cut off (3dB) frequency appears for insertion loss. This is understood to be because in the insertion loss measurement circuit in Figure 2-5, impedance of the bypass capacitor becomes significantly large against impedance of the measurement system (50Ω).

By looking at Figure 3-3, we can tell that the characteristic curves are neatly separated in the capacitive zone, but essentially become one line in the inducible zone. By this we can assume that MLCC's ESL is influenced by a factor other than capacitance.

In order to significantly improve the characteristics in this inducible zone, we need a capacitor with reduced ESL. We will describe such a capacitor in Chapter 4.

MLCC in this manual refers to a regular multilayer ceramic capacitor (without a special structure for reducing ESL).



(a) Impedance (b) Insertion loss

Figure 3-3 An example of frequency characteristics of capacitor
(From Murata Chip S-Parameter & Impedance Library)

3.2 Influence of the capacitor mounting pattern

Insertion loss characteristics for the capacitor we have discussed so far pertain to capacitors mounted on a printed circuit under ideal conditions. These characteristics may vary when mounted on an actual substrate. For example, when considering connecting a capacitor to a ground from a power supply wiring as illustrated in Figure 3-4, mounting pattern and via inductance would be placed linearly to the capacitor. When factoring in the component inductance ($ESL_{(PCB)}$) generated by mounting on a substrate, insertion loss characteristics of the capacitor change, as seen in Figure 3-5 and insertion loss is observed to decrease in the inducible zone (high frequency range).

When a capacitor is used to suppress high frequency noise, it should be designed with thick and short wiring so that this mounting inductance ($ESL_{(PCB)}$) can become small.

$ESL_{(PCB)}$ must be kept small from the viewpoint of the power supply impedance in addition to that of the insertion loss (noise suppression effect). Wiring design to suppress inductance value in the wiring and power supply impedance will be introduced in detail in Chapter 7.

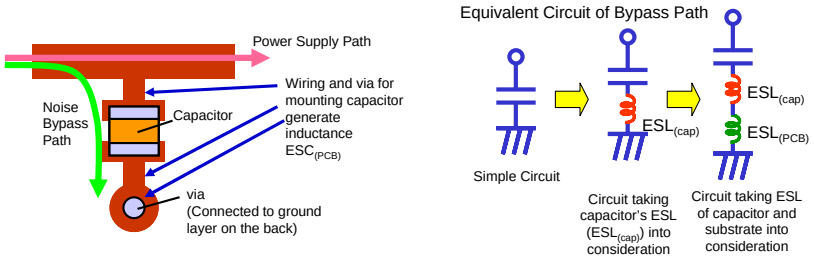


Figure 3-4 Influence of wiring when mounting a capacitor

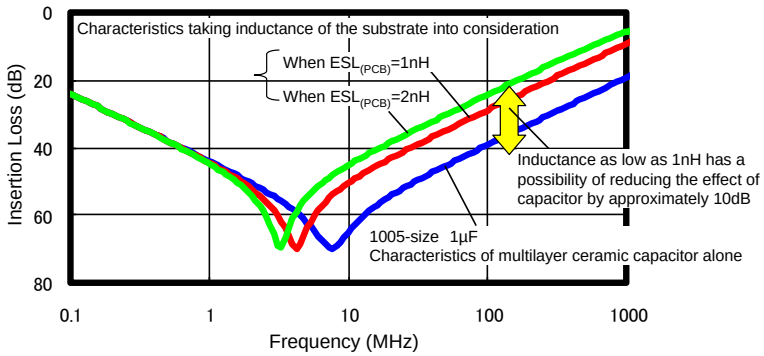


Figure 3-5 Fluctuation in characteristics of conductor due to mounting inductance (calculated values)

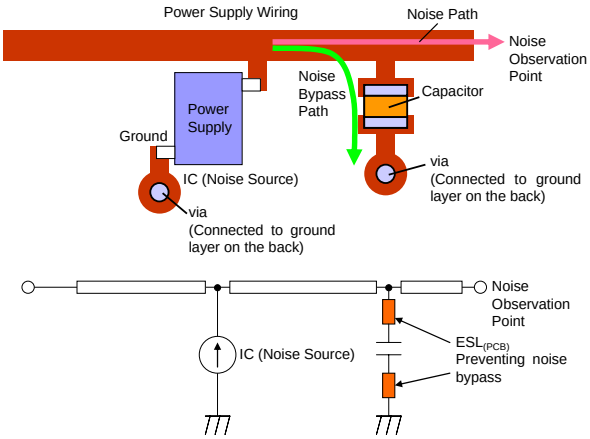
3.3 Noise path and capacitor mounting position

Mounting Inductance ($ESL_{(PCB)}$) when the capacitor is mounted may change according to the noise path and capacitor mounting position. For example, when the capacitor is positioned over the noise path as shown in Figure 3-6 (a), $ESL_{(PCB)}$ comes from the capacitor mounting pattern and via, making it relatively small. On the other hand, if the mounting position is located on the opposite side of the noise path as shown in Figure 3-6 (b), all the wiring from the power supply terminal to the mounting position is included in $ESL_{(PCB)}$ making $ESL_{(PCB)}$ larger. The effect of the capacitor lessens in the high frequency region, in this case. We shall call this kind of wiring away from the noise path “branched wiring”.

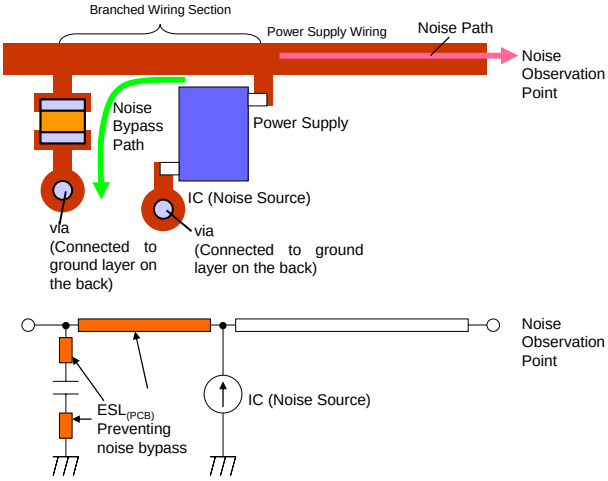
An example of calculating fluctuation in insertion loss assuming this branched wiring being a 10mm-long MSL (Micro Strip Line) is shown in Figure 3-7. In this example, insertion loss decreases close to 20dB in an over-10MHz frequency range.

When the pattern configuration is complex like a power supply circuit, and there are multiple power supply terminals emitting noise, it is necessary to place capacitors so that there is no branched wiring, in consideration of the noise sources and transmission paths

corresponding with the capacitors.



(a) Layout limiting mounting inductance (Top: Layout Bottom: Schematic Diagram)



(b) Layout with large mounting inductance (Top: Layout Bottom: Schematic Diagram)

Figure 3-6 Relation between noise path and capacitor position

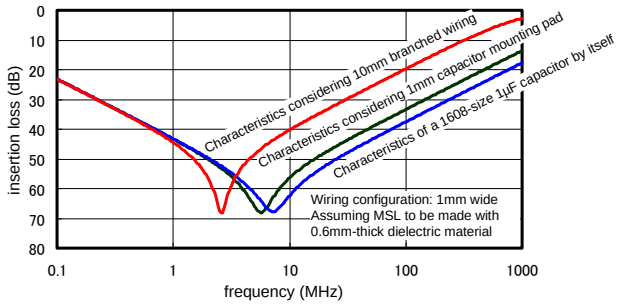
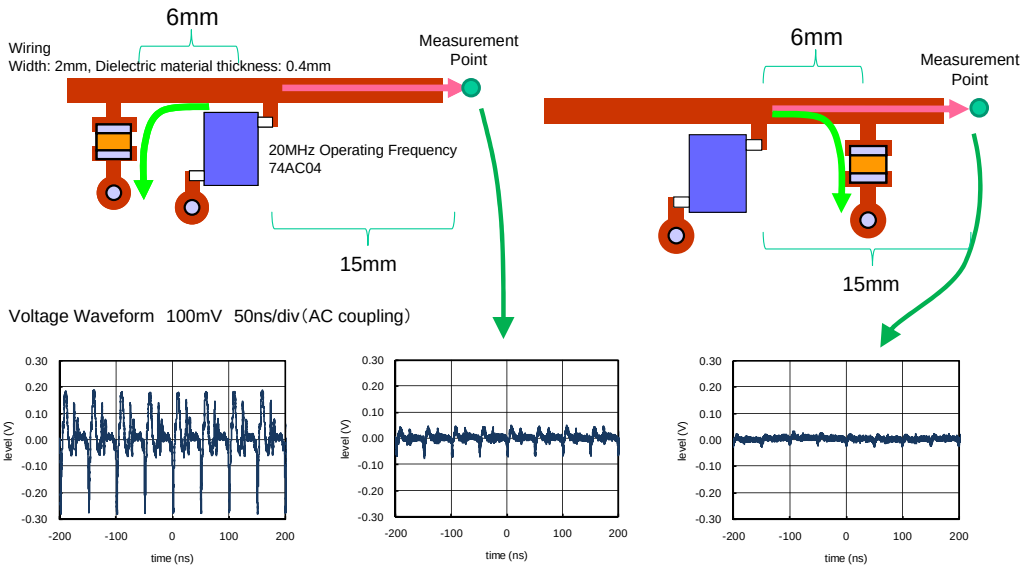


Figure 3-7 An example of fluctuation in insertion loss when branched wiring is present (calculated values)

Figure 3-8 is an example to confirm the influence of branched wiring shown in Figure 3-7 in an experiment. Noise emitted at the power supply terminal of a digital IC operating at 20MHz is suppressed by mounting 1608-size, 1µF MLCC 6 mm away from the power supply terminal. Size of the noise can be confirmed with voltage waveform measured with

an oscilloscope located at 15mm away from the power supply terminal.

Figure 3-8 indicates measurement results when (a) without a capacitor, (b) a capacitor is mounted on the other side of the noise path (with branched wiring), and (c) a capacitor is mounted over the noise path (no branched wiring). Compared with (b), voltage fluctuation (ripple) is less than one third in (c), indicating that existence of branched wiring can greatly affect noise suppression.



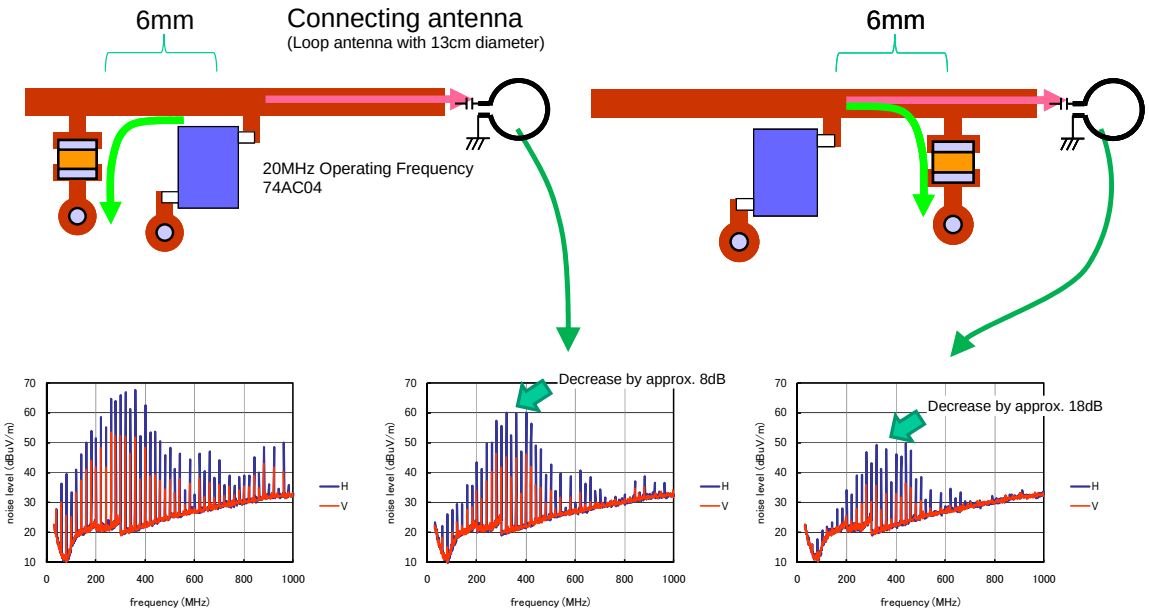
(a) Without a capacitor (b) With branched wiring (c) Without branched wiring

Figure 3-8 Confirming power supply noise suppression effect (voltage waveform)

In Figure 3-9, the same circuit as Figure 3-8 is used to evaluate change in the influence of the power supply with regard to noise emission. A loop antenna emitting noise is mounted at one end of the power supply wiring, and the noise emitted was measured from 3m away. Horizontal polarization is marked with H and vertical polarization is marked with V. As with Figure 3-8, measurement results when (a) without a capacitor, (b) a capacitor is mounted on the other side of the noise path (with branched wiring), and (c) a capacitor is mounted over the noise path (without branched wiring) are indicated.

Results of Figure 3-9 also shows that the noise suppression effect of (c) without branched wiring is better than (b) with branched wiring by approximately 10dB in terms of the frequency showing peak emission. This 10dB difference is understood to represent the influence of inductance at 6mm-branched wiring section.

Furthermore, while with as seen in Figure 3-8, voltage fluctuation is contained within approximately 1/5 when comparing (a) and (b) in spite of the presence of branched wiring, in Figure 3-9, peak emission fluctuates by approximately 8dB (approximately 1/2.5) when comparing (a) and (b). The reason for this may be that the influence for all frequencies is multiplied together for voltage fluctuation, while radiation is measured for each frequency, accentuating the effect of high frequency in this observation. We can see that the influence of $ESL_{(PCB)}$ such as branched wiring becomes more significant when dealing with high-frequency noise.



(a) Without a capacitor (b) With branched wiring (c) Without branched wiring

Figure 3-9 Confirming IC power supply noise suppression effect (noise radiation spectrum)

3.4 Influence of peripheral circuit impedance

Insertion loss characteristics for the capacitor described in Section 3.1 show the value when mounted on a 50Ω system capacitor. Since the actual power supply circuit will be different from this, we need to compensate for the estimation of capacitor effect, taking circuit impedance into consideration. One example in Figure 3-10 shows the result of calculating capacitor characteristic fluctuation, assuming that peripheral circuit impedance will show a certain resistance value.

As shown in Figure 3-10, insertion loss of a capacitor generally tends to be small in a circuit with low impedance. Since power supply circuits are considered to be relatively low-impedance, when designing a filter, we need to figure in the reduction in insertion loss. Also, in order to improve the capacitor's effect in such a low-impedance circuit, the use of an inductor in combination is effective. A decoupling circuit with an inductor added is introduced in Chapter 5.

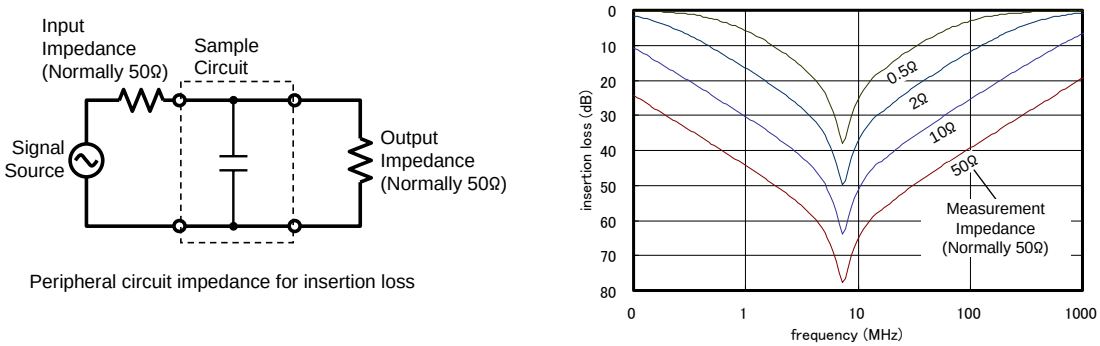
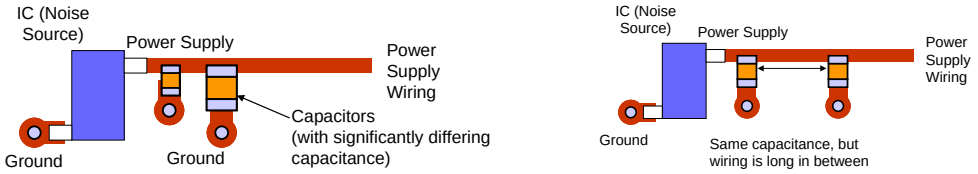


Figure 3-10 Fluctuation in insertion loss in relation with peripheral circuit impedance

3.5 Parallel connection of capacitors and antiresonance

When the capacitance of a capacitor is insufficient, or target impedance and/or insertion loss cannot be achieved due to large ESL and ESR, multiple capacitors may be connected in parallel as seen in Figure 3-11. We must be careful with parallel resonance (called antiresonance) occurring among capacitors in this case, and as shown in Figure 3-12, to make impedance of certain frequencies becoming higher than the case with one capacitor.[11] (In the case of Figure 3-11 (b), wiring between capacitors works as an inductor to increase insertion losses in some frequencies; however, impedance seen from the power supply terminal tends to become large due to antiresonance.)

Antiresonance is a phenomenon where the self-resonant frequency of two capacitors differs, and parallel resonance occurs in the frequency region where one capacitor is in the inducible zone and another capacitor is in the capacitive zone, resulting in increased total impedance (ideally, it becomes infinitely large). Therefore, insertion loss becomes small for the frequencies where antiresonance occurs.



(a) Capacitors having significantly different capacitance (b) Capacitors being far apart

Figure 3-11 Examples of capacitor connections likely to have antiresonance

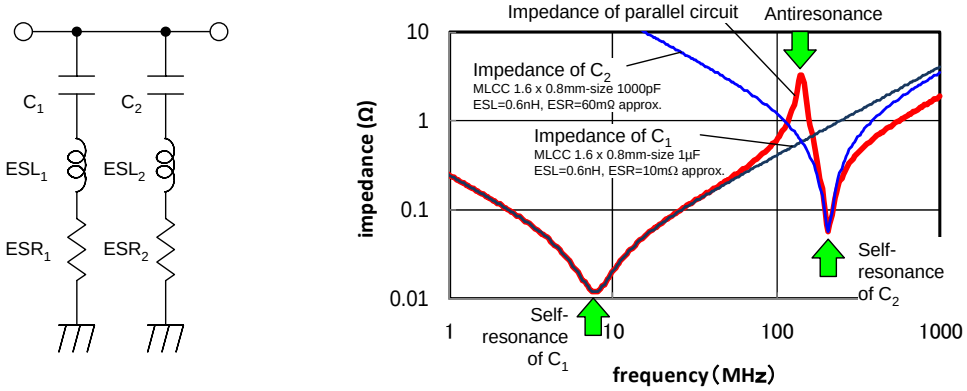


Figure 3-12 Parallel resonance of the capacitor (calculated values)

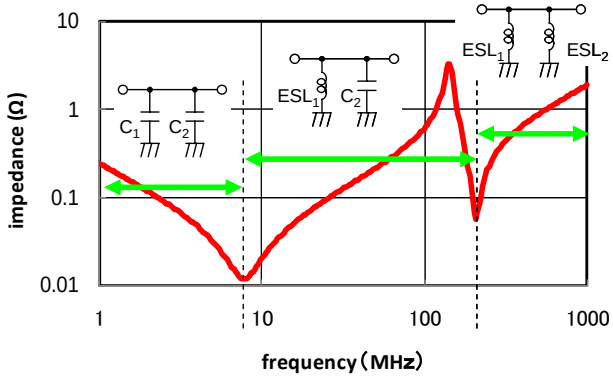


Figure 3-13 Mechanism of the capacitor's parallel resonance

The following methods, shown in Figure 3-14, would prevent antiresonance by:

(1) inserting resonance suppression components such as ferrite beads between capacitors,

(2) matching capacitance of capacitors to align self-resonant frequencies, and

(3) containing the capacitance difference less than 10:1 when combining capacitors with different capacitance.

Method (1) is quite effective for improving insertion loss. However, the effect of lowering impedance is smaller, as explained in Section 2.6. While complete suppression of antiresonance is difficult for methods (2) and (3), in practicality, the problem is somewhat lessened. As shown in Figure 3-14 (d), if the target capacitance is reached with one high-performance capacitor with low ESL and ESR, it would be ideal since it can eliminate the problem of antiresonance. This high-performance capacitor will be introduced in Chapter 4.

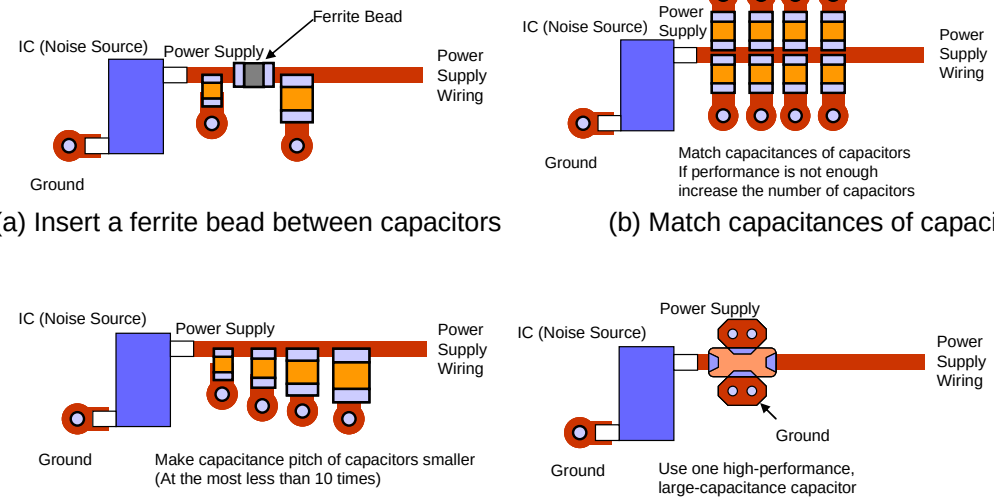


Figure 3-14 Examples of positioning capacitors to suppress antiresonance

Figures 3-15 through 3-17 are examples to confirm the influence of antiresonance in experiments. The noise observed at the power supply terminal of a digital IC operating at 4MHz is measured with an oscilloscope and a spectrum analyzer. Measurement is taken on the left and right of the decoupling circuit (left: input side of the noise; right: output side of the noise).

In this diagram, measurement results of the oscilloscope are located in the center and measurement results of the spectrum analyzer are located on the outside. Both are measured using an FET probe. (Spectrum is measured by resolving frequency of the terminal voltage, as opposed to measuring emissions.)

In Figure 3-15, antiresonance occurring from a combination of two MLCCs is observed. The first row is the case with only one MLCC, and antiresonance does not occur. The occurrence of antiresonance is deliberately induced by creating extreme conditions by applying conditions in Figure 3-11 for the second and third rows. MLCCs at 1µF and 1000pF are connected through wiring. As indicated by the arrows, noise spectrum increased for some frequencies, and strong ringing is observed in the third row even over the power supply voltage.

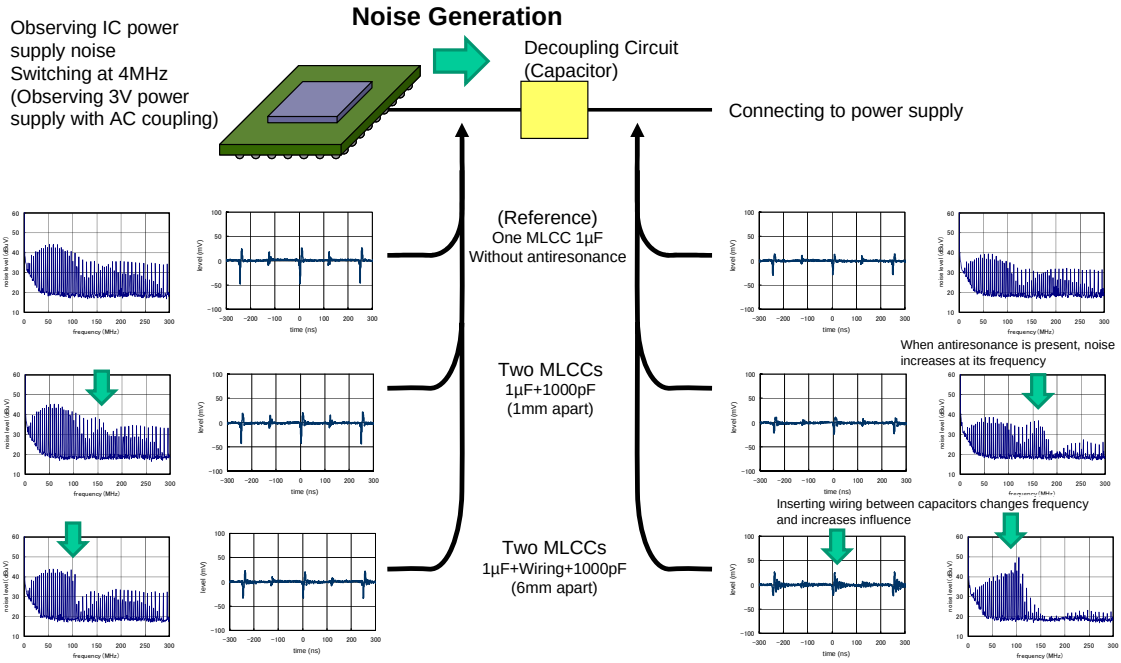


Figure 3-15 Examples of noise observation when antiresonance is present

In contrast, Figure 3-16 indicates results of the experiment suppressing antiresonance. The first row shows the case with one MLCC as with Figure 3-15. Conditions from Figure 3-14 (b) were applied for the case on the second row to match the capacitance of capacitors (with two capacitors). Conditions from Figure 3-14 (c) are applied to the third row to make the capacitance pitch smaller (with four capacitors). In these cases, as the number of capacitors increases, power supply voltage fluctuation becomes smaller and noise spectrum decreases as well.

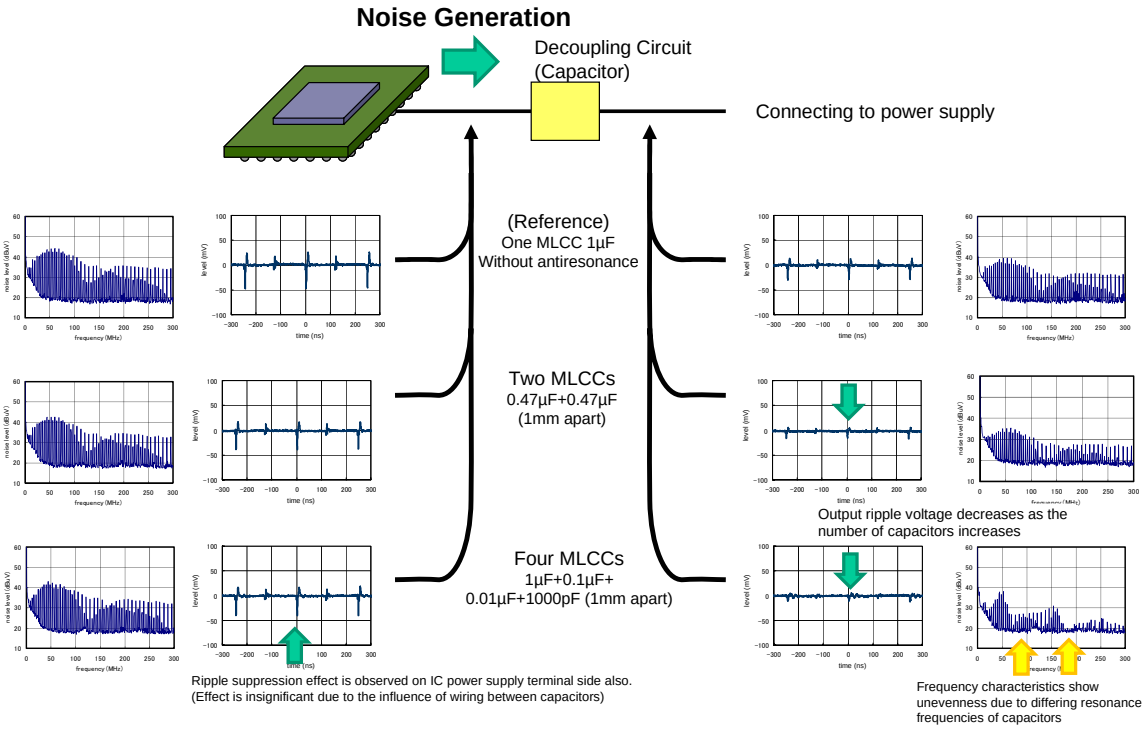


Figure 3-16 Measurement results for combinations with little antiresonance

Figure 3-17 shows the results of the experiment where a low ESL capacitor and a 3-terminal capacitor are used as an example of Figure 3-14 (d). The first row in the diagram indicates one MLCC as with the earlier example for the sake of comparison.

The second row indicates a case with a low-ESL capacitor. Fluctuations in power supply voltage become small on the left and right of the decoupling circuit, and the spectrum becomes smaller because of it also. A low-ESL capacitor is considered to be an especially effective component for suppressing fluctuation in power supply voltage.

The third row indicates a case with a 3-terminal capacitor. We can see that the voltage fluctuation and spectrum on the right is especially small. This should indicate excellent noise suppression characteristics of a 3-terminal capacitor.

These high-performance capacitors are introduced in detail in Chapter 4.

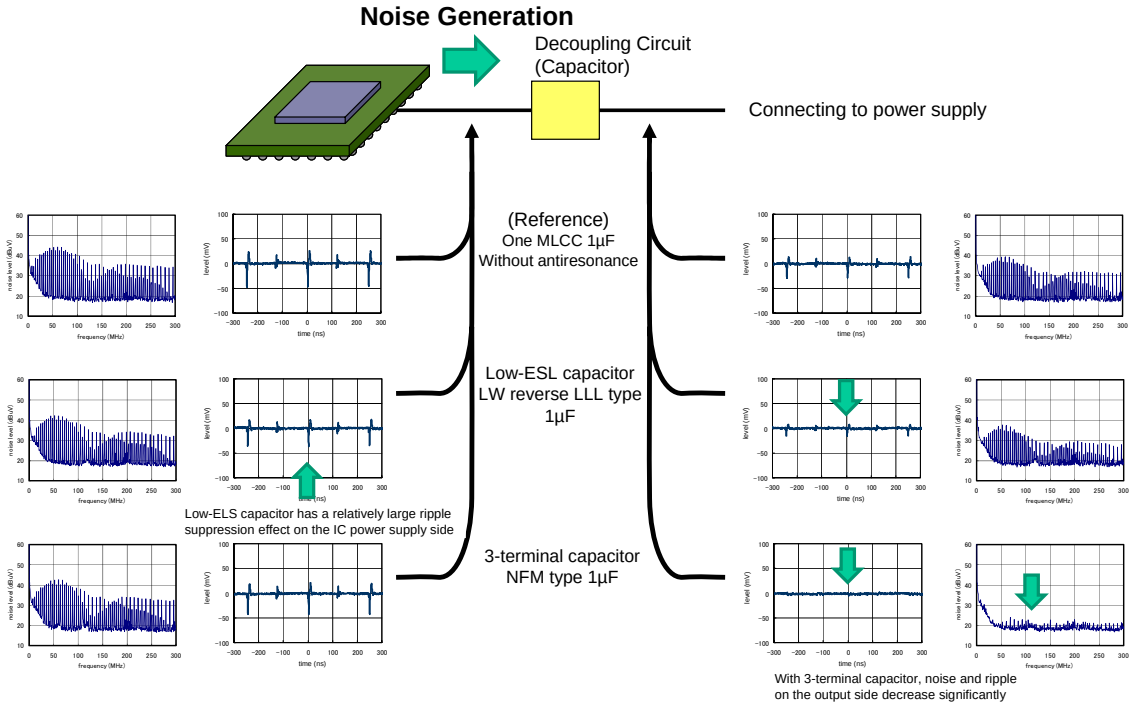


Figure 3-17 Measurement results when using low-ESL capacitors

4. Capacitor with improved high-frequency characteristics

In Chapter 3, we described general frequency characteristics when using a capacitor for a decoupling circuit of IC power supply. In this chapter, we will introduce capacitors with improved high-frequency characteristics by reducing ESL.

4.1 Low-ESL capacitor

The ESL of an MLCC is understood to be generated by magnetic flux that occurs when current flows through external and internal electrodes as shown in Figure 4-1. Therefore, we may alter ESL by changing current path and distribution as a result of the change in electrode configuration.

An example of a capacitor with ESL reduced through innovation of electrode configuration is shown in Figure 4-2.

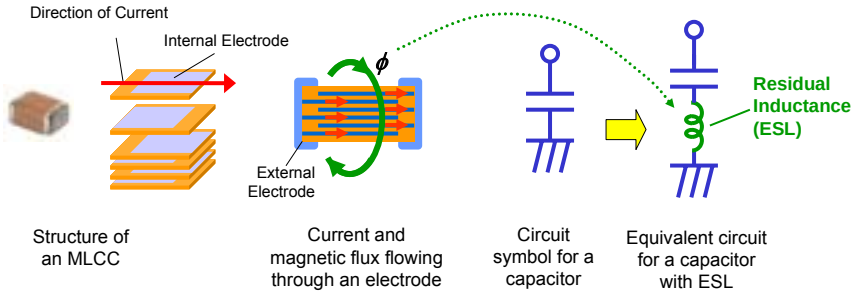


Figure 4-1 Mechanism of ESL generation in an MLCC

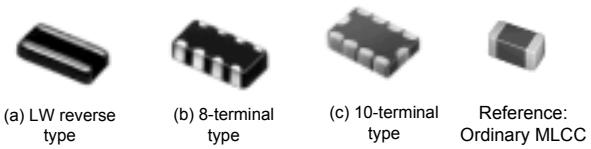


Figure 4-2 Configurations of low-ESL capacitors

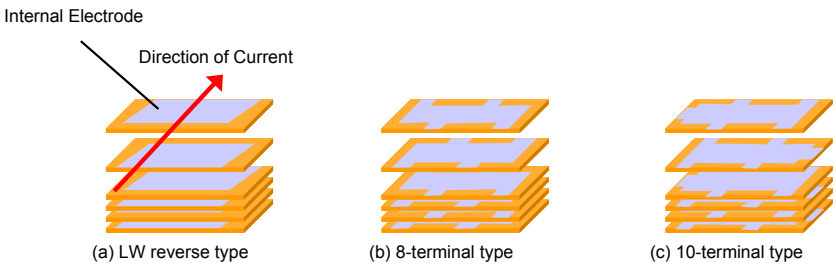


Figure 4-3 Structure of low-ESL capacitor (schematic view)

Figure 4-2 (a) indicates a capacitor with reduced inductance due to its wide and short electrode, called length width reverse capacitor or LW reverse capacitor. As shown in the internal structure diagram in Figure 4-3 (a), the internal electrode is wider and shorter compared with common MLCCs.

In Figure 4-2 (b) and (c), multi-terminal capacitors with an increased number of external

electrodes, where neighboring electrodes have reversed polarities, are indicated. As shown in the internal structure diagrams in Figure 4-3 (b) and (c), internal electrodes are formed thick and short, and additionally internal electrode drawers are formed so that they can be connected to external electrode alternately. (Their external appearances seem similar to capacitor arrays, but these components' internal electrode configuration is totally different.)

By choosing such a structure, mutual inductance occurs between currents where they flow in opposite directions, cancelling each other's inductance as shown in Figure 4-4. For the components where currents flow between neighboring electrodes, the current loop tends to be extremely small as opposed to the currents flowing in opposing directions. Furthermore, these inductances are connected in parallel, realizing extremely small ESL as a total of the components.

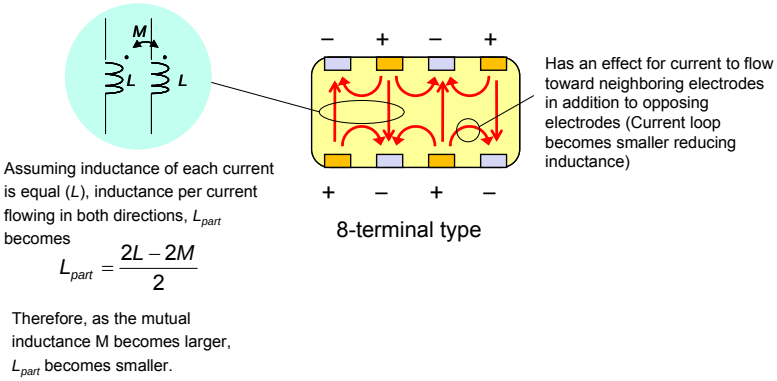


Figure 4-4 Inductance cancellation effect from mutual inductance

Figure 4-5 indicates an example of comparing impedances of a conventional MLCC and low-ESL capacitors. All capacitors are 1.6x0.8mm size and 1µF. Impedance decreased to approximately 1/5 for the LW reverse capacitor and approximately 1/2 of the LW reverse capacitor for the multi-terminal capacitor in the frequency range over 100MHz. Compared with the conventional MLCC, the ESL of a multi-terminal capacitor should be less than 1/10.

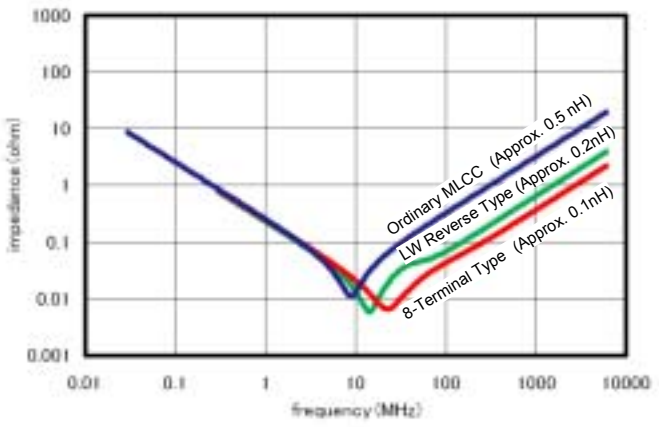


Figure 4-5 An example of impedance characteristics for a low-ESL capacitor
(From Murata Chip S-Parameter & Impedance Library)

Characteristics shown in Figure 4-5 are those of conversion from S parameter to impedance, where a capacitor is mounted in on the bypass side of a micro strip line (MSL) for measurement. Therefore, they represent characteristics specific to the component (and can be approximated with a lumped constant).

Generally, when mounting a capacitor on a printed circuit, influence by inductances (ESL_{PCB}) of pattern connected to the capacitor and via, in addition to capacitor's ESL, is significant. As shown in the diagram, when a multi-terminal capacitor is mounted on a substrate, the inductance cancellation effect between currents flowing in opposite directions next to each other influences currents in the pattern and via as in Figure 4-6, making the influence of ESL_{PCB} relatively small. Therefore, compared with using MLCCs with conventional pattern and via, use with patterns and via dedicated for multi-terminal capacitors would yield a higher impedance improvement effect surpassing the performance difference indicated in Figure 4-5.

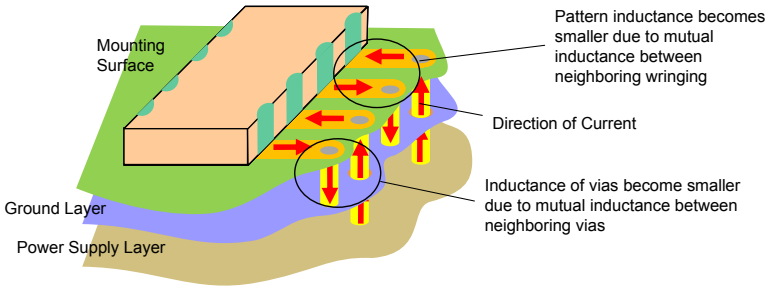


Figure 4-6 Inductance suppression effect when mounting a multi-terminal capacitor

4.2 Low-ESL capacitor lineup

An overview of the low-ESL capacitors currently commercialized is shown below. Please refer to the catalog, etc. for the latest information.

● LW reverse capacitor LLL series

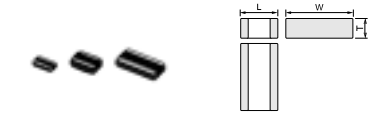
Capacitance range

0.5 x 1.0mm size : 0.1－0.22μF

0.8 x 1.6mm size : 0.0022－2.2μF

1.25 x 2.0mm size : 0.01－2.2μF

1.6 x 3.2mm size : 0.01－10μF



Part Number	Dimensions (mm)		
	L	W	T
LLL153	0.5 ±0.05	1.0 ±0.05	0.3 ±0.05
LLL185	0.8 ±0.1	1.6 ±0.1	0.6 max.
LLL215	1.25 ±0.1	2.0 ±0.1	0.5 +0/-0.15
LLL216			0.6 ±0.1
LLL219			0.85 ±0.1
LLL315	1.6 ±0.15	3.2 ±0.15	0.5 +0/-0.15
LLL317			0.7 ±0.1
LLL31M			1.15 ±0.1

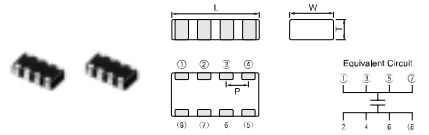
● 8-terminal-type capacitor LLA series

Capacitance range

1.6 x 0.8 mm size : 0.1－2.2μF

2.0 x 1.25 mm size : 0.01－4.7μF

3.2 x 1.6 mm size : 0.1－2.2μF



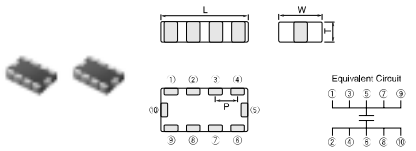
Part Number	Dimensions (mm)			
	L	W	T	P
LLA185	1.6 ±0.1	0.8 ±0.1	0.5 +0.05/-0.1	0.4 ±0.1
LLA215	2.0 ±0.1	1.25 ±0.1	0.5 +0.05/-0.1	0.5 ±0.05
LLA219	2.0 ±0.1	1.25 ±0.1	0.85 ±0.1	0.5 ±0.05
LLA315	3.2 ±0.15	1.6 ±0.15	0.5 +0.05/-0.1	0.8 ±0.1
LLA319	3.2 ±0.15	1.6 ±0.15	0.85 ±0.1	0.8 ±0.1
LLA31M	3.2 ±0.15	1.6 ±0.15	1.15 ±0.1	0.8 ±0.1

● 10-terminal-type capacitor LLM series

Capacitance range

2.0 x 1.25 mm size : 0.01－2.2μF

3.2 x 1.6 mm size : 0.1－2.2μF



Part Number	Dimensions (mm)			
	L	W	T	P
LLM215	2.0 ±0.1	1.25 ±0.1	0.5 +0.05/-0.1	0.5 ±0.05
LLM315	3.2 ±0.15	1.6 ±0.15	0.5 +0.05/-0.1	0.8 ±0.1

4.3 3-terminal capacitor

Another method of reducing ESL is the use of 3-terminal capacitors. An example of a 3-terminal capacitor is shown in Figure 4-7. This is a type of feed-through capacitor which is an MLCC with excellent frequency characteristics, having circuit connection designed to reduce ESL.

As shown in Figure 4-8, a 3-terminal capacitor is structured with input/output terminals to draw in the noise path inside the component. Consequently, inductance generating at an internal electrode branches out three ways to form a T-shaped circuit. When connecting input/output terminals of a 3-terminal capacitor to the noise path, ESL in the input/output directions enters the noise path serially, increasing insertion loss (improving the noise suppression effect). Also, ESL in the bypass direction is only at the ground area, making it about one-half of an MLCC. The 3-terminal capacitor indicated in Figure 4-7 further reduces inductance in the ground area by designing it with two ground electrodes on the left and right sides of the capacitor.

These innovations contain the ESL of a 3-terminal capacitor in the bypass direction at about 10 to 20pH, which is less than 1/30 for conventional MLCCs for some models. Therefore, we can expect a good bypass effect under high frequency over 1GHz.

Insertion losses for an MLCC and a 3-terminal capacitor are compared in Figure 4-9. They are both 1.6x0.8mm size at 1µF, but 3-terminal capacitor shows approximately 35dB larger insertion loss in the frequency range over 100MHz.

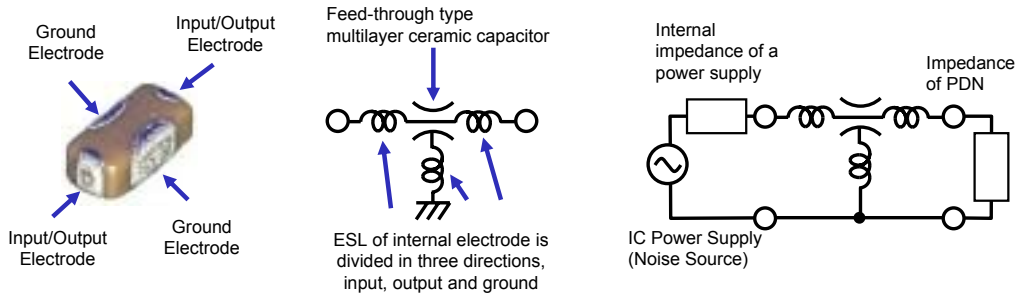


Figure 4-7 An example of a 3-terminal capacitor for power supplies

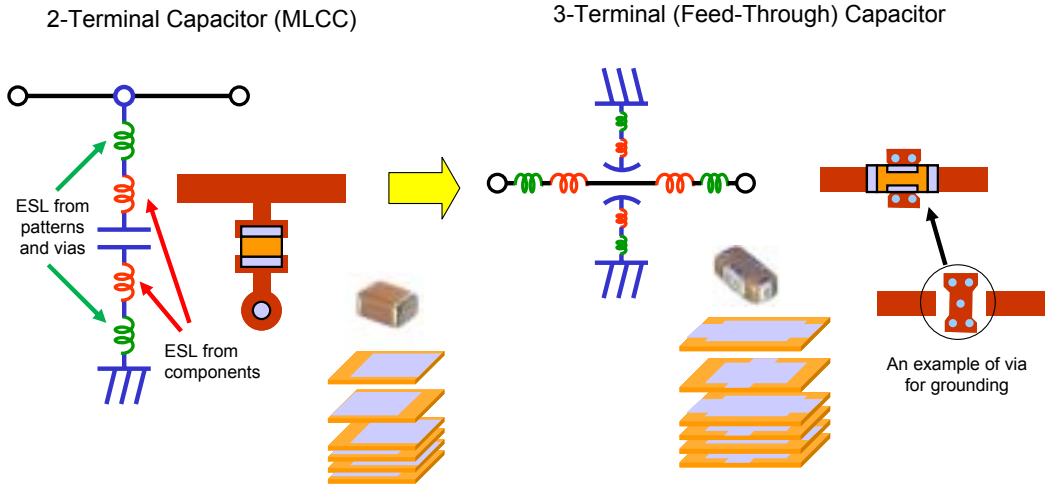


Figure 4-8 Mechanism of ESL reduction using a 3-terminal capacitor

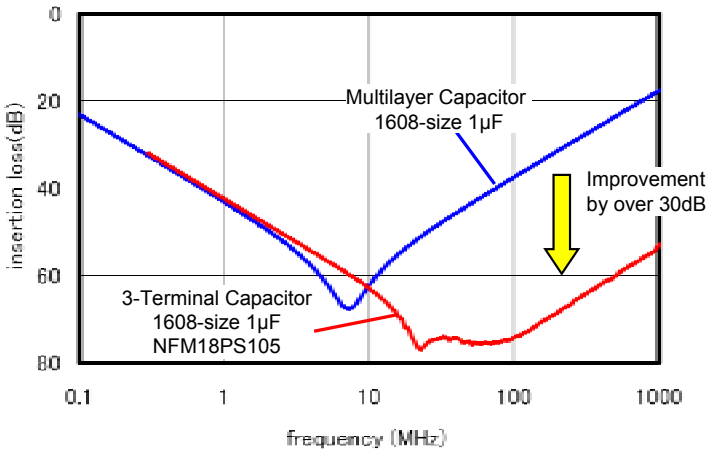
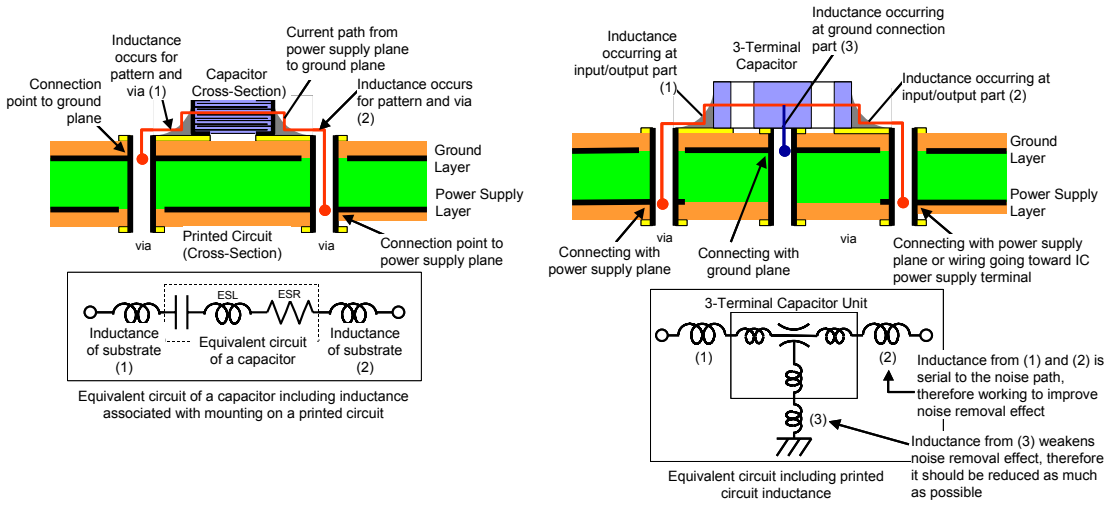


Figure 4-9 Insertion loss characteristics of a 3-terminal capacitor

In addition to the effect described above, 3-terminal capacitors are characterized by increasing insertion loss by forming a T-type filter without interfering with current flowing in the bypass direction since its inductance (ESL_{PCB}) from the circuit pattern and via are located serially with the noise path where the input/output terminals are mounted, as shown in Figure 4-10. Although its ESL_{PCB} at the area where the ground terminal is mounted enters the bypass direction, this can be minimized with multilayer substrates by connecting with the ground plane with multiple vias with this area directly beneath the component.[2)]

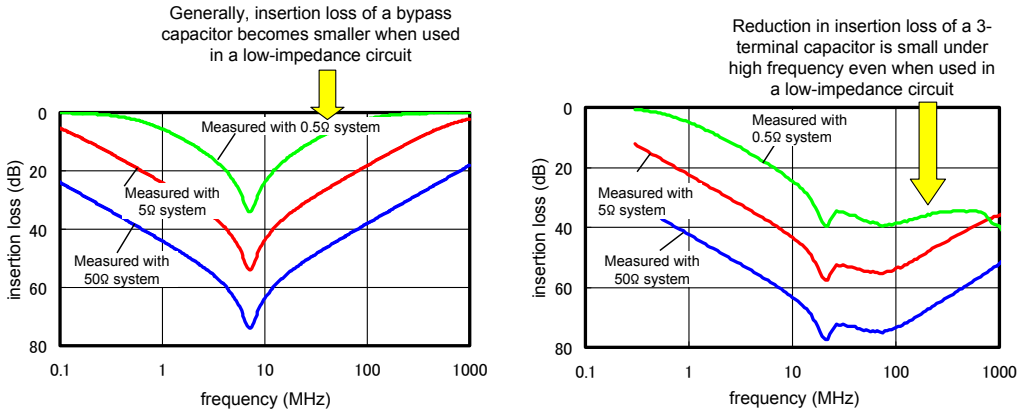


For MLCC　　For 3-terminal capacitor

Figure 4-10 Equivalent circuit of a capacitor including inductance from the substrate

For these reasons, 3-terminal capacitors can achieve larger insertion loss compared with MLCCs even when they are mounted on a printed circuit. Also, reduction of insertion loss when mounted on a low-impedance circuit is smaller than MLCCs (due to ESL_{PCB} located serially with the noise path).

In Figure 4-11, fluctuation of insertion loss is compared for varying measurement impedance by taking 1µF capacitors as an example. We assume capacitors are used in a power supply circuit which tends to be low in impedance, and the impedance of the measurement system is varied from 50Ω to 5Ω and 0.5Ω. Insertion loss of 3-terminal capacitors maintains over 30dB at 1GHz for a low-impedance circuit. This suggests that an inherently large insertion loss of a 3-terminal capacitor, and ESL arranged in T-shaped as shown in Figure 4-8 is effective in the high-frequency range around 1GHz.



(a) For MLCC (b) For 3-terminal capacitor

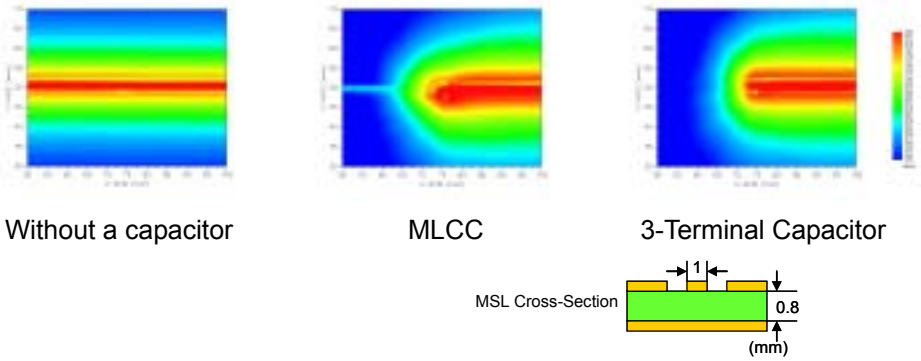
Figure 4-11 Change in characteristics when measurement impedance is varied (calculated values) (assuming impedance of the measurement system to be 50Ω, 5Ω and 0.5Ω)

In Figure 4-12, an example for confirming fluctuation of the capacitor's noise suppression effect with varied measurement impedance is indicated through an experiment. Bypass capacitor operation is observed, in this case, by taking a measurement of near magnetic field distribution around the capacitor. It visually illustrates the way noise is being bypassed to the ground with the capacitor, since this near magnetic field is understood to correspond with the current.

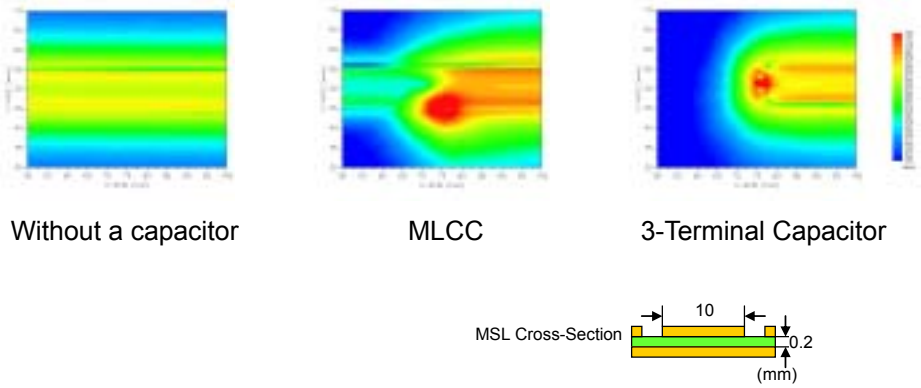
Characteristic impedances of the wiring used in this experiment are (a) approx. 60Ω and (b) approx. 3Ω. Both ends of the wiring are terminated in order to eliminate the effect of the reflected wave. The measurement frequency was 100MHz, while the range of measurement was 40mmx30mm with the capacitor mounted in the center. The diagram shows that the noise is entering from the right side, and the capacitor's noise suppression effect is observed from the intensity of the current leaving from the left side. Intensity of the current is marked in colors, indicating stronger current as it changes from blue to red.

We could confirm from results of the experiment shown in Figure 4-12 that MLCC controls the noise relatively well for (a) 60Ω, but its filtrating effect tends to decrease for (b) 3Ω (current flows through to the left). Meanwhile, the 3-terminal capacitor controlled the noise well for both (a) and (b). We also found that 3-terminal capacitors have a tendency for smaller noise diffusion toward the ground compared with MLCCs. This is assumed to be because the 3-terminal capacitor is connected to the ground with vias directly under the component.

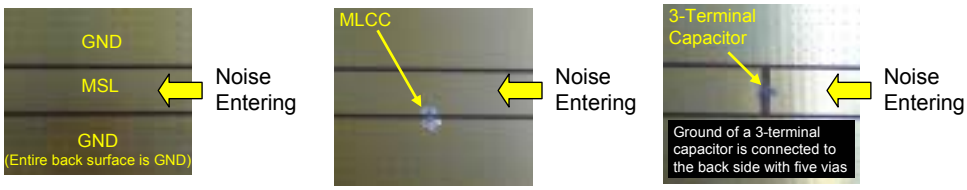
Since, wide wiring with low characteristic impedance tends to be used for power supply circuits as in this experiment, a 3-terminal capacitor should be the better choice for noise suppression.



(a) When characteristic impedance is approx. 60Ω



(b) When characteristic impedance is approx. 3Ω



(C) Reference: Mounted state of a capacitor (wiring thickness is for (b) 3Ω)

Figure 4-12 Change in current distribution around the capacitor when measurement impedance is varied

4.4 3-terminal capacitors lineup for power supplies

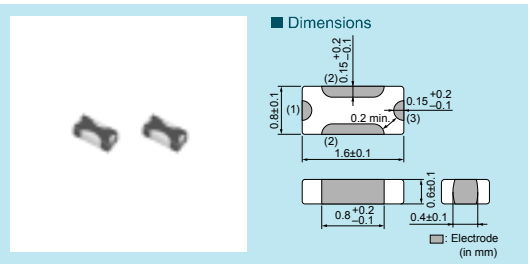
The lineup of 3-terminal capacitors suitable for IC power supplies is listed below. Please refer to the catalog, etc. for the latest information.

● 1608 size

High attenuation type NFM18PS series

Capacitance range

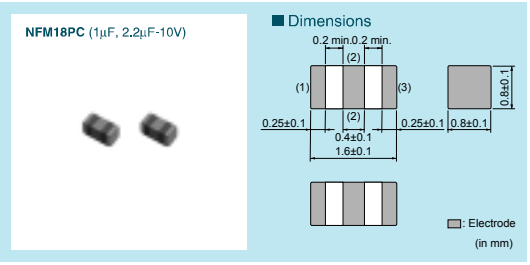
0.47-1.0μF



High capacitance type up to 2.2μF NFM18PC series

Capacitance range

0.1-4.7μF

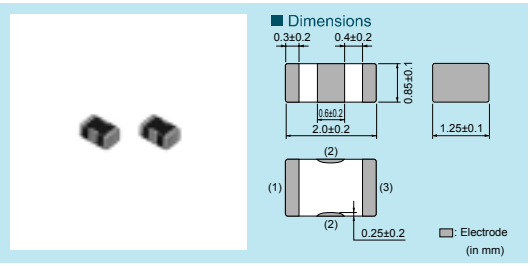


● 2012 size

High capacitance type up to 10μF NFM21PC/PS series

Capacitance range

0.1-10μF

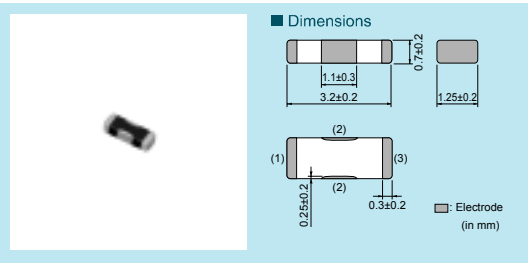


● 3212 size

Rated at 50V NFM3DPC series

Capacitance range

0.022μF



5. Inductors and LC filters

When a decoupling capacitor is not sufficient to suppress power supply noise, the combined use of inductors and LC filters is effective. In this chapter, we will introduce inductors and LC filters suitable for controlling power supply noise.

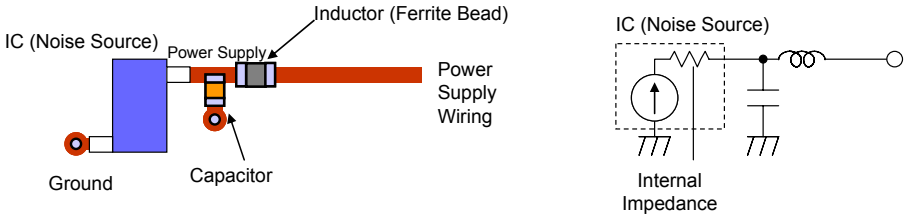
Choke coils and ferrite beads are the common inductors used for power supply decoupling circuits. While ferrite beads are used to control a wide range of frequencies that are relatively high frequency, choke coils tend to be used to control specific frequencies. Although ferrite beads are used more for the noise measures described by this manual, choke coils are also for noise control; therefore they are both introduced in this chapter. We will also introduce an LC filter for power supplies with a combination of inductors and capacitors.

5.1 Decoupling circuit using an inductor

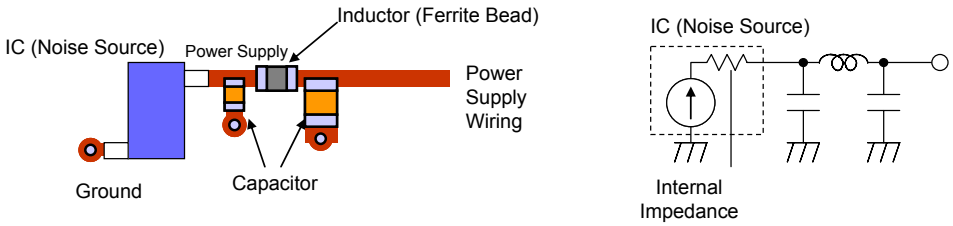
A general configuration when forming a decoupling circuit with an inductor added to the power supply is shown in Figure 5-1. Figure 5-1 (a) shows a decoupling capacitor with an inductor added, and (b) shows a higher performance π-section filter by adding a capacitor to (a). Since many capacitors are used with other ICs in power supply wiring, even (a) could practically become a π-section filter, while the configuration in (b) could suppress noise with more certainty.

Generally, inductors with larger impedance (and consequently with larger inductance) would show excellent noise suppression effect (however, there are some considerations mentioned in Section 5.6).

On the other hand, when an inductor is used as in Figure 5-1, momentary current necessary for the IC operation will be supplied by the capacitor between the inductor and the IC. The capacitance necessary for this capacitor becomes larger corresponding with the inductance as shown in equation 2-2. Therefore, it is not recommended to use excessively large inductance.



(a) When forming a L-type filter



(b) When forming a π-section filter

Figure 5-1 Construction of a power supply filter in combination with an inductor

5.2 Frequency characteristics of inductors

In Section 5.1, we showed an example of using an inductor with a capacitor. In this section, we describe characteristics when an inductor is used alone, in order to aid in understanding its characteristics. Inductors are inserted serially with a noise path as shown in Figure 5-2. The inductor's insertion loss characteristics are that of a low-pass filter as with a bypass capacitor. This is due to the inductor's impedance increasing proportionally to the frequency, and the larger the impedance is, the larger the insertion loss becomes.

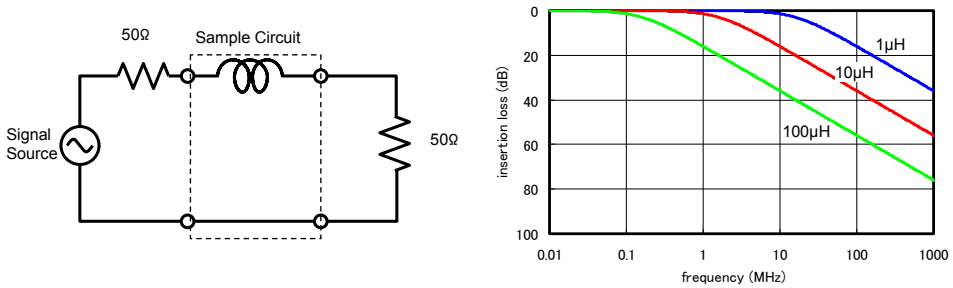


Figure 5-2 Frequency characteristics of the insertion loss measurement circuit and ideal inductor

Actual inductors, much like capacitors, show frequency characteristics. A simplified equivalent circuit of an inductor and the shape of impedance frequency characteristics are shown in Figure 5-3.

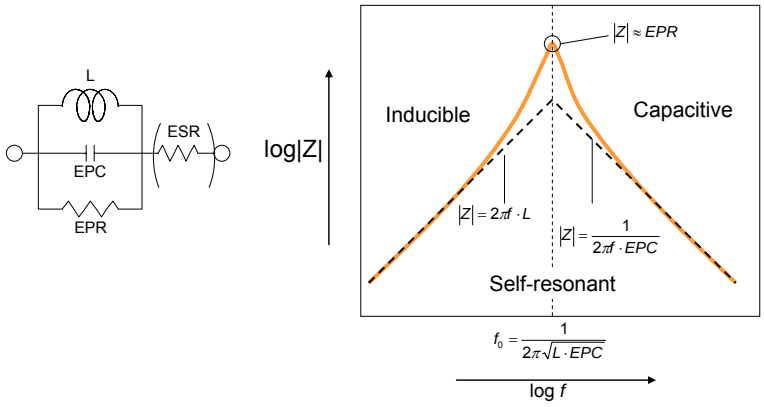


Figure 5-3 Equivalent circuit of an inductor and its frequency characteristics

As seen in the equivalent circuit illustrated in Figure 5-3, equivalent parallel capacitance (EPC) and equivalent parallel resistance (EPR) appear in parallel with the inductor coil (L). Therefore, the impedance of the inductor shows inducibility at a relatively low frequency, and increases almost linearly. However, it reaches the maximum at a certain frequency (self-resonant frequency f_0) and shows capacitivity and decreases almost linearly after that.

Impedance for a self-resonant frequency is constrained by EPR, and impedance in the capacitive region is constrained by EPC. Therefore, in order to realize large impedance

under high frequency, it becomes important to choose an inductor with small EPC. Capacitance generated at the winding wire shows in this EPC. Also, the resistance of the winding wire can be considered with ESR (equivalent serial resistance) aside from these.

An example of comparing impedance and insertion loss as inductance of an inductor is varied is shown in Figure 5-4. When the measurement is taken with a 50Ω system, at the frequency where the inductor impedance becomes approximately 100Ω, a cut off (3dB) frequency appears for the insertion loss. As with the capacitor, it corresponds with the frequency where inductor impedance becomes a significant size compared with the impedance of the measurement system.

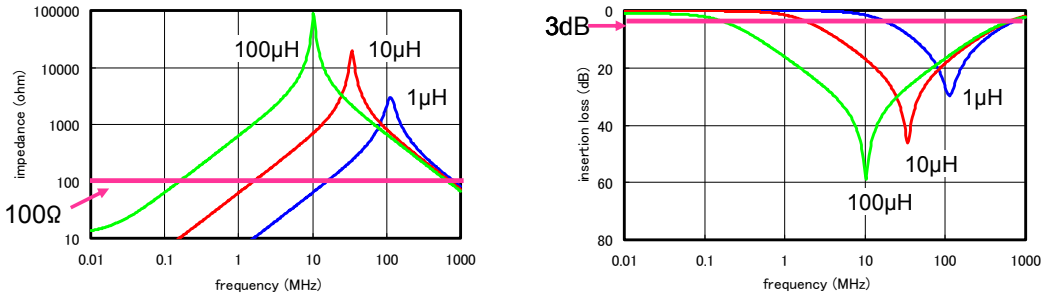


Figure 5-4 Comparison of impedances and insertion losses of inductors
(For LQH3C series)

These insertion loss characteristics change, as seen in Figure 5-5, as the impedance of the measurement system varies. As opposed to the capacitor described in Section 3.4, with an inductor, insertion loss of an inductor increases as the impedance of the measurement system decreases. Therefore, when we try to suppress noise for a low-impedance circuit, an inductor is a more suitable component in general. (However, when used for a power supply, a low-impedance power supply must be available; therefore an inductor is not used alone, but used in combination with a capacitor as shown in Figure 5-1.)

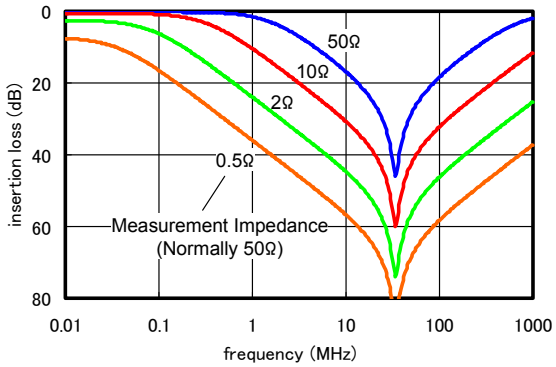


Figure 5-5 Fluctuation in insertion loss in relation with measurement system impedance
(Calculated values, sample circuit LQH3C 10μH)

5.3 Frequency characteristics of ferrite beads

When a ferrite bead is used as an inductor, its characteristics differ slightly from what is described in Section 5.2.

5.3.1 Basic structure of a ferrite bead

As shown in Figure 5-6, the basic structure of a ferrite bead consists of a cylindrical (bead-shaped) ferrite with a lead going through it. (Although recently there have been ferrite beads with multilayer ferrite with a spiral formed inside, as seen in the right bottom diagram of Figure 5-6, the basic structure is as described above.) Since magnetic flux is formed inside ferrite in response to the current going through the lead, it is possible to gain inductance and impedance relative to the magnetic permeability of ferrite. [12)]

This inductance fluctuates depending on the frequency characteristics of ferrite's magnetic permeability, and generally is not fixed. Also, impedance generated is strongly influenced by the magnetic loss of the ferrite. Therefore, characteristics of ferrite beads are usually expressed in terms of frequency characteristics of impedance, as opposed to inductance.

An equivalent circuit of a ferrite bead is shown in Figure 5-7, and an example of impedance frequency characteristics is shown in Figure 5-8.

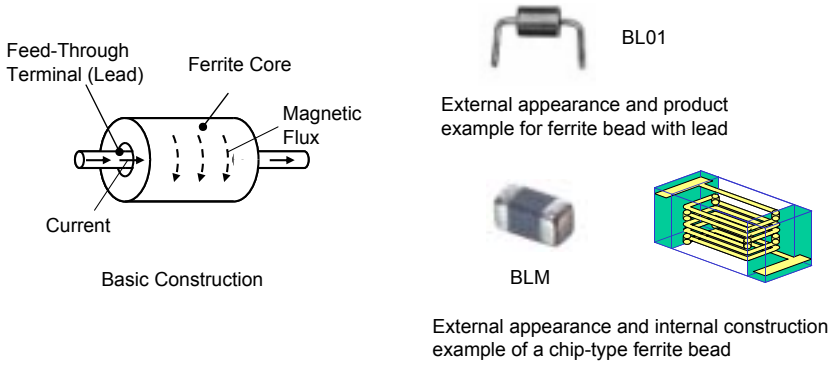


Figure 5-6 Ferrite bead construction

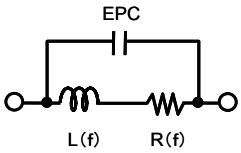


Figure 5-7 Equivalent circuit for a ferrite bead

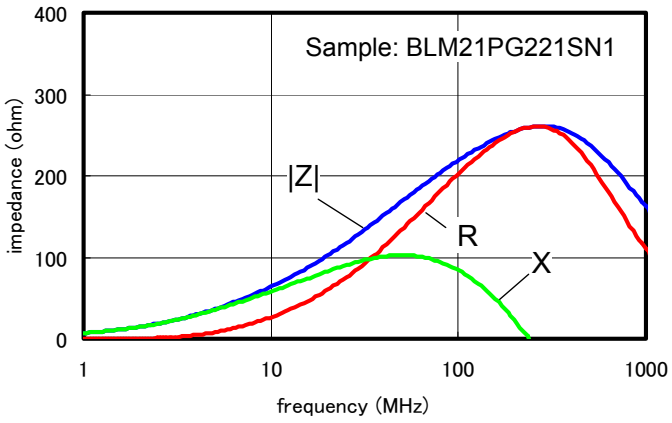


Figure 5-8 Frequency characteristics for ferrite bead impedance

5.3.2 Frequency characteristics of ferrite beads

In Figure 5-8, |Z|, R and X indicate absolute value of impedance, component resistance, and component reactance respectively. For relatively low frequency under 10MHz, impedance mainly indicates reactance, but for frequencies over 10MHz, the component resistance increases. For the frequencies where the component resistance is the majority, ferrite beads show their propensity to absorb noise by converting it to heat. This resistance component does not generate with the direct current, and would not affect power supply (no energy loss occurs for direct current), therefore, is a suitable component for noise suppression of power supplies.

Also, the impedance in Figure 5-8 shows a peak at a frequency around 300MHz; the curve is milder than the inductor shown in Figure 5-4. This indicates that while ferrite beads reduce impedance at high frequency due to EPC as with inductors, the Q value of resonance becomes smaller due to the component resistance.

On the other hand, the slope of insertion loss characteristic for ferrite beads tends to be smaller than pure inductors. Figure 5-9 shows insertion loss characteristics of a ferrite bead shown in Figure 5-8. For a pure inductor, insertion loss characteristics have a slope at -20dB/dec. shown as the dotted line, while that of a ferrite bead would show a milder slope.

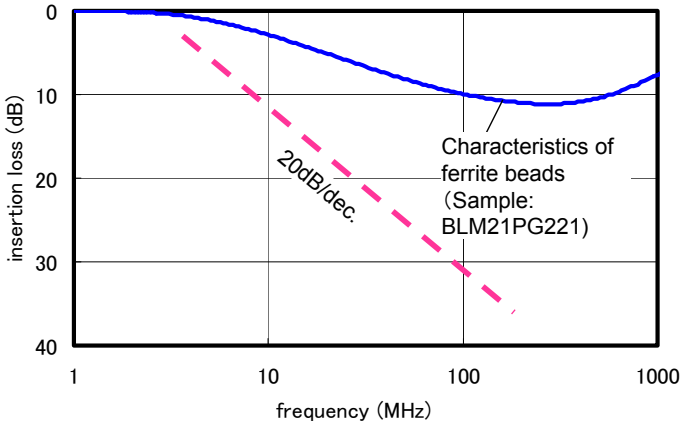


Figure 5-9 An example of insertion loss characteristics for a ferrite bead

5.3.3 Improving high frequency characteristics of ferrite beads

As shown in Figure 5-7, ferrite beads also have stray capacitance EPC, becoming the main cause for a decrease in impedance at high frequencies above 100MHz. Products with improved high-frequency impedance by making this EPC smaller have been commercialized, and used for high frequency noise measurement for frequencies above several hundred MHz. Figure 5-10 shows an example of impedance characteristics for a component with reduced EPC.

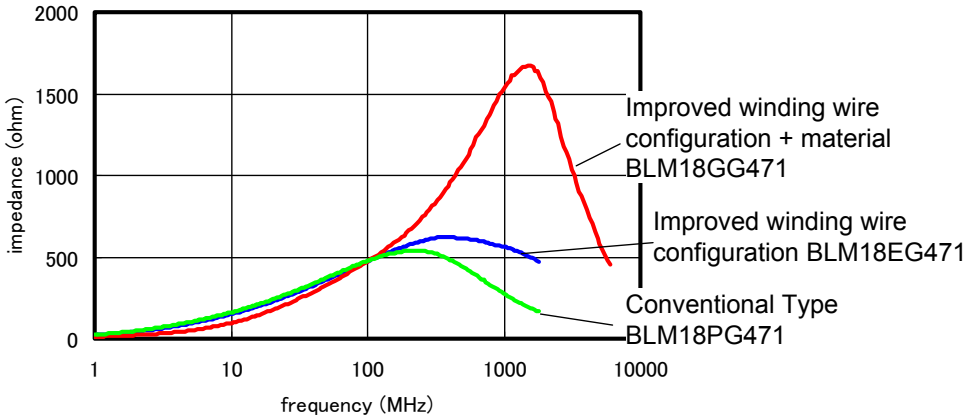


Figure 5-10 Impedance characteristics of ferrite beads with improved high frequency characteristics by reducing EPC

5.4 Characteristics for a combination of capacitors and inductors

When inductors are used for power supplies, often capacitors are used in combination. Therefore, we will introduce characteristics of LC filters where capacitors and inductors are used in combination.

Ideal forms of an LC filter's insertion loss characteristics are shown in Figure 5-11. When the measurement system impedance is fixed and the ratio between L and C are established appropriately, we can get frequency characteristics with 20dB/dec. slope per element. [9)]

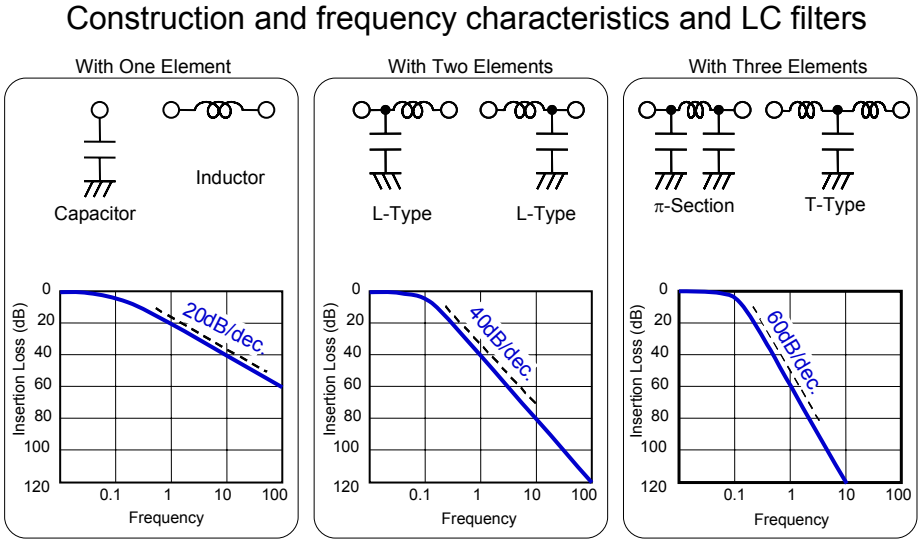


Figure 5-11 Insertion loss characteristics of LC filters

Generally, impedance is not constant for power supply circuits, so that it is difficult to match the ratio between L and C for all frequencies. Also, a capacitor is always placed between an inductor and an IC as described in Section 5-1; the filter becomes L type or π-section. Therefore, examples of the cases where the ratio between L and C is off from the measurement system impedance are shown in Figure 5-12.

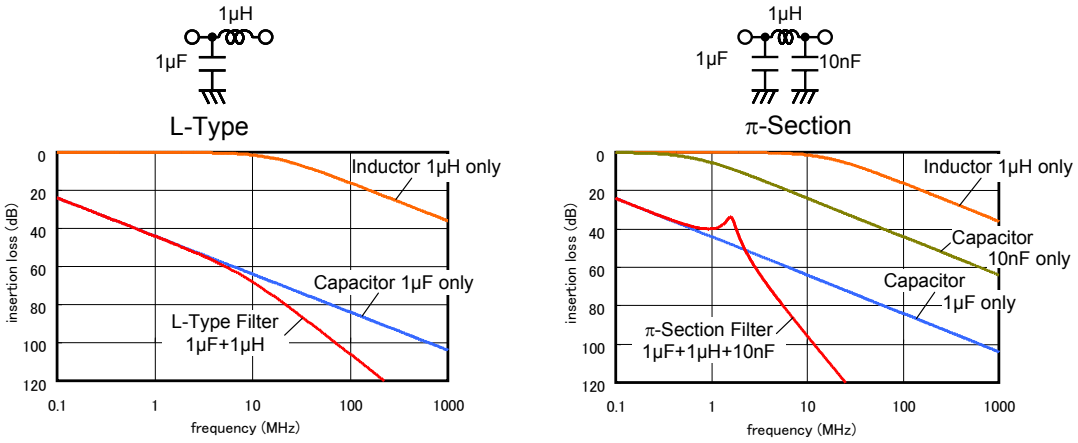


Figure 5-12 Examples of insertion loss characteristics of L-type and π-section filters (calculated values)

In addition, characteristics of a capacitor and an inductor comprising an LC filter are also indicated in Figure 5-12. When the ratio of L and C does not match like this, the slope of the curve representing the attenuation region is not constant, having a point of inflection. Meanwhile, as we have described previously, capacitors and inductors do not operate ideally under high frequency. Therefore, in order to predict actual frequency characteristics, this influence must be taken into consideration as well.

Results of calculating insertion loss, when an L-type filter is formed in combination of an MLCC and a ferrite bead, are shown in Figure 5-13. As shown in this graph, the frequency characteristics of an actual LC filter differ from Figure 5-11. As an overall tendency, total insertion loss can be made larger by combining a ferrite bead.

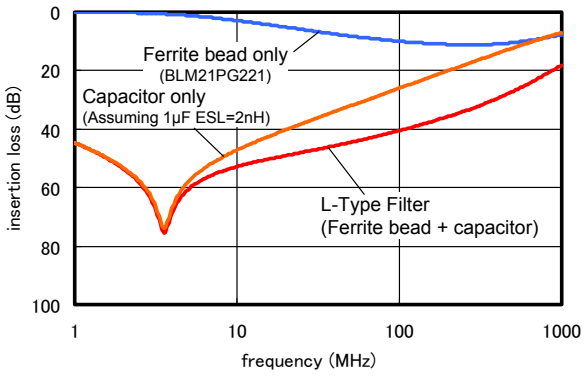


Figure 5-13 Characteristics of L-type filter using a ferrite bead (calculated values)

Figure 5-14 shows an example of confirming the fluctuation in noise control effect when combining a capacitor and a ferrite bead through an experiment. In this example, the source of the noise is an IC operating at 4MHz, and the noise passing through the decoupling circuit is observed with voltage fluctuation and spectrum. The first row shows a measurement without a ferrite bead (using a 1μF decoupling capacitor), the second row is a measurement of an L-type filter by adding a ferrite bead to the first row, and the third row

is a measurement of a π-section filter by adding a 10μF capacitor to the second row. In the second and third row examples, where a ferrite bead is used, it is confirmed that both voltage fluctuation and spectrum are greatly improved.

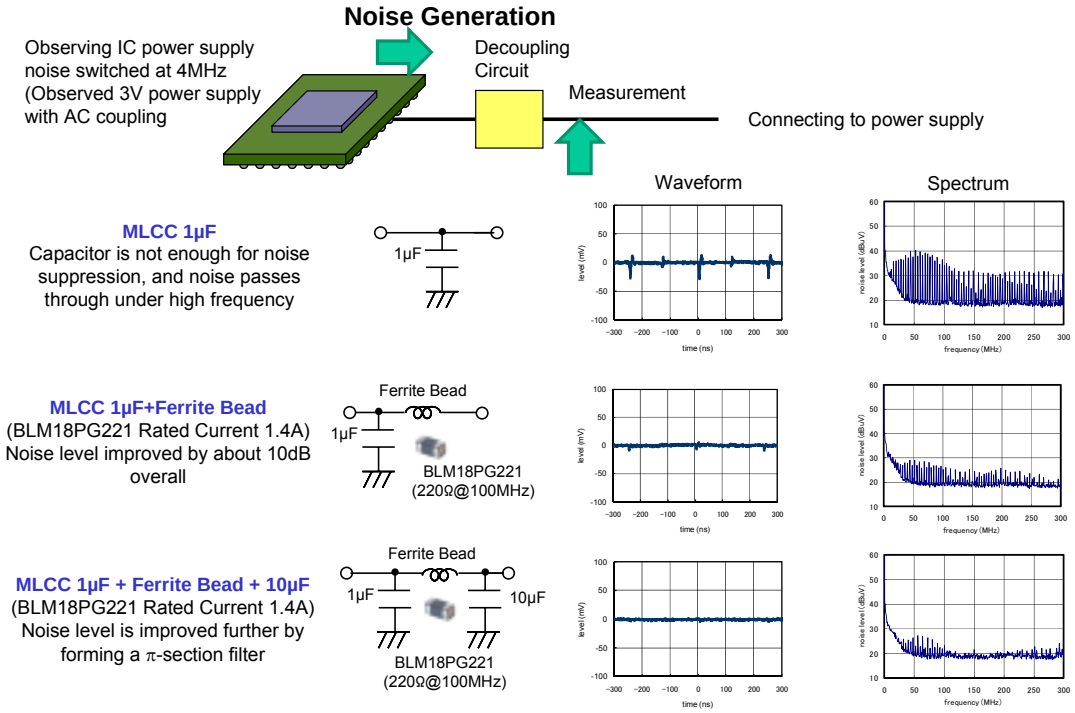


Figure 5-14 An example of noise suppression and improvement by ferrite beads

5.5 LC filter

As described in Chapter 2, the insertion loss of a capacitor tends to become smaller for frequencies above 10MHz. In order to make an improvement, overall insertion loss is made larger by combining a capacitor with small capacitance and taking advantage of self-resonance. However, in this case, antiresonance occurs between two capacitors, diminishing the improvement effect. In order to avoid such a problem, it is effective to use an LC filter where a ferrite bead is used in combination in place of a capacitor with small capacitance. [11)]

Figure 5-15 shows an example of this LC filter, and Figure 5-16 shows calculation results of frequency characteristics when combining this filter with a large-capacitance capacitor.

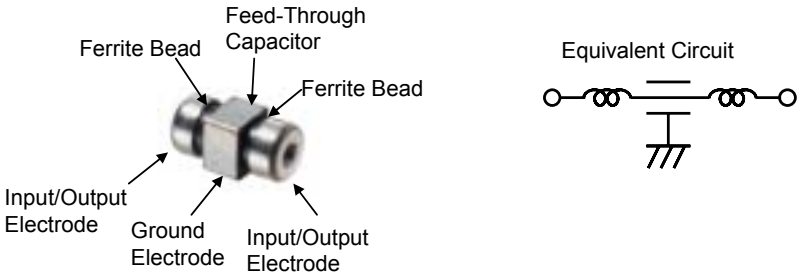
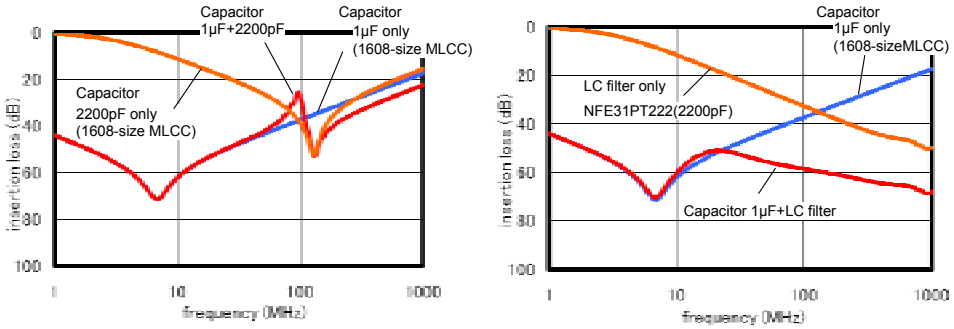


Figure 5-15 LC filter NFE31 for power supplies



(a) When combining two capacitors (b) When combining a capacitor and a LC filter

Figure 5-16 Frequency characteristics of a power supply filter (calculated values)

Figure 5-15 shows a component with a combination between a feed-through capacitor and a ferrite bead with excellent high-frequency characteristics assuming its use with a large capacitance capacitor. Input and output electrodes on both ends are connected with a metal molded terminal, making the serial resistance extremely small while realizing 6A rated current.

As with the calculation results shown in figure 5-16 (a), when two capacitors are simply combined, their insertion loss may be smaller than one capacitor at the frequency where antiresonance occurs. Figure 5-16 (b) shows that when using an LC filter combined with a ferrite bead in place of a small-capacitance capacitor, this kind of problem can be prevented, making it possible to form a filter circuit effective at high frequency near 1GHz. We can assume that using an LC filter has the effect of suppressing antiresonance with the component resistance of the built-in ferrite bead.

Figure 5-17 is an example of confirming fluctuation in the noise suppression effect when combining an LC filter with a capacitor through an experiment. As with Figure 5-14, an IC operating at 4MHz is used as the noise source, and the noise passing through the decoupling circuit is observed with voltage fluctuation and spectrum. (The spectrum analyzer is with higher sensitivity to allow for observation of more minute noise.)

The first row shows a case where a 1µF MLCC is combined with a 2200pF capacitor (a 6mm wiring is inserted in the middle to generate strong antiresonance). In this case, antiresonance between capacitors cause a strong ringing for the power supply voltage, and a strong spectrum is observed at this frequency.

The second row shows a case where an LC filter with 2200pF capacitance replaces the 2200pF MLCC in the same location, and a 10µF MLCC is added to the second row for the third row. In either case, significant improvement is made for both voltage fluctuation and spectrum. Spectrum, especially, is kept at an extremely low level, confirming the fact that an LC filter with a feed-through capacitor has an excellent suppression effect for high frequency noise.

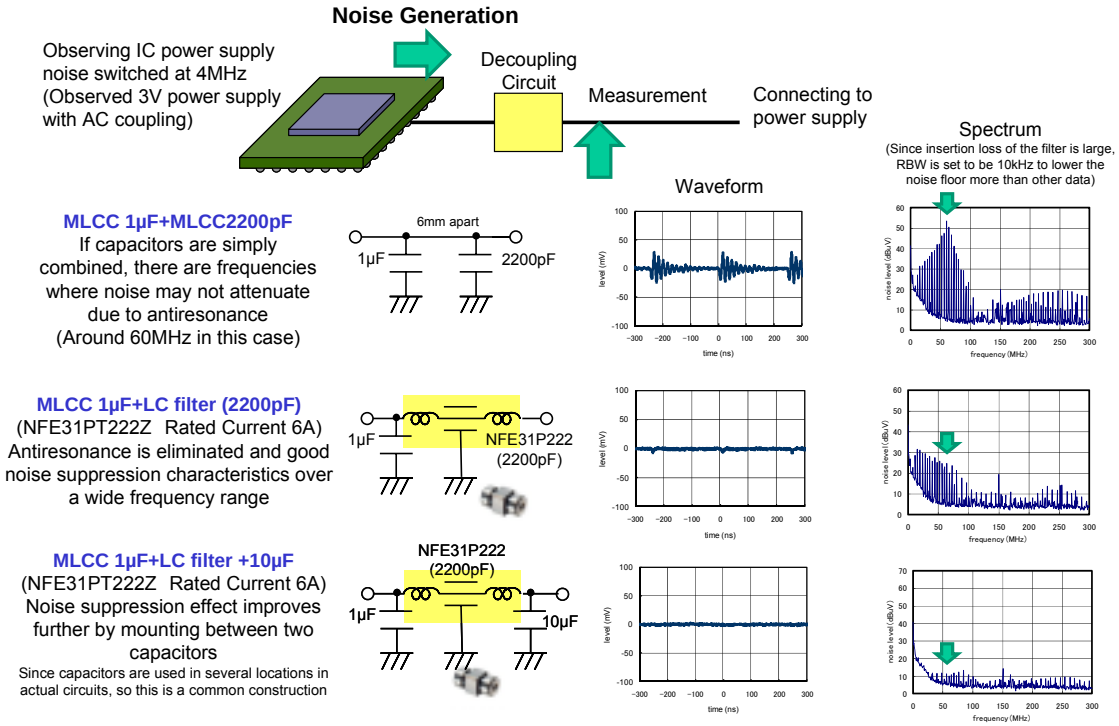
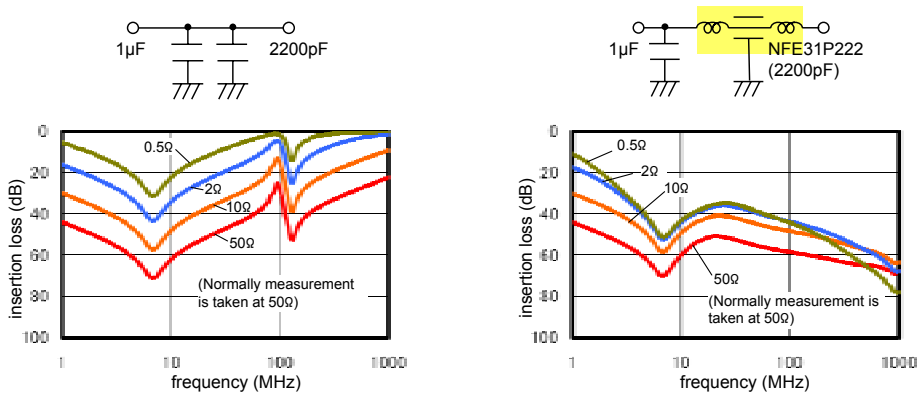


Figure 5-17 An example of improving noise suppression using an LC filter

On the other hand, the insertion loss characteristics described in Figure 5-16, etc. are for the case where the measurement impedance is 50Ω, and impedance of power supplies are often smaller than that. Therefore, we will show the result of fluctuation in characteristics as the measurement impedance is varied in Figure 5-18. This is converted from the calculation results in Figure 5-16.

While with simply combining two capacitors as in Figure 5-18 (a), insertion loss tends to decrease greatly in low-impedance circuit, there is a tendency for a certain level of effect to be maintained even for a low-impedance circuit in Figure 5-17 (b) with an LC filter combined. This is considered to be the case because while the capacitor's effect decreases in the low-impedance circuit, the effect of the inductor increases, therefore two effects are cancelled together when combined with an LC filter. Therefore, the decoupling circuit for power supplies combined with an inductor is expected to show a noise suppression effect relatively stable against fluctuation in power supply impedance.



(a) When combining two capacitors (b) When combining a capacitor and an LC filter

Figure 5-18 Characteristics when measurement impedance is varied (calculated values)

5.6 Considerations when using an inductor for a power supply

Although the noise suppression effect of an inductor basically increases as impedance increases (inductance increases), as we have described thus far, impedance stops increasing under high frequency due to the influence of EPC. Also for the sake of noise suppression or suppression of resonance, generally, the larger the component resistance in impedance, the better the effect will become. We need to select a component for noise suppression from this kind of viewpoint.

On the other hand, from the viewpoint of providing low-impedance power supplies, since the use of an inductor works to increase impedance, we will need to compensate with a capacitor having enough capacitance between the inductor and the IC (guidelines for determining the necessary capacitance is indicated in equation 2-2). Therefore, it is not recommended to use an inductor with unnecessarily large impedance.

When using an inductor for a power supply, we need to select a component considering saturation due to direct current resistance and current in addition.

5.6.1 Influence of direct current resistance

Since direct current resistance of an inductor can generally cause energy loss and heat generation, it is desirable for it to be small when using an inductor for a power supply. Aside from this, voltage fluctuation due to voltage drop can be problematic.

Since direct current resistance can decrease voltage for circuits where constant current flows through, power supply voltage must be maintained high to compensate for that. When there is large current fluctuation, voltage ripple may occur as the following:

$$\Delta V_{ripple} = R_{dc} \cdot \Delta I_{ripple} \qquad (5\text{-}1)$$

Here, ΔV_{ripple}, R_{dc} and ΔI_{ripple} represent voltage ripple, direct current resistance of a component, and current fluctuation respectively. For example, when current fluctuation of 1A is applied to a component with about 100mΩ R_{dc}, 100mV voltage ripple occurs. Therefore, for a low-voltage power supply with small allowable voltage ripple, we need to choose a component with small direct current resistance.

5.6.2 Influence of current saturation

In general, when magnetic flux density of a ferromagnetic material, such as ferrites, reaches saturation, their magnetic permeability tends to become smaller. Therefore, we need to focus on the fact that when large current flows, inductance and impedance decrease for inductors with magnetic cores. In order to confirm this influence, we need to observe the noise level while current is large.

5.7 Lineup of inductors suitable for power supplies

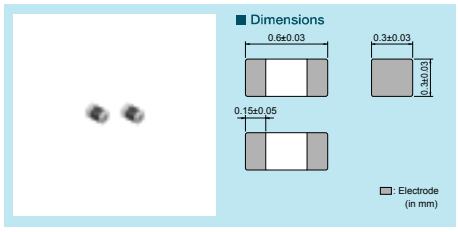
Main examples of ferrite beads and choke coils commercialized at Murata are listed below.

Please refer to our catalog for their details.

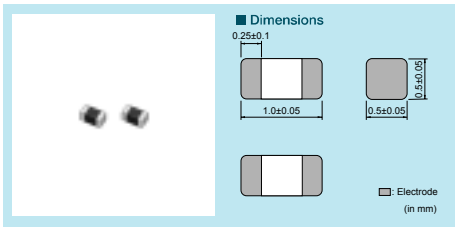
5.7.1 Ferrite beads

Models to keep direct current resistance down are in the lineup for ferrite beads for power supplies.

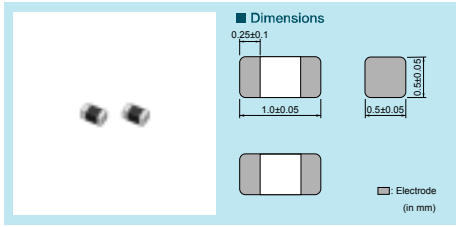
●0603 size BLM03P series



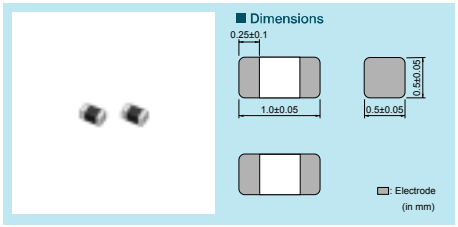
●1005 size BLM15P series



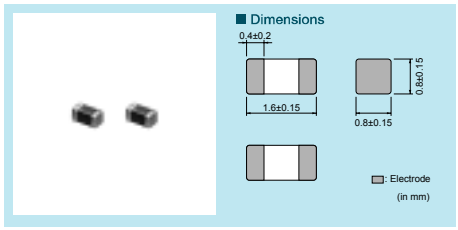
●1005 high frequency improvement (by structure) BLM15E



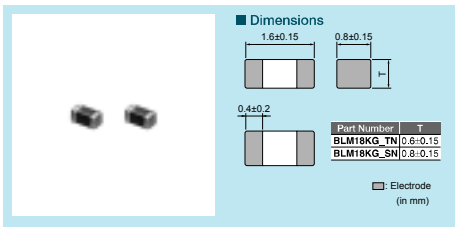
●1005 high frequency improvement (by structure and material) BLM15G



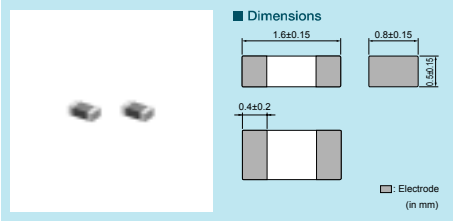
●1608 size BLM18P series



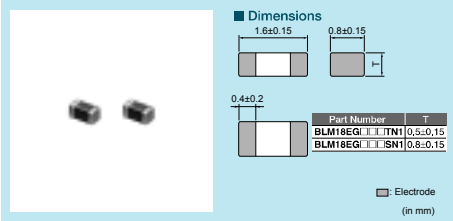
●1608 for 6A 600Ω BLM18K series



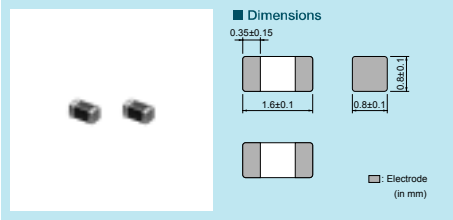
●1608 6A high performance BLM18S series



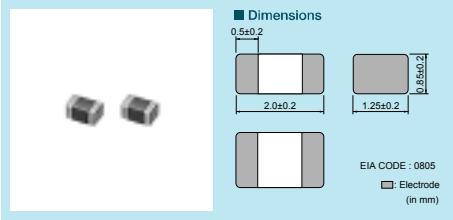
●1608 high frequency improvement (by structure) BLM18E



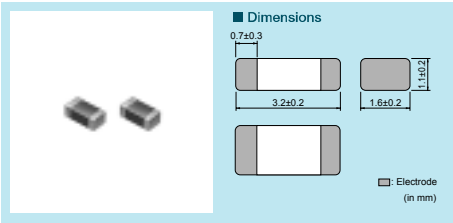
●1608 high frequency improvement (by structure and material) BLM18G



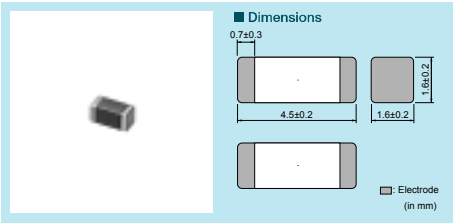
●2012 size BLM21P series



●3216 size BLM31P series



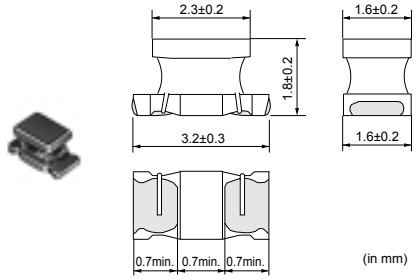
●4516 size BLM41P series



5.7.2 Choke coils

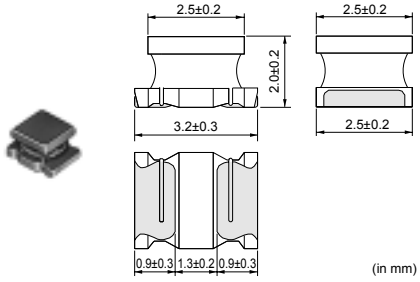
This product group reduces direct current resistance.

●3216 size LQH31C series



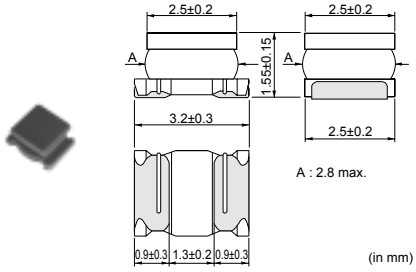
(in mm)

●3225 size LQ32C series



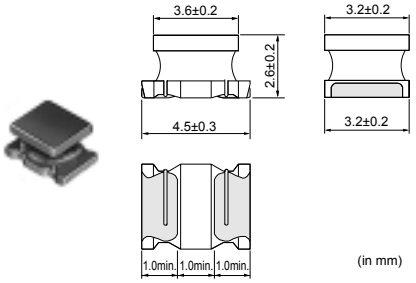
(in mm)

●3225 size low-direct current resistant type LQH32C_33, 53 series



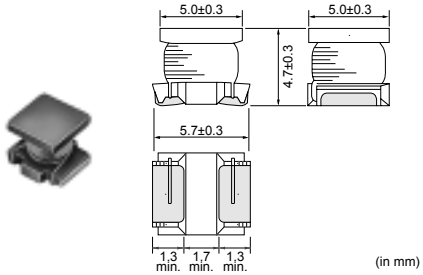
(in mm)

●4532 size LQH43C series



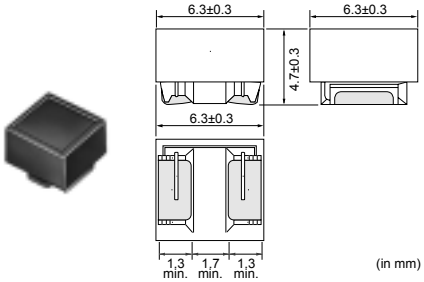
(in mm)

●5750 size LQH55D series



(in mm)

●6363 size LQH66S series

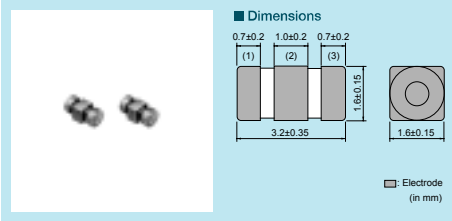


(in mm)

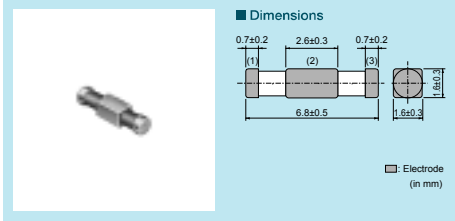
5.8 Lineup of LC filters suitable for power supplies

The NFE series in combination of ferrite beads and feed-through capacitor with excellent high frequency characteristics, and the BNX series combined with grounds are available. Generally, the BNX series is used mainly for a power supply input part such as power supply connectors, not for decoupling circuits described in this manual.

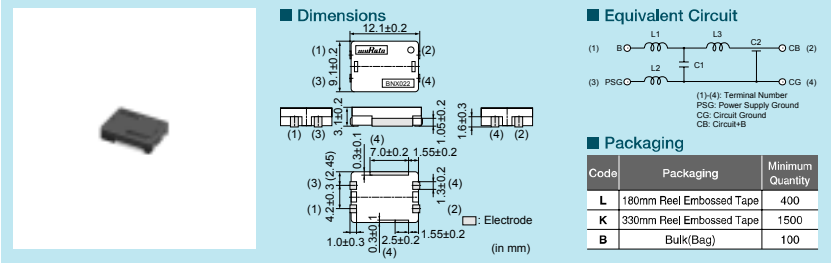
●3216 size NFE31P series



●6816 size NFE61P series



●BNX series



Code	Packaging	Minimum Quantity
L	180mm Reel Embossed Tape	400
K	330mm Reel Embossed Tape	1500
B	Bulk(Bag)	100

6. Suppressing power supply voltage fluctuation

Thus far in previous chapters, we have mainly described noise suppression performance/insertion loss characteristics of decoupling circuits for power supplies. Starting in this chapter, we will mainly describe power supply impedance and voltage fluctuation from the viewpoint of current supply performance of power supplies.

Power supply voltage must be constant in order for a digital IC to operate correctly. As shown in Figure 6-1, when power supply current fluctuates from the IC operation, power supply voltage may fluctuate due to the influence by the wiring between the power supply module and IC, as well as the influence by the response characteristics of the power supply module itself, causing malfunction in the IC or affecting peripheral circuits with noise. It can also reduce operating speed and signal integrity in some cases.

In order to prevent this voltage fluctuation, a capacitor called a decoupling capacitor, which temporarily supplies current in the vicinity of the IC, is used. This ability of a decoupling capacitor to supply current to a capacitor is sometimes called charge supply capability.

In this chapter, we will describe the mechanism of suppressing voltage fluctuation by a decoupling capacitor using a circuit to go through simple current fluctuation as a model. The performance necessary for a capacitor to keep down voltage fluctuation is also introduced.

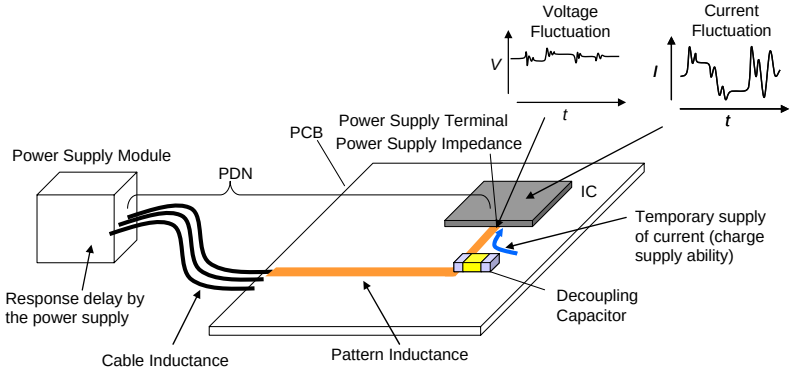


Figure 6-1 Current and voltage fluctuations

6.1 Relationship between power supply impedance and voltage fluctuation

The size of the voltage fluctuation occurring at the power supply, when a power supply terminal for the IC is connected to the power distribution network (PDN), and power supply current of the IC fluctuate as in Figure 6-2, can be expressed by the equation below:

$$\left|\Delta V\right| = \left|\Delta I \cdot Z_P\right| \qquad (6\text{-}1)$$

In this equation, ΔV, ΔI and Z_P correspond with voltage fluctuation (V), current fluctuation (A) and power supply impedance of PDN (Ω) respectively. This ΔV is voltage observed at the power supply terminal of the IC and Z_P is likewise impedance observed at the power supply terminal.

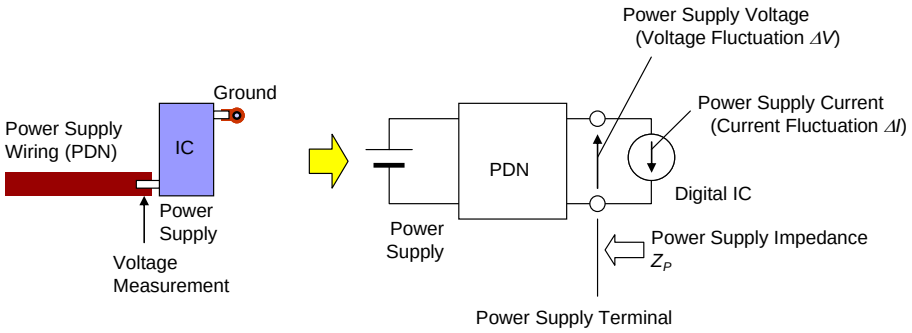
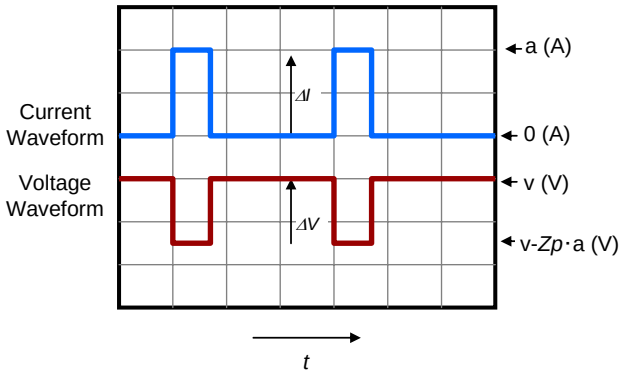
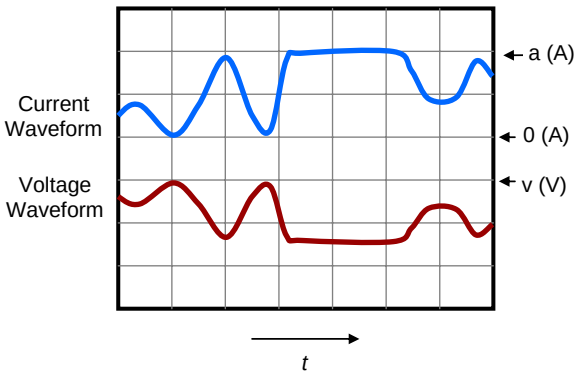


Figure 6-2 Measurement position of voltage fluctuation

An example of voltage waveform when power supply voltage fluctuates is shown in Figure 6-3. In this case it is understood that the power supply impedance is resistivity without frequency characteristics. Figure 6-3 (a) shows a case where the current simply varies stepwise, and Figure 6-3 (b) fluctuates in a slightly more complex pattern. In either case, voltage fluctuation appears in correspondence with current fluctuation (when current increases voltage decreases).



(a) When current fluctuates step-wise



(b) When current fluctuate in a complex manner

Figure 6-3 An example of voltage fluctuation in relation with current variation

6.2 Voltage fluctuation when a capacitor is present

In an actual PDN, impedance would have reactance as well as frequency characteristics instead of resistivity due to the inductance from the decoupling capacitor and wiring, and

consequently the voltage waveform would appear differently from the current waveform showing complex changes. An example of the measurement results is shown in Figure 6-4.

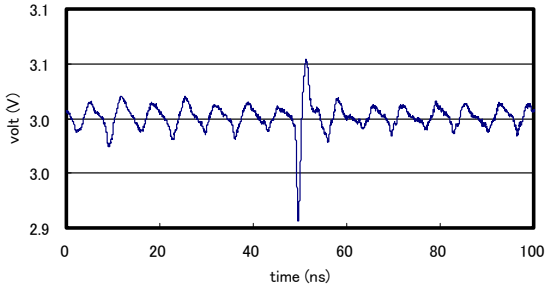


Figure 6-4 Measurement example of digital IC power supply voltage (3V line)

Therefore, we will consider a voltage waveform where current fluctuates stepwise, in order to understand the basic voltage fluctuation when using a decoupling capacitor.

Let us consider the voltage fluctuation when current flows through a power supply using a simple model illustrated in Figure 6-5. For the purpose of simplicity, let us assume there are no peripheral elements including wiring inductance, and PDN consists of only one capacitor. Voltage fluctuation is calculated with a circuit simulator then, assuming that the power supply current of the IC fluctuated stepwise as shown in 6-3 (a). We set power supply voltage to be 3V, power supply impedance to be 0.5Ω, current amplitude to be 1A, launching time to be 10ns and pulse width to be 1μs.

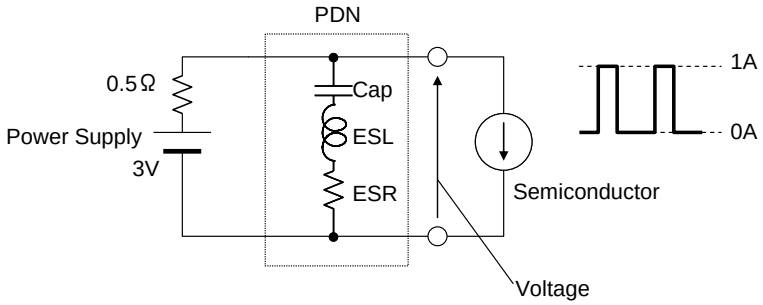


Figure 6-5 Voltage fluctuation calculation model

Calculation results are shown in Figure 6-6. In order to check the trend, three types of capacitors, 2μF, 5μF, and 10μF were designated. Each capacitor is understood to have 10nH ESL (includes mounting inductance ESL_{PCB} assuming the use of an electrolytic capacitor with lead) and 50mΩ ESR.

The graph on the left of Figure 6-6 is voltage waveform, and current waveform is indicated above for a comparison purpose. The graph on the right of Figure 6-6 indicates frequency characteristics of the capacitor impedance.

For the voltage waveform, a spike is observed at the launching stage, and the voltage decreases gradually due to the discharge characteristics of the capacitor. After that, we can observe a gradual increase in voltage as the current pulse ends and the capacitor begins to recharge. Since charge and discharge time of a capacitor is relative to the capacitance, the slope of the curve changes according to the capacitor's capacitance, causing the range of

voltage fluctuation to change as well.

As we can see from the result of Figure 6-6, when capacitance is larger, voltage fluctuation from charge and discharge will become smaller. Also, the scale of fluctuation in this section corresponds with the size of impedance for the capacitive zone of the low frequency side for the impedance characteristics on the right. When impedance is smaller (the lower curve in the graph), the range of voltage fluctuation becomes smaller. In order to reduce voltage fluctuation by this capacitor charge and discharge, it is necessary to use a capacitor with a large enough capacitance.

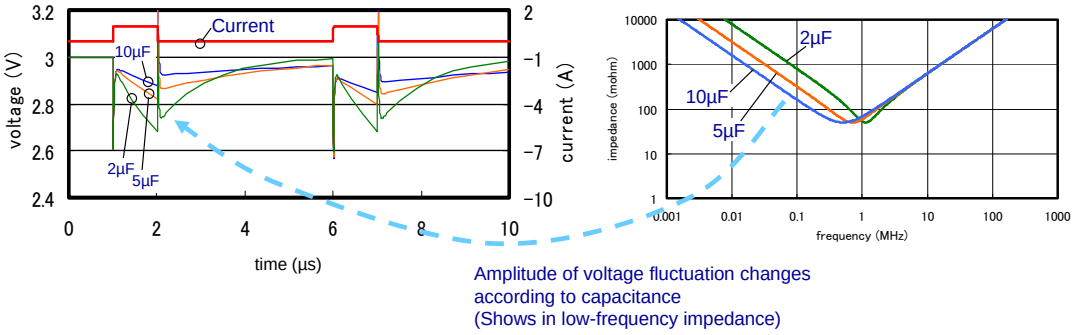


Figure 6-6 An example of the voltage waveform when using a capacitor (calculated values)

In order to observe the spike at the launching time for the calculation results of Figure 6-6 in more detail, Figure 6-7 shows an expanded time axis for a 10μF capacitor. Calculation results for an ideal capacitor without ESR or ESL is also graphed for comparison purposes. While no spike occurs for an ideal capacitor, a spike occurs for the capacitor including ESR and ESL at the launching time. The size of the spike tends to correspond mainly with ESL. In the impedance characteristics on the right side, the capacitor corresponds with the high frequency impedance where the capacitor becomes inducible (small impedance: the curve toward the bottom has a smaller spike).

When this spike is deep, voltage fluctuation may not stay within the rated power supply voltage even if a capacitor with a sufficient capacitance is used. If this spike causes a problem, ELS must be reduced.

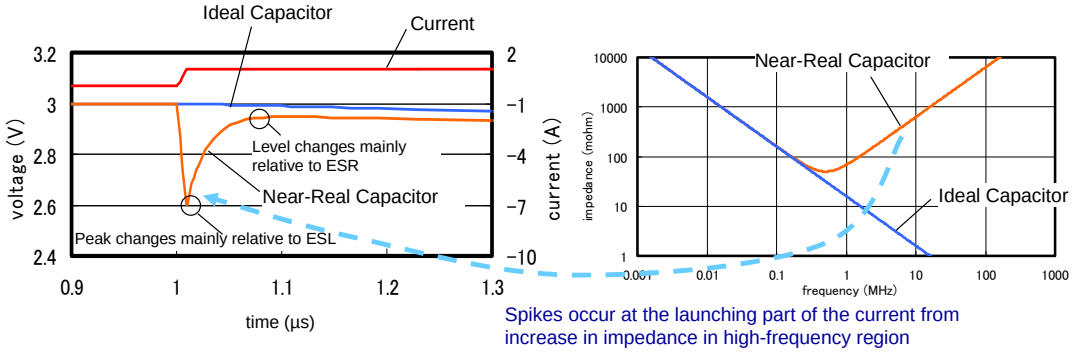


Figure 6-7 Launching part of the voltage waveform when using a capacitor

Since the size of this spike also corresponds with the size of current fluctuation (dI/dt) in

addition to capacitor's ESL, the spike may not be very evident when voltage fluctuation is relatively small. This calculation is based on the launching time of 10ns (dI/dt = 1 x 10^8 A/s).

6.3 Suppressing spikes with parallel capacitors

In order to suppress the spike from the current fluctuation at launching time, relatively small-capacitance capacitors with excellent frequency characteristics can be used in parallel. Figure 6-8 shows an example of a waveform when capacitors are used in parallel. In this case, in addition to a 10µF capacitor, a 1µF MLCC (ESL is 2nH taking ESL_{PCB} into consideration and ESR is 10mΩ) is supposed to be used. The calculation results of the figure show that the depth of the spike is halved by adding those capacitors. This effect corresponds with the fact that the high frequency impedance is reduced in terms of the impedance characteristics shown in the right side of the figure.

We can also add capacitors with smaller capacitance to further suppress this spike.

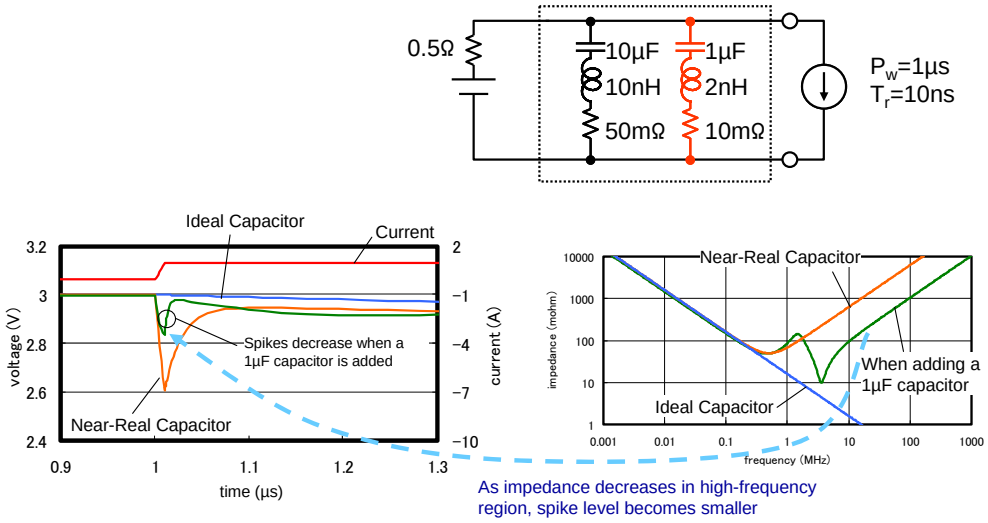


Figure 6-8 Change in waveform when capacitors connected in parallel are added

As seen above, connecting capacitors in parallel has a certain effect for suppressing the spike. However, antiresonance between neighboring capacitors may cause a problem, as described in Chapter 3. Figure 6-9 shows an example of intentionally creating such a condition.

In this case, the calculation results for using a 0.1µF capacitor in place of the 1µF capacitor mentioned above are shown. Although the size of the spike is unchanged from the 1µF capacitor, a strong surge in the waveform passed the spike (ringing with an approximately 0.2µs frequency). The frequency of this surge corresponds with the antiresonance frequency over the impedance curve. When a surge is large like this, we must take caution in avoiding going over the acceptable limit for power supply voltage fluctuation.

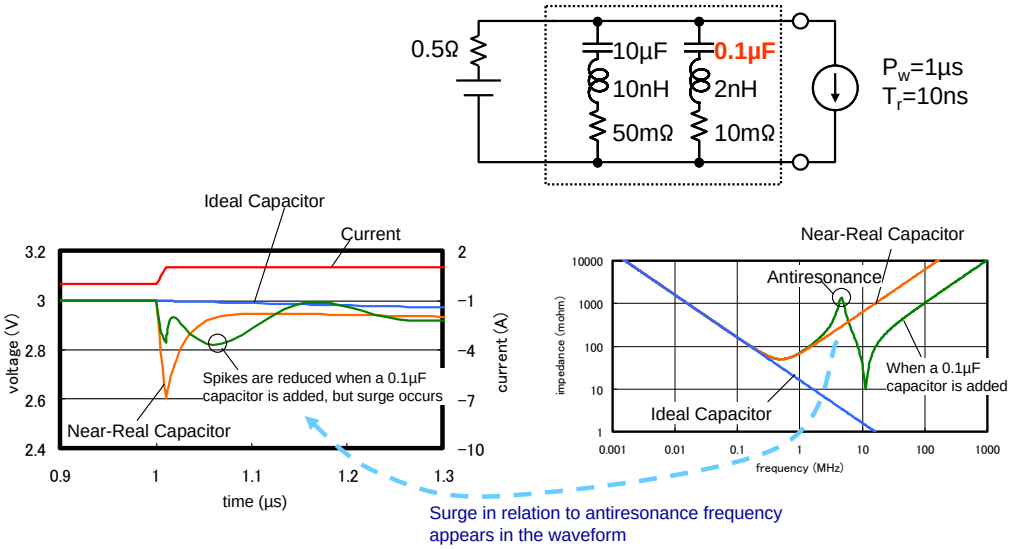


Figure 6-9 When parallel capacitors are resonating

6.4 Suppressing spikes with low-ESL capacitors

Using a capacitor with small ESL is another way to keep the spike small. Figure 6-10 shows the results of the calculation. We will assume that the low-ESL capacitor introduced in Chapter 4 is used, and capacitance is set to be 10μF, ESL is set to be 0.2nH, and ESR is set to be 50mΩ. As we can see from this figure, under these conditions, the spike is almost totally eliminated and ringing in the case of combined capacitors is not observed either. Therefore, we can see that low-ESL capacitors are advantageous for suppressing voltage fluctuation.

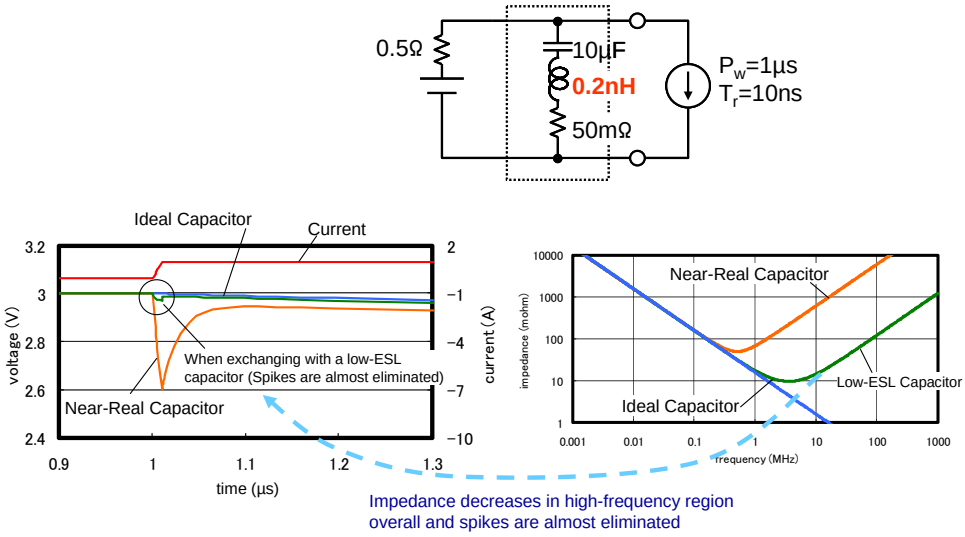


Figure 6-10 When using a capacitor with small ESL

6.5 Voltage fluctuation when the pulse width is wide

When the pulse width of the current is wide, we will need to wait for the power supply response, since a capacitor alone cannot maintain the voltage. In Figure 6-11, delay in

power supply response is expressed as inductance $L_{PowerDelay}$, to simply simulate voltage fluctuation when the pulse width is long. The calculation results in this case are indicated in Figure 6-12.

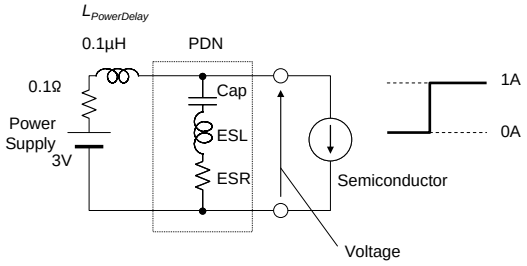


Figure 6-11 Simulation circuit when pulse width is wide

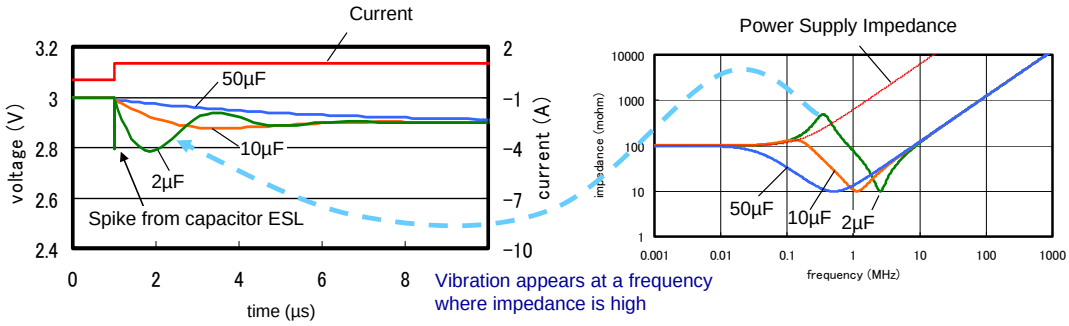


Figure 6-12 Calculation results when pulse width is wide

From Figure 6-12, we see that there is a possibility that more low frequency surge is observed over the voltage waveform depending on the capacitance of a capacitor. We can assume that there is a form of resonance occurring between the response time of the power supply and the capacitance of the capacitor. The frequency of this surge corresponds with the frequency with high impedance for the impedance characteristics on the right in Figure 6-12.

As we can see from the result of comparing capacitors in Figure 6-12, this surge is more evident when the capacitance is relatively small (2μF in the figure). Therefore, we will consider the necessary capacitance for the capacitor to eliminate the surge.

When we consider the circuit in Figure 6-11 as a type of RLC serial resonance circuit, damping condition for the resonance circuit is as the following: [13)]

$$C \geq \frac{4L_{PowerDelay}}{R^2} \tag{6-2}$$

In this case, C represents the capacitance of the capacitor and R represents output resistance of the power supply (for the purpose of simplicity, we have neglected the influence of ESR and ESL). The possibility for the surge to occur becomes small if we use a capacitance larger than C. For example, if we apply the conditions indicated in Figure 6-12 to equation (6-2), the necessary capacitance for the capacitor becomes approximately 40μF

(when we look at the case with 50μF capacitor, the surge is completely eliminated).

We have assumed that the main cause of delay in the power supply response is the inductance of the wiring from the power supply module to the IC, and expressed characteristics of the power supply as $L_{PowerDelay}$. In some cases we need to take delay in response of the power supply module itself. In such a case, we will let response time be $T_{PowerDelay}$(s) and we will make a model assuming $L_{PowerDelay}$ to be approximately

$$L_{PowerDelay} = R \cdot T_{PowerDelay} \tag{6-3}$$

from the time constant of the RL serial circuit.

In a real-life situation, since it is not plausible to express the response characteristics of a power supply as inductance, the value calculated with the method above is purely an estimate. Also, with a smoothing capacitor used for the power supply output, we cannot apply the method above since we need to consider totally different elements such as power supply capacitance and output voltage range.

7. Location of a capacitor for suppressing power supply impedance

In Chapter 6, we described the relationship between voltage fluctuation and power supply impedance, as well as voltage fluctuation waveform when using a decoupling capacitor. However, we did not touch on the influence from capacitor mount wiring. In order to suppress voltage fluctuation in an IC, impedance relative to the power supply terminal of an IC must be made small. However, normally there is some kind of printed wiring between a power supply terminal and a capacitor. Since inductance of this wiring is significant compared with the capacitor's ESL, it is necessary to make the wiring inductance small in order to make impedance relative to the power supply terminal small.

Inductance of this wiring is influenced by a pattern configuration or the distance to the capacitor. In this chapter, we will describe printed circuit design to reduce inductance for the wiring connecting an IC and a capacitor, in order to suppress power supply impedance below a certain value under high frequency.

7.1 Power supply impedance relative to an IC

Although power supply wiring between an IC and a capacitor does not have a set configuration, making it difficult to make a model, we will assume that it can be expressed as a micro strip line (MSL) for the purpose of discussion. Let us consider impedance of PDN with several capacitors attached as illustrated in Figure 7-1.

Let us assume that capacitors are laid out hierarchically in order of 10μF, 2.2μF and 0.47μF (in Figure 7-1, the size of the illustrated capacitors corresponds with their capacitance). A small-size and small-capacitance capacitor is located right near the IC and a large-size and large capacitance capacitor is located relatively far from the IC.

Figure 7-2 shows the calculation results of impedance at PDN relative to IC power supply terminals A, B, and C in such a model. The blue line represents impedance where all capacitors are connected to PDN in Figure 7-1, and the red line represents impedance with only the capacitor nearest to the power supply terminal connected.

From the results of Figure 7-2, we can tell that the power supply impedance is mainly formed from the nearest capacitor when frequency is over 10MHz. This signifies that impedance in a high-frequency zone is dominated mainly by inductance, and influence from relatively distant capacitors can be negligible due to the increase in effective ESL from the wiring inductance. (In this diagram, the PDN as a whole and the closest capacitor show a relatively large difference for point A. This is considered to be due to the fact that the nearest capacitor and the rest of the PDN are connected parallel to each other left and right.)

Since in the high-frequency zone impedance of the nearest capacitor becomes dominant, in order to reduce impedance of a PDN below a certain value, we only have to consider the nearest capacitor and the wiring it is connected to. We will focus on wiring design up to the nearest capacitor with such a premise.

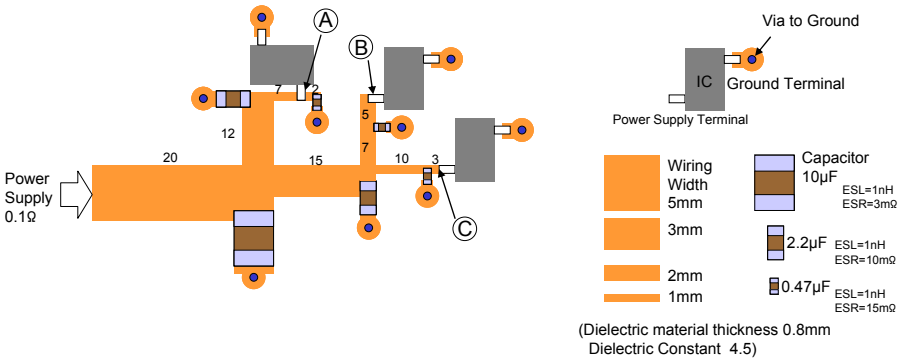
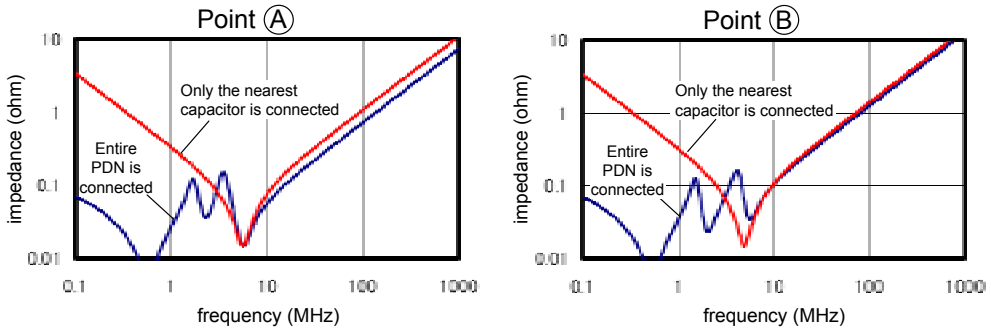
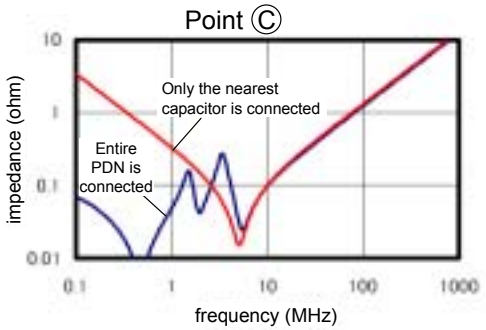


Figure 7-1 Modeling diagram of power supply impedance calculation



(a) Point A (b) Point B



(c) Point C

Figure 7-2 Calculation results of power supply impedance

7.2 Simple estimation of power supply impedance relative to an IC

Assuming that the wiring from the IC's power supply terminal up to the nearest capacitor may be expressed as an MSL, by modeling it as in Figure 7-3, impedance of this capacitor relative to the power supply terminal, $Z_{PowerTerminal}$ can be expressed with the following equation:

$$Z_{\mathrm{PowerTerminal}} = Z_{cap} + Z_{line} \tag{7-1}$$

In this equation, Z_{cap} is impedance of the capacitor and Z_{line} is impedance of the wiring leading to the capacitor. Z_{cap} includes impedance of the pad for mounting the capacitor and a via.

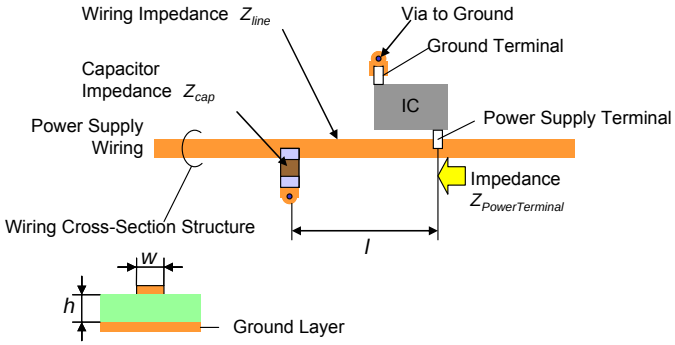


Figure 7-3 Wiring model to the nearest capacitor

Z_{line}, which is impedance for the wiring, can be considered short-circuited at the tip (since a capacitor is connected to the model illustrated in Figure 7-3, it can be considered short-circuited under high frequency); if the length of wiring is sufficiently short compared against the wavelength of the corresponding frequency, the inductance can be approximated by inductance. We will let inductance of the wiring be L_{line}. Also, in the high-frequency zone exceeding self-resonant frequency, the impedance of capacitor Z_{cap} is formed by the ESL of the capacitor, ESL_{cap}. Therefore, impedance relative to the power supply terminal of an IC, $Z_{PowerTerminal}$, can be expressed as the following equation:

$$Z_{\mathrm{PowerTerminal}} = Z_{cap} + Z_{line} \cong j2\pi f(ESL_{cap} + L_{line}) \qquad (7\text{-}2)$$

We can use inductance per unit length of MSL multiplied by length l as the value for L_{line}. Various approximation equations are proposed based on the inductance per unit length of MSL correlating with characteristic impedance. [14] However, when handling a case with wide wiring width like a power supply, its equation may become complex. Therefore, the following equation is proposed to very roughly approximate L_{line}:

$$L_{line} = 0.4l\left(\frac{h}{w}\right)^{0.6} \times 10^{-6} \quad (H) \qquad (7\text{-}3)$$

In this equation, h is the thickness of the dielectric material considering the power supply wiring as an MSL, w is the width of the wiring, and l is the length of the wiring (units are all millimeters). By substituting L_{line} with ESL_{cap} of the capacitor used in the equation (7-2), we can estimate the impedance relative to the power supply terminal of the IC in the high-frequency region (where the capacitor becomes inducible). Note that we need to include inductance from the capacitor mounting pad and via (ESL_{PCB}) in ESL_{cap} used here.

7.3 Possible range for placing the closest capacitor of an IC

We can calculate by inversion the length of wiring necessary to control power supply

impedance below a target value, approximating inductance of wiring with a simple equation in (7-3). Let the target impedance relative to the power supply of the IC be Z_T and the target frequency, the largest frequency necessary to satisfy this impedance is $f_{T@PCB}$, the maximum allowable length of wiring l_{max} is as the following.

As mentioned earlier, impedance relative to the power supply terminal shows inducibility under high frequency; we will only consider the inductance. We can derive the largest allowable inductance for the wiring, L_{line_max}, by substituting Z_T for the power supply impedance $Z_{PowerTerminal}$ and f_T for the frequency f in the equation (7-2).

$$L_{\text{line\_max}} \cong \frac{Z_T}{2\pi f_T} - ESL_{cap} \tag{7-4}$$

We can derive the maximum allowable length for the wiring, l_{max}, by substituting L_{line} with this L_{line_max} in the equation (7-3):

$$l_{\max} = 2.5\frac{L_{line\_\max}}{\left(\frac{h}{w}\right)^{0.6}} \times 10^6 \cong 0.4\frac{Z_T - 2\pi f_{T@PCB} ESL_{cap}}{f_{T@PCB}\left(\frac{h}{w}\right)^{0.6}} \times 10^6 \quad \text{(m)} \tag{7-5}$$

As shown in figure 7-4, when placing the closest capacitor within this l_{max} from the power supply terminal of an IC, we can achieve the target impedance in the high-frequency zone. We will call this l_{max} the maximum allowable wiring length. When l_{max} is large, we have more flexibility in the location of the capacitor.

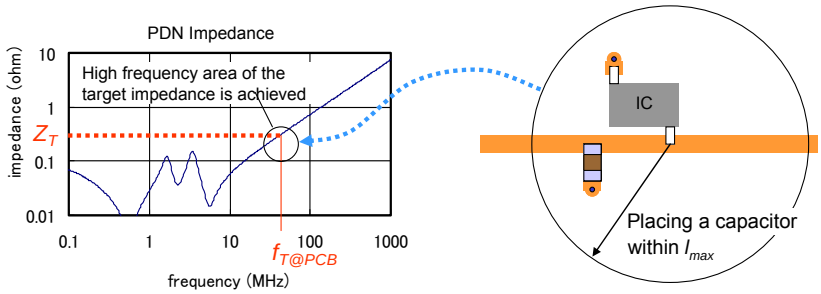


Figure 7-4 Placing a capacitor within l_{max}

On the other hand, in terms of the capacitor, l_{max} can be seen as the capacitor's effective range for containing the power supply impedance to less than Z_T. As shown in Figure 7-5, when the power supply terminal of an IC is placed less than l_{max} from the capacitor, one capacitor can suppress multiple power supply impedances of the IC at less than Z_T. As we can see from the equation (7-5), this capacitor has a wide effective range since l_{max} of a capacitor with small ESL_{cap} becomes large.

When one capacitor covers multiple IC power supplies as in Figure 7-5, current may become large when the timing of IC operations match, necessitating the change in the target impedance Z_T. Also, when the wiring connecting the capacitor and multiple ICs overwraps (like two ICs on the right), voltage induced in the overwrapped wiring may cause noise interference between ICs. When these problems occur, a capacitor should be

used for every IC.

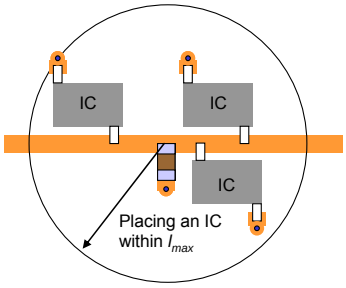


Figure 7-5 Placing an IC within l_{max}

If $2\pi f_T ESL_{cap}$ is larger than Z_T in the equation (7-5), a capacitor cannot be used since l_{max} will be less than zero. This indicates that the ESL of the capacitor itself is too large, making it unable to achieve the target impedance Z_T even if the wiring is connected with ideal zero inductance. In such a case, we need to either use a capacitor with small ESL or use multiple capacitors in parallel to make an equivalence of small ESL_{cap}.

7.4 Guideline for the maximum allowable wiring length, l_{max}

We can assume from the equation (7-5) that when using a capacitor with small ESL_{cap}, l_{max} becomes large, increasing the flexibility of the capacitor location. Also, this l_{max} should be influenced by the dimension of intersection for the printed wiring (h and w). Therefore, in order to confirm this tendency, and show a guideline for wiring design, we have calculated l_{max} varying wiring width, thickness of the dielectric material, and mounting conditions for the capacitor as shown in Figure 7-6. The results are shown between Figures 7-7 and 7-10.

We assume low-ESL capacitors such as 3-terminal capacitor and LW reverse capacitor or MLCC are used in this case. We set the upper limit frequency, $f_{T@PCB}$ of target impedance tentatively at 100MHz assuming that the measurement is taken at the power supply terminal external to an IC. (In an actual situation, the value $f_{T@PCB}$ varies greatly depending on the IC used.)

From calculation results in Figures 7-7 through 7-10, we can tell that in order to make l_{max} large, low-ESL capacitor, thin dielectric substrate, and wide wiring are effective. Also, the smaller the target impedance is, the larger the fluctuation in l_{max} tends to be due to capacitor ESL.

As seen in this section, l_{max} becomes large with a low-ESL capacitor making capacitor placement more flexible. Also, the effective range of one capacitor becomes larger, enabling the use of fewer capacitors to cover a wide area of PDN.

When targeting less than 0.2Ω@100MHz for Figures 7-7 through 7-10, using one MLCC would cause $2\pi f_T ESL_{cap}$ to become larger than Z_T as described earlier, making it “impossible to wire”. In such a case, we need to use multiple capacitors in parallel as described in Chapter 8, to make ESL_{cap} smaller. Also, the use of a low-ESL capacitor, introduced in Chapter 4, would be effective in making ESL_{cap} smaller.

The descriptions above presume that the power supply wiring can be treated as MSL and

target frequency is sufficiently low for the wiring length. Therefore, they would not apply if a single-sided substrate which cannot be treated as MSL is used or if wiring resonance occurs due to high frequency.

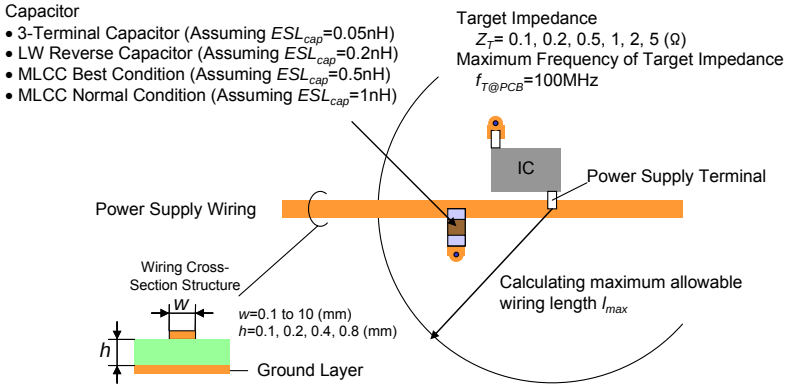


Figure 7-6 Calculation conditions

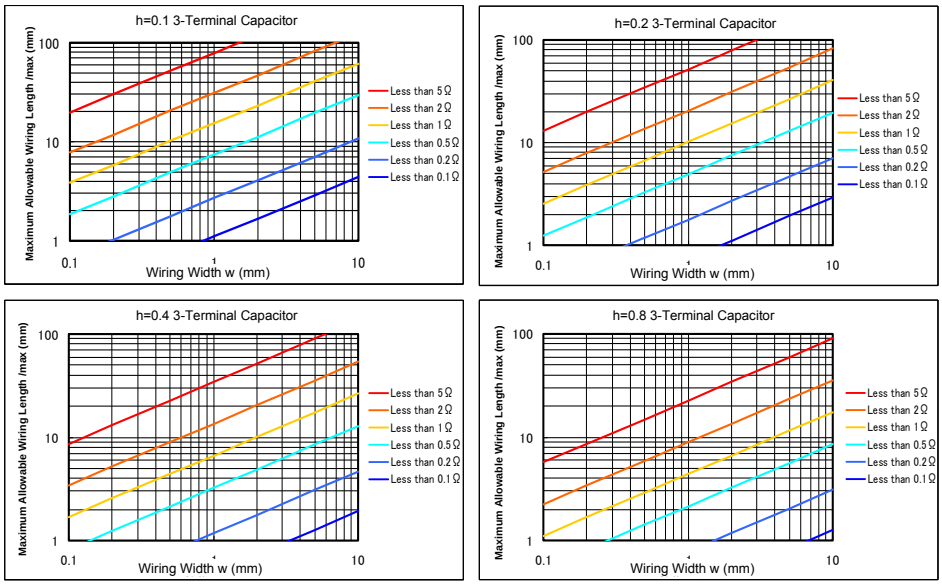


Figure 7-7 3-Terminal Capacitor Best Conditions (ESL_{cap}=0.05nH)

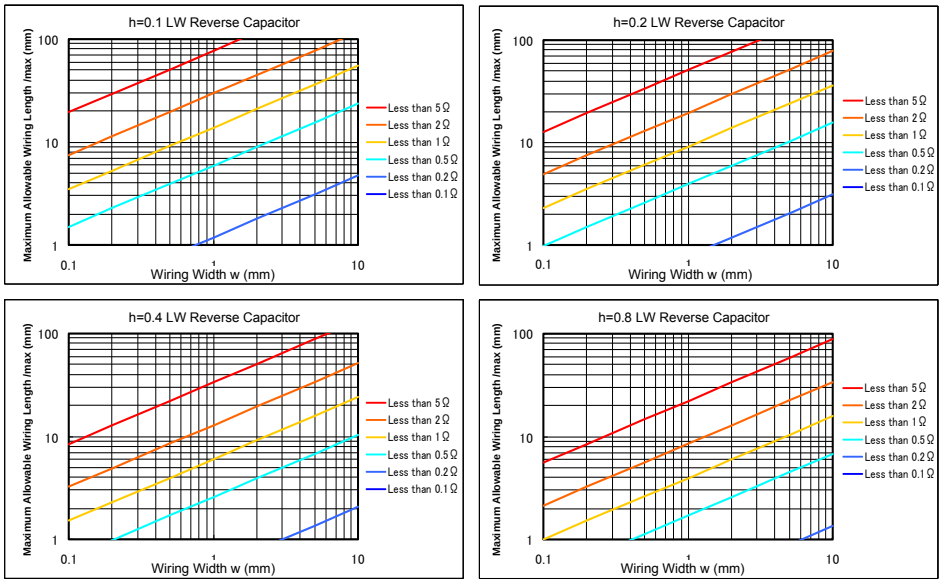


Figure 7-8 LW Reverse Capacitor Best Conditions (ESL_{cap}=0.2nH)
(Cannot be wired when under Z_T=0.1Ω)

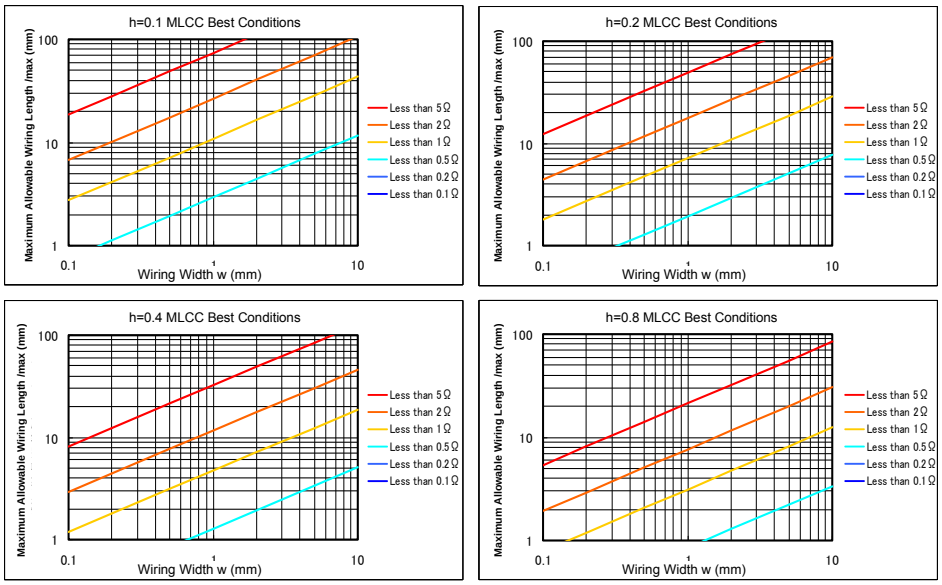


Figure 7-9 MLCC Best Conditions (ESL_{cap}=0.5nH)
(Cannot be wired when under Z_T=0.2Ω)

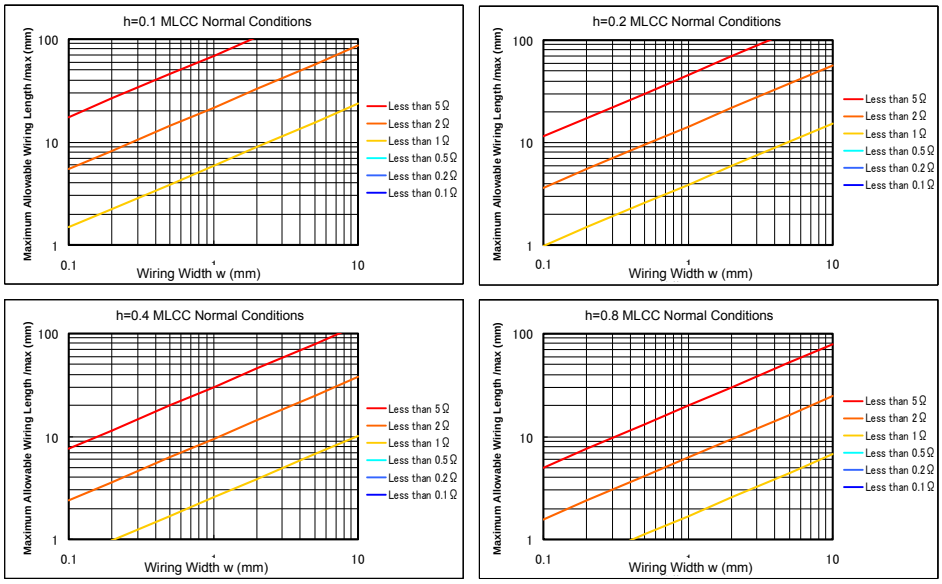


Figure 7-10 MLCC Normal Conditions (ESL_{cap}=1nH)

(Cannot be wired when under Z_T=0.5Ω)

8. Configuration of PDN combined with capacitors

Power supply wiring and decoupling capacitors connected to a power supply terminal of an IC as a whole is called PDN. [1)] One of performance indicators for this PDN is impedance (power supply impedance) at PDN relative to the power supply terminal of an IC. When the power supply impedance is smaller for the PDN, the current supply performance and power integrity (PI) will be higher. As described in Chapter 6, when the power supply impedance is smaller, voltage fluctuation when power supply current for the IC fluctuates becomes smaller.

In a large-scale and high-speed IC, power supply current strongly fluctuates and its frequency is high; power supply impedance must be made small over a wide frequency range. In such a case, since one capacitor cannot achieve the necessary impedance, multiple capacitors are positioned hierarchically as shown in Figure 8-1 to achieve the target power supply impedance. We will now describe the hierarchical positioning of capacitors to fulfill the target impedance.

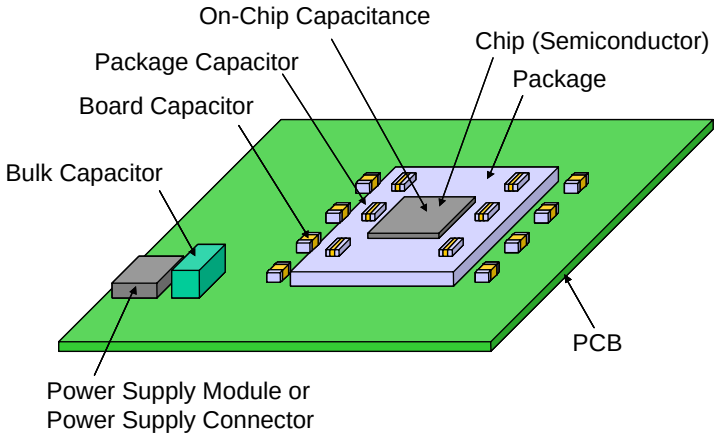


Figure 8-1 An example of decoupling capacitor placement

8.1 Hierarchical positioning of decoupling capacitors

When capacitors are positioned hierarchically as in Figure 8-1, each of the capacitors is named depending on its position, as in Figure 8-1, and connected as illustrated in Figure 8-2. [15)] On-chip capacitance (capacitance formed on silicone) is not a component, but is added because it shares the same function.

Those capacitors function as a “reservoir of charge” from the viewpoint of the current supply function of the PDN. In other words, by instantaneously handling a local current request near a semiconductor, they maintain the time-to-respond and voltage for power supply modules. Also from the viewpoint of the frequency characteristics of power supply impedance, as frequency increases impedance increases for the power supply module without any help, capacitors are placed near ICs to reduce impedance in high-frequency region.

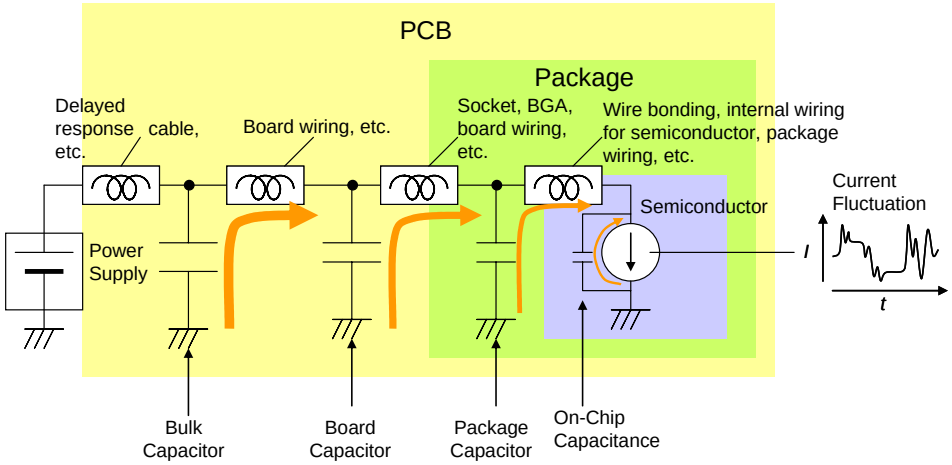


Figure 8-2 Current supply model from capacitors

As described in Chapter 7, we need to consider wiring inductance in addition to capacitors for power supply impedance relative to the IC. In Figure 8-2, the influence of the wiring between the semiconductor and each of the capacitors is expressed in terms of inductance (for the purpose of simplicity, capacitance and resistance of the wiring is neglected). Since the wiring inductance of the far capacitors becomes large, impedance cannot be reduced under high frequency. Conversely, we can expect capacitors near the semiconductor to stay effective in the high frequency.

In this sense, if we can gain sufficient capacitance from the on-chip capacitance, it would be ideal for reducing power supply impedance. In reality, this is difficult due to space constraints. Therefore, we place capacitors hierarchically from near to far from the semiconductor as shown in Figure 8-2 to achieve target power supply impedance.

8.2 Impedance of PDN

The target value for power supply impedance necessary for IC operation is called target impedance (Z_T), and it is necessary to stay below the target value for the frequency range necessary as shown in Figure 8-3 (although the target value is a constant in the figure, it may vary depending on the frequency).

PDN consists of a power supply, a decoupling capacitor, and wiring to connect them, etc. PDN must be designed to meet the target impedance as a total. (Although a target impedance must be selected taking operations of the IC and the circuit in consideration, it may not be explicit in some cases. We will introduce the guideline for its set-up in Section 8.7.)

Ideally, power supply impedance should be expressed in terms of impedance relative to the transistor on the silicon wafer of the model in Figure 8-2. However, it is not practical to take a measurement over the wafer. In reality, the power supply impedance needs to be expressed by establishing a point of measurement such as a BGA terminal on the package or power supply pad over the PCB (generally, the value varies depending on the measurement location). According to the description below, it is impedance (a virtual value

since it is unmeasurable in reality) relative to the semiconductor element unless stated otherwise.

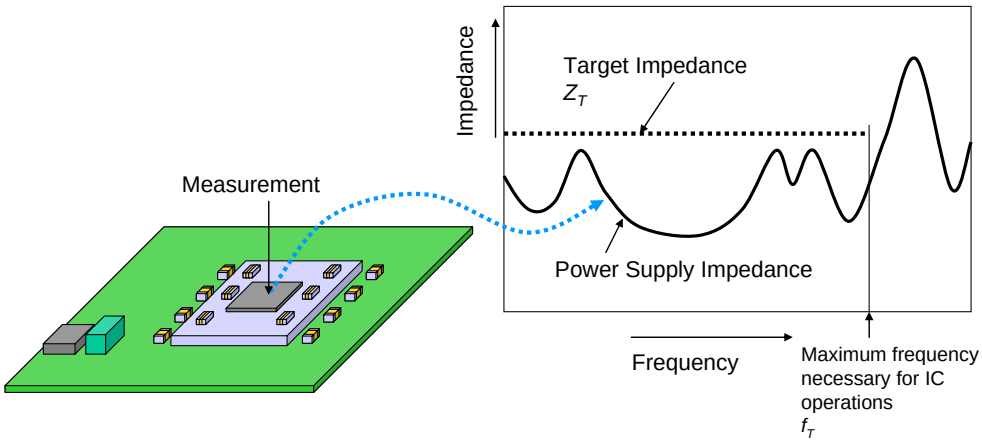


Figure 8-3 Target impedance

8.3 Hierarchical positioning of capacitors

The frequency characteristics of the impedance from the entire PDN when positioning capacitors hierarchically as shown in Figure 8-2 will become that of Figure 8-4. Target impedance is met as a total by combining frequency ranges covered by each of the capacitors. 1)

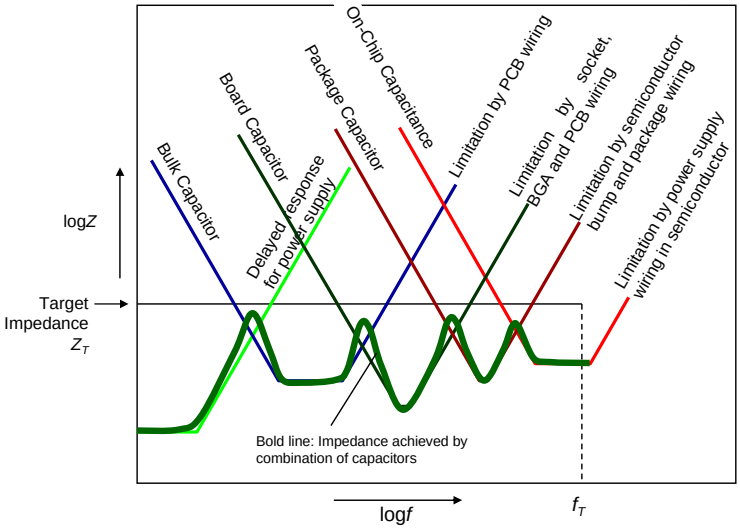


Figure 8-4 Simulation diagram for impedance from a combination of capacitors

The impedance of each capacitor shown in Figure 8-4 is not from components alone, but includes influence by wiring between semiconductor elements and capacitors as shown in Figure 8-5. The frequency characteristics of impedance at this capacitor relative to the semiconductor element become roughly V-shaped as shown in Figure 8-6 (wiring capacitance is neglected for the purpose of simplicity).

The range of this curve where it meets the target impedance Z_T is called the effective frequency range of the capacitor in this case. As shown in Figure 8-6, the lower limit f_{min} of

the effective frequency range is limited by the capacitance of the capacitor C_{cap} and the upper limit f_{max} is limited by the inductance of the capacitor ESL_{total}. This ESL_{total} includes inductance of the capacitor ESL_{cap} and inductance of wiring L_{line}. Also, this ESL_{total} in turn includes the ESL of the capacitor itself and the inductance of the capacitor mounting pad and vias.

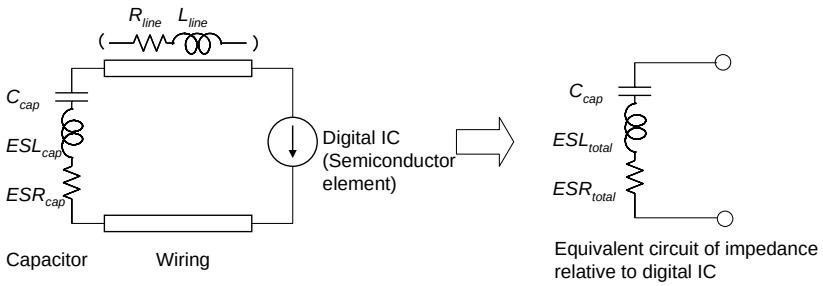


Figure 8-5 Equivalent circuit for a single capacitor

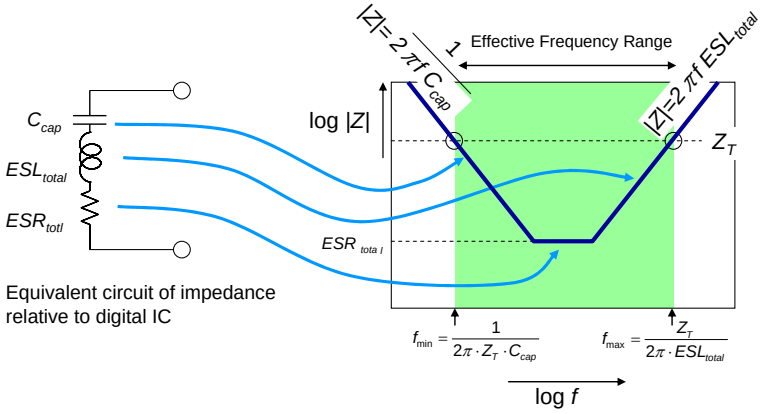


Figure 8-6 Frequency characteristics for impedance of a single capacitor

As we can see from Figure 8-6, the effective frequency range of a capacitor becomes wider when Z_T is large, and becomes narrow when Z_T is small.

The lower limit of the capacitor impedance is limited by ESR_{total}. We need to use a capacitor with its ESR smaller than Z_T for the power supply with small Z_T.

At the connecting area of the capacitor hierarchy, the capacitor on the low-frequency side (Capacitor 1) and the capacitor on the high frequency side (Capacitor 2) must be combined in such a way that the effective frequency range is overwrapped (without any gap) as shown in Figure 8-7. Therefore, when ESL_{total} of a capacitor on the low-frequency side changes, the capacitance necessary for the capacitor on the high-frequency side changes as well.

Also, as shown in Figure 8-4, impedance may increase at the connecting area for the frequency. This is due to the fact that antiresonance may occur between capacitors as described in Chapter 3. Therefore, connection within the effective frequency range must be established with sufficient margin.

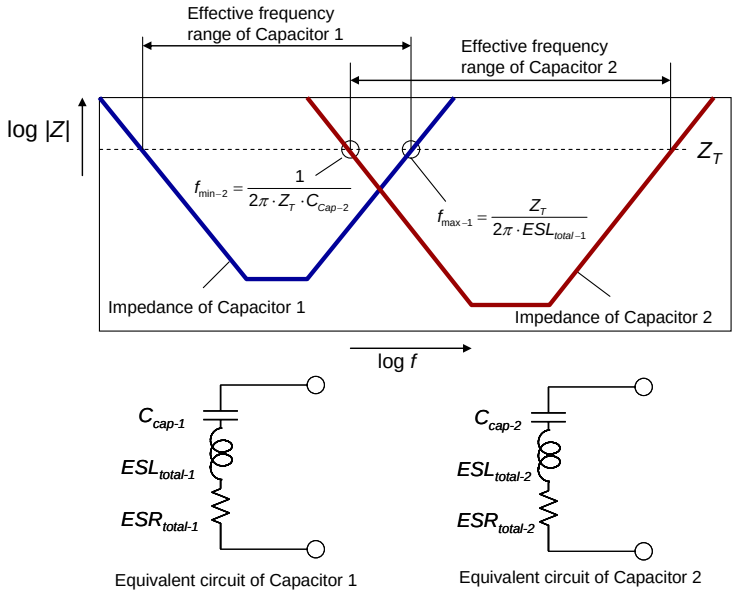
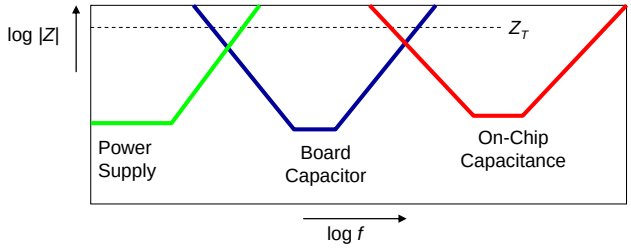


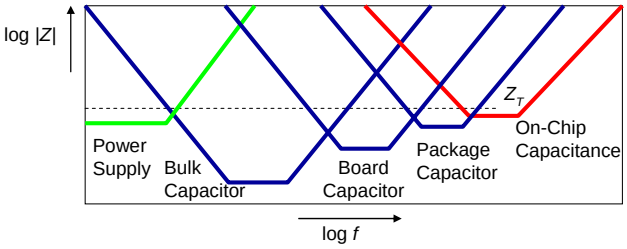
Figure 8-7 Hierarchical connection of capacitor impedance

Meanwhile, the effective frequency range of a capacitor varies depending on the level of target impedance as described previously, allowing hierarchy to be omitted. When current fluctuation of an IC is small, the effective frequency range expands with relatively high target impedance. Also, when capacitance of a board capacitor is large and a capacitor with small ESL is being used, the effective frequency range expands, making it possible to eliminate a bulk capacitor or a package capacitor front and back and reduce the number of capacitors used.

An example of simplifying hierarchy is shown in Figure 8-8.



(a) When target impedance is high



(b) When target impedance is low

Figure 8-8 An example of the hierarchical structure of capacitors

8.4 Target impedance on PCB

In the capacitor hierarchy shown in Figure 8-2, an on-chip capacitance and a package capacitor are provided on the IC, so that they cannot be controlled during the PCB design stage.

Therefore, normally the lower limit of the frequency covered by the on-chip capacitance and the package capacitor is considered as the upper limit frequency, $f_{T@PCB}$, at the PCB design stage, and designated to be the upper limit frequency for target impedance set for the power supply terminal external to the IC package. This frequency is generally considered to be 10MHz to 100MHz.

When designing a decoupling capacitor on PCB, our aim will be to meet target impedance up to this $f_{T@PCB}$ (it is not necessary to target the maximum frequency for IC operation). The measurement point for this impedance is the power source terminal of the IC package.

In the following section we will describe capacitors used hierarchically on the PCB and their use.

8.5 Bulk capacitor

A bulk capacitor is a large-capacitance capacitor covering impedance in the low-frequency region. It is positioned in a section at the power supply area, and in some cases substitutes as a smoothing capacitor for the power supply module.

As shown in Figure 8-6, the lower limit for impedance of a capacitor is limited by ESR, and the upper limit of the effective frequency range is limited by ESL and wiring inductance. Therefore, when using a capacitor with small ESR and ESL, the capacitance of a board capacitor handling higher frequency can be reduced, or capacitor layout may become more flexible.

An example comparing the impedance of an electrolytic capacitor and an MLCC is shown in Figure 8-9. In this case both capacitors are 2.2µF. Even with a low-ESR capacitor using conductive high polymer, its impedance in the frequency range over 10MHz is larger compared with MLCC. This indicates that the ESL of the MLCC is small and its upper limit for the effective frequency range is high.

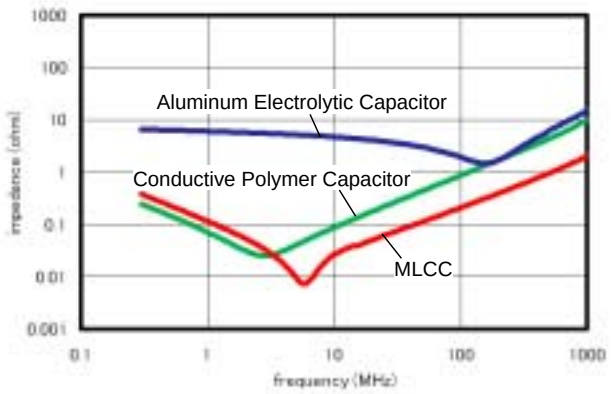


Figure 8-9 Comparison between the impedance of an electrolytic capacitor and an MLCC

8.6 Board capacitor

Impedance in a higher frequency region where a bulk capacitor does not function is handled by a board capacitor located on the PCB near the IC. Normally, an MLCC is used for this capacitor. One capacitor is sufficient for a relatively small-scale and low-speed IC, but for high-performance ICs with low target impedance, multiple capacitors in parallel may be used as shown in Figure 8-10. [2)]

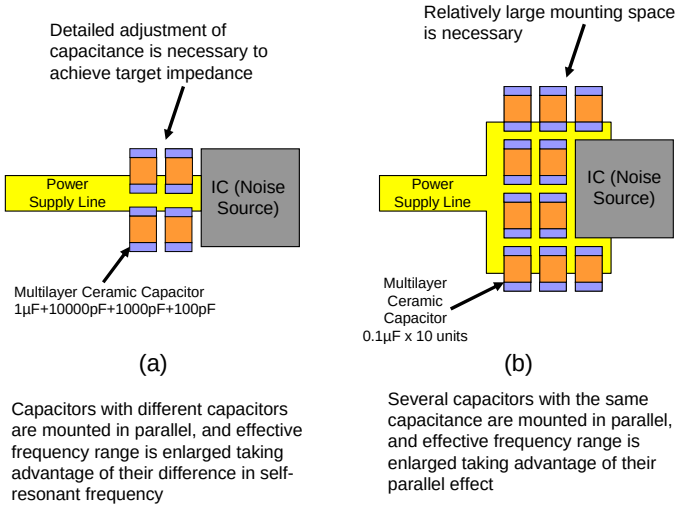


Figure 8-10 Examples of board capacitor parallel layout

Figure 8-10 (a) shows a combination of capacitors with different capacitances. Low impedance over a wide frequency range is targeted by combining capacitors with different self-resonant frequencies, taking advantage of the characteristics of capacitors where it becomes low impedance near the self-resonant frequency.

Caution must be taken in a case where impedance does not become smaller because antiresonance occurs in the gap between self-resonant frequencies of capacitors as described in Chapter 3. An example of joint impedance when using four capacitors at 1μF, 10000pF, 1000pF and 100pF in parallel is shown in Figure 8-11. The frequency characteristics of impedance appear in waves, and in some cases their impedance exceeds one 1μF capacitor at antiresonance frequencies.

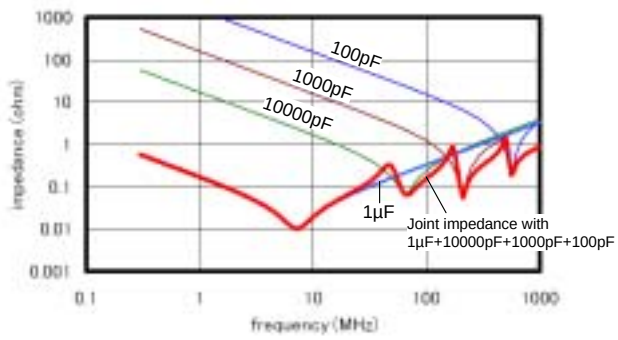


Figure 8-11 Joint impedance when capacitors with differing capacitance are used in parallel (calculated values)

Figure 8-10 (b) shows a case of capacitors with the same capacitance in parallel. In this case, as the calculation results in Figure 8-12 indicate, problems from antiresonance do not occur as frequently (calculation assumes that wiring between capacitors may be neglected). This method has an effect of capacitor impedance becoming parallel, in addition to impedance of pads and vias becoming parallel (in the case where a via is used for each capacitor). There is also the advantage that it is relatively easier to increase capacitance because of the increased number of capacitors.

On the other hand, an increased number of capacitors has the disadvantages of increased space and cost. Also, as the area increases, mounting positions of capacitors are relatively far apart, making capacitors less effective from the wiring impedance, gradually decreasing the effect of the increased number of capacitors.

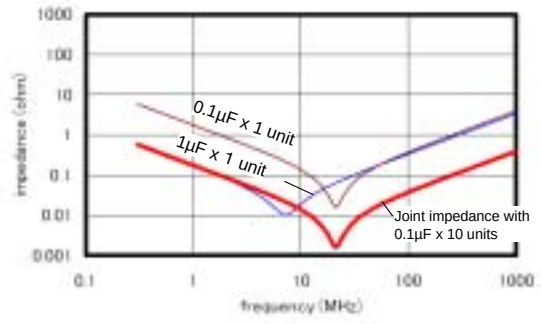


Figure 8-12 Impedance when capacitors with the same capacitance are used in parallel (calculated values)

If the method shown in Figure 8-10 gives trouble, using a low-ESL capacitor as shown in Chapter 4 will give the same effect as an increased number of capacitors with one capacitor. This is more advantageous for space and cost. Figure 8-13 shows a comparison of impedance for multiple MLCCs and one low-ESL capacitor. One low-ESL capacitor realizes impedance equivalent to using 10 MLCCs in parallel.

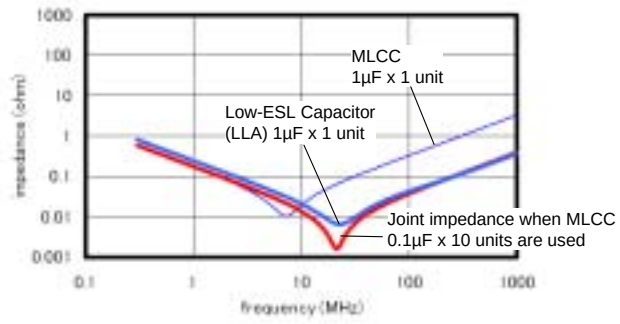


Figure 8-13 Comparison between using MLCCs in parallel and a low-ESL capacitor (calculated values)

8.7 Capacitance design of a capacitor

An example of establishing capacitance for a bulk capacitor and a board capacitor from the target impedance is shown below. As shown in Figure 8-14, we consider the case where a bulk capacitor and a board capacitor are positioned between the power supply module and the IC. Wiring is formed with MSL and the mounting positions of capacitors are roughly predetermined.

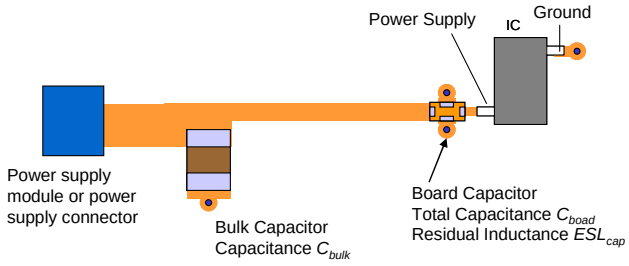


Figure 8-14 Model for designing capacitor capacitance

8.7.1 Establishing target impedance

First, target impedance Z_T is determined as shown in Figure 8-15. If the target value and maximum frequency of the power supply impedance necessary for IC operation are already known, these values are used. If they are unknown, they are established with the following equation:

$$Z_T = \frac{\Delta V}{\Delta I} \tag{8-1}$$

In this case, ΔV is the maximum allowable ripple voltage and ΔI is the maximum transient current fluctuating from the static state (if unknown, we will let it be about one-half of the maximum current value of an IC [16) 17)]). Maximum frequency $f_{T@PCB}$, of Z_T varies depending on the operation speed of an IC. If unknown, set it to be approximately 100MHz.

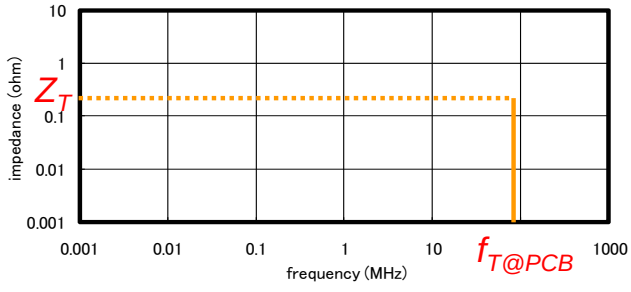


Figure 8-15 Establishing target impedance

8.7.2 Establishing capacitance of a bulk capacitor

Next, we will establish the capacitance of capacitors from the low frequency side. The first capacitor will be the bulk capacitor. Its model is shown in Figure 8-16.

When we can assume that inductance from cables between the power supply module and a circuit or printed wiring is the main factor preventing us from achieving target

impedance at the bulk capacitor mounting position when the power supply module is operating ideally, we will let this inductance be L_{Power} and establish the bulk capacitor capacitance C_{bulk} as shown in Chapter 2.

$$C_{bulk} \geq \frac{L_{Power}}{Z_T^{\,2}} \tag{8-2}$$

When the wiring consists only of printed wiring, we can use the following equation below from Chapter 7 to estimate L_{Power}.

$$L_{line} = 0.4l\left(\frac{h}{w}\right)^{0.6} \times 10^{-6} \quad (H) \tag{7-3}$$

In this equation, h is the thickness of dielectric material in MSL, w is the wiring width, and l is the wiring length.

In a case where the response characteristics of the power supply module itself are not negligible, this inductance $L_{powerResponce}$ must be calculated into L_{power} in equation (8-3). A rough estimate can be established as the following from the time constant of inductance as shown in Chapter 6.

$$L_{Power\,Response} = Z_T \cdot t_{Power\,Response} \tag{8-3}$$

In this equation, $t_{powerResponce}$ is the response speed of the power supply module.

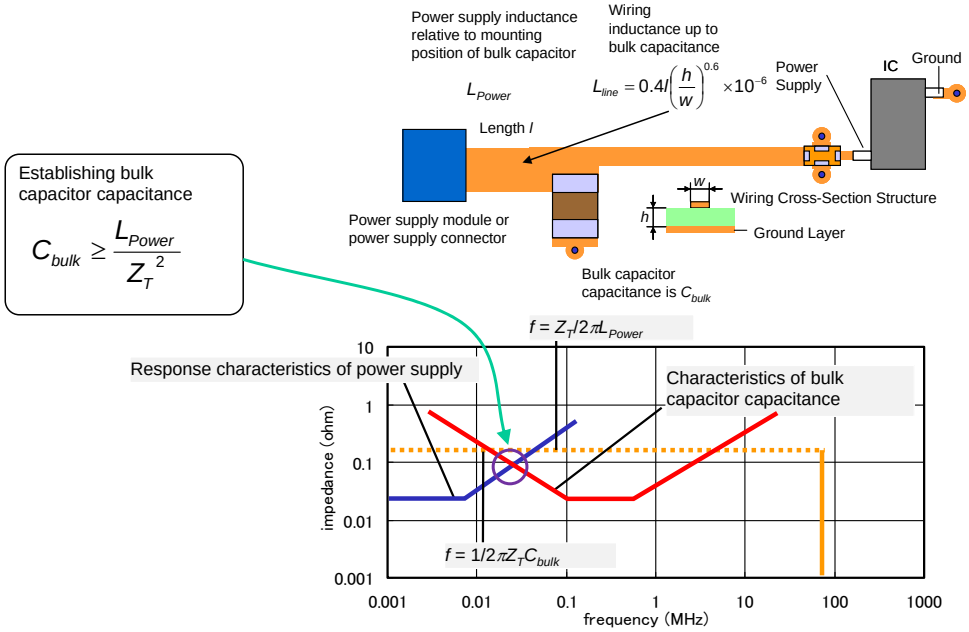


Figure 8-16 Establishing capacitance for a bulk capacitor

8.7.3 Establishing a board capacitor

Next, we will establish capacitance for the board capacitor, C_{boad}, as shown in Figure 8-17. If we let the inductance of the wiring between the bulk capacitor and the board capacitor be L_{bulk}, the necessary capacitor at the board capacitor mounting area is

$$C_{boad} \geq \frac{L_{bulk}}{Z_T^{\,2}} \tag{8-4}$$

as with the equation (8-2). Although, strictly speaking, this L_{bulk} includes the ESL of the bulk capacitor and the inductance of all wiring between the IC and the bulk capacitor, in Figure 8-17, only the wiring between the bulk capacitor and the board capacitor will represent inductance as a whole.

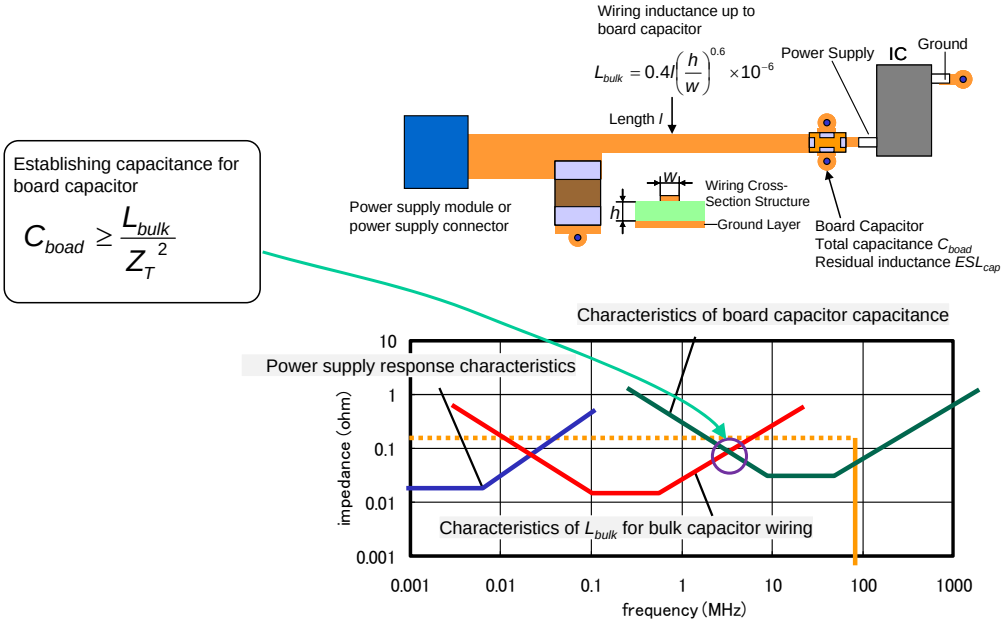


Figure 8-17 Establishing board capacitor capacitance

8.7.4 Positioning of the board capacitor

Next, the board capacitor will be positioned. By positioning the board capacitor so that the distance between the IC and the power supply terminal is within the maximum allowable wiring length l_{max} as described in Chapter 7, Z_T can be met at a frequency up to $f_{T@PCB}$ as shown in Figure 8-18.

$$l_{\max} \cong 0.4 \frac{Z_T - 2\pi f_{T@PCB} ESL_{cap}}{f_{T@PCB}\left(\frac{h}{w}\right)^{0.6}} \times 10^6 \quad \text{(m)} \tag{7-5}$$

In this equation, ESL_{cap} is the ESL of the board capacitor, and it includes inductance (ESL_{PCB}) from the capacitor mounting pad and via, in addition to ESL of the capacitor itself.

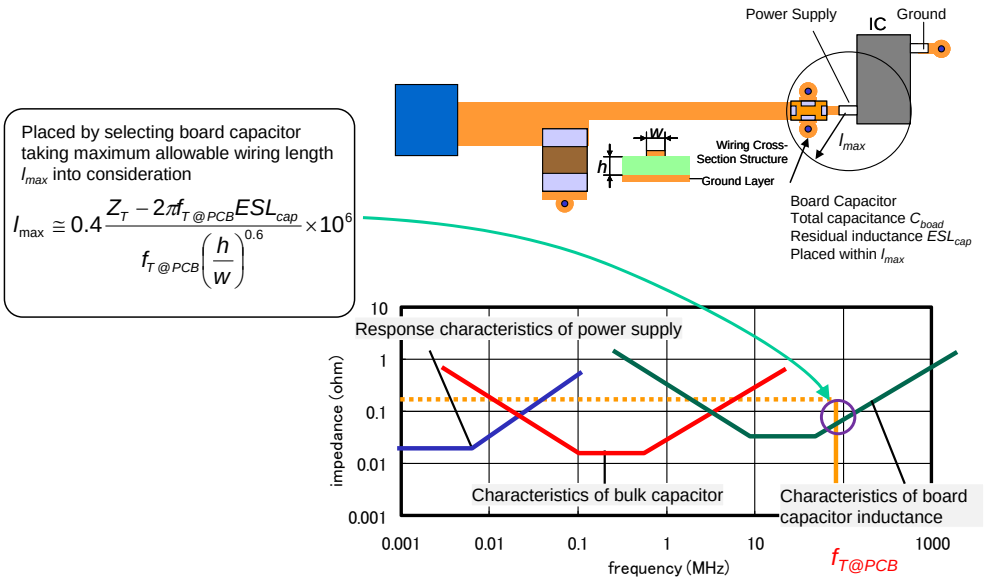


Figure 8-18 Placement of the board capacitor

8.7.5 Reducing ESL_{cap}

Depending on the target impedance, one capacitor does not achieve an appropriate length of l_{max} being unable to reach target impedance. In such a case, we need to position multiple capacitors in parallel as indicated in the diagram on the left of Figure 8-19, to reduce ESL_{cap} equivalently, and enlarge l_{max}. The use of a low-ESL capacitor as described in Chapter 4 is effective as well.

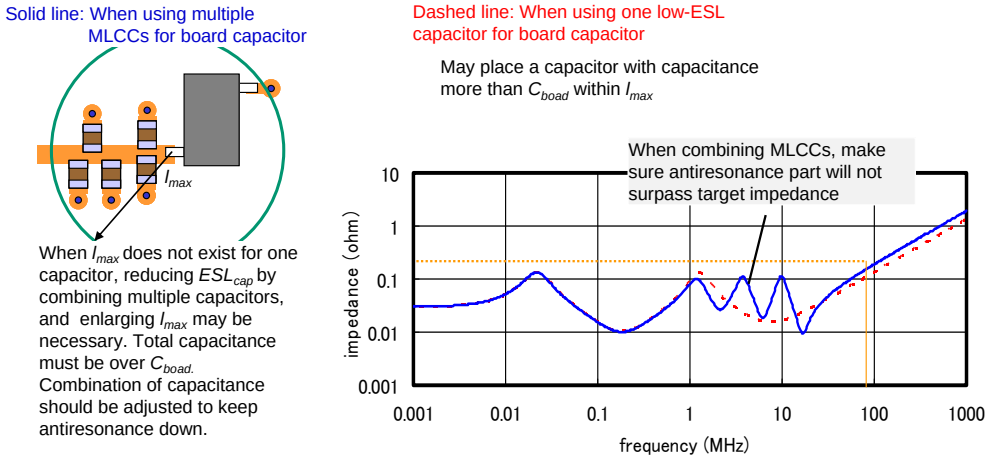


Figure 8-19 Reduction of ESL_{cap}

A summery of the procedures above is shown in Figure 8-20.

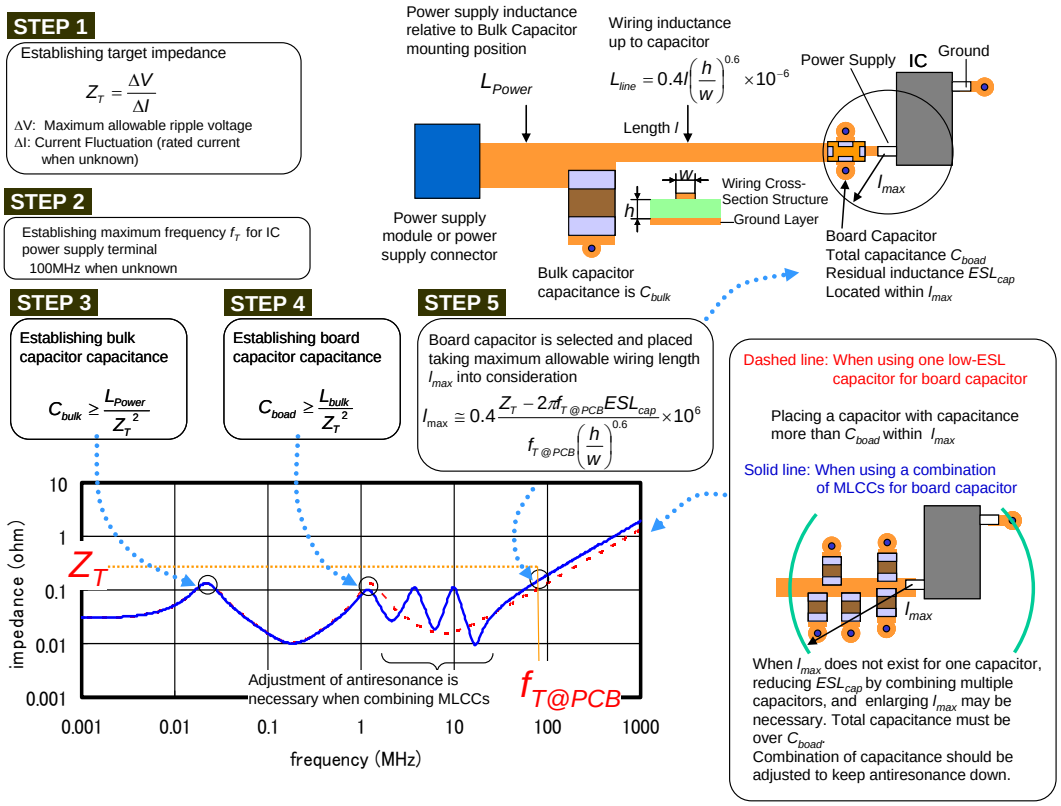


Figure8-20 An example of capacitor design to achieve target impedance

8.8 Making a PDN with ultra-low impedance

When low voltage, large current and high-speed response are required in a power supply simultaneously such as the core power supply for a large-scale CPU, we may need low impedance in the magnitude of mΩ. In such a case, it becomes necessary to combine multiple capacitors for each hierarchy to reach target impedance with the effect of parallel connections. Impedance design become complex in this case since the number of capacitors and power supply terminals increases greatly and the power supply wiring configuration will be complex too. The use of low-ESL capacitors introduced in Chapter 4 may make power supply design simpler and become advantageous in terms of space and cost from a reduced number of capacitors. Figure 8-21 shows an example of ultra-low impedance design with a combination of various capacitors.

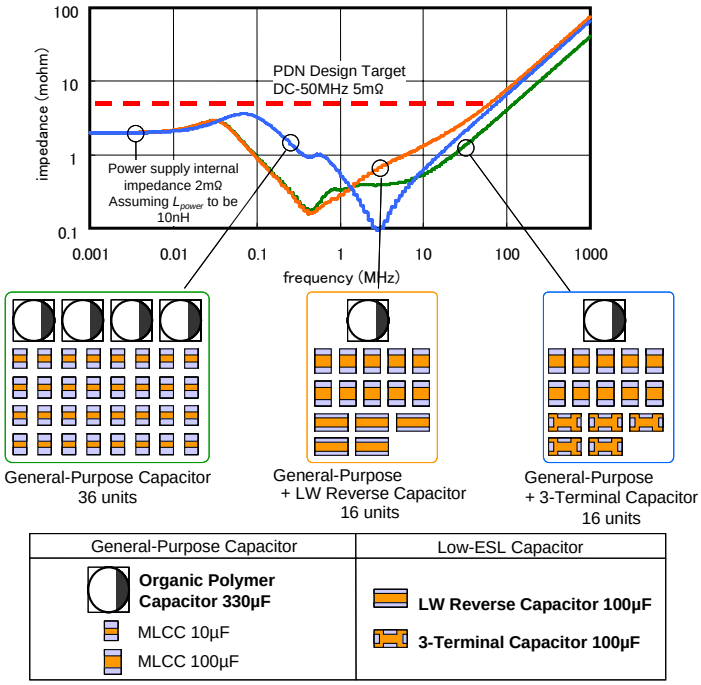


Figure 8-21 An example of ultra-low impedance design with a combination of capacitors

9. Summary

In this manual, we have described the configuration and mounting method of decoupling circuits used for power supplies for ICs. It is assumed that the use of this circuit is for suppressing noise and supplying enough current for IC operations (achieving PI: power integrity). Descriptions are made based on insertion loss from the viewpoint of noise suppression and impedance from the viewpoint of power integration as performance indicators for decoupling circuits.

Figure 1 shows various decoupling circuits being compared from the viewpoints of noise suppression and power integrity. For IC power supplies, MLCCs are used as a method of achieving both of these features simply. When replacing this with 3-terminal capacitors or low-ESL capacitors, performance improvement can be expected for both noise suppression and power integrity. Furthermore, when inductors such as ferrite beads are added, performance can be improved from the viewpoint of noise suppression; however, an increase in power supply impedance may occur in some cases. In such a case, capacitors must be reinforced. An increased number of stages for combinations of capacitors and inductance can further attenuate the noise. These filters should be applied in correspondence with levels required by circuits.

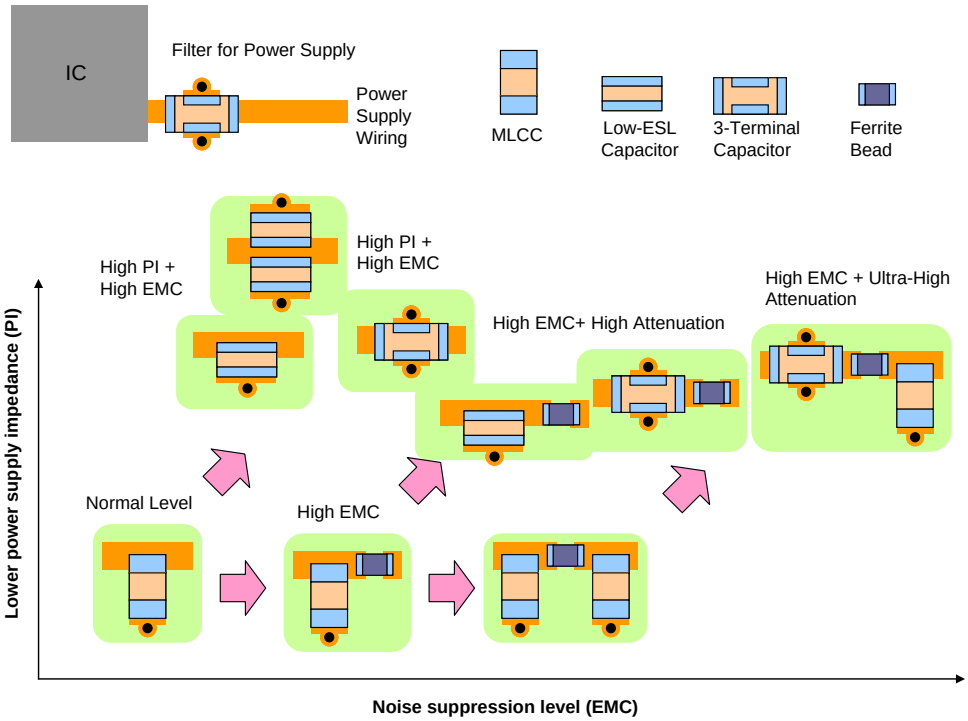


Figure 1 Structure of power supply filters

Characteristics of power supply circuits from the viewpoint of noise countermeasures include wiring configuration being complex compared with signal circuits, making it difficult to design characteristic impedance; extremely low impedance in some cases; a wide range of frequency range for noise countermeasure applications from voice band to GHz; and having a wide sphere of influence due to being shared by many circuits. In order for a bypass capacitor to function effectively in such circuits, mounting structure and

wiring design creating small inductance are necessary for low impedance under high frequency. To this end, this manual describes the wiring configuration for mounting capacitors as far as possible. We hope you can utilize this information when designing electronic equipment.

References

1) Hidetoshi Yamamoto, “Pawainteguritei no tame no kondensa no tekiyou (Application of Decoupling Capacitors for Power Integrity Improvement),” Journal of Japan Institute of Electronics Packaging, vol. 12 No.3, May 2009
2) Hidetoshi Yamamoto, “Mobairukiki no dengen noizutaisaku (zenpen) (Power Supply Noise Countermeasure for Mobile Equipment Part 1/2)” pp. 117-129, Electro Magnetic Compatibility (EMC), September 2007, No. 233
3) Mark I. Montrose, “EMC and the Printed Circuit Board - Design, Theory and Layout Made Simple,” Wiley-IEEE Press, 1998
4) Brian Young, “Digital Signal Integrity Modeling and Simulation with Interconnects and Packages,” Prentice Hall PTR, 2001
5) Clayton R. Paul, “Introduction to Electromagnetic Compatibility,” Wiley-Interscience, 1992
6) Tadashi Kubodera, “Kousoku dejitarukairo jissou nouhau (High-Speed Digital Circuit Mounting Know-How),” CQ Publishing Co., Ltd., 2002
7) “Dejitarukairo ni okeru DCdengenrain no noizutaisaku (Noise Countermeasure for DC Power Supply Line in Digital Circuits),” Murata Manufacturing Technical Material, TE13JT, 1996
8) Yukio Sakamoto, “Yokuwakaru dengenrain no EMC/noizutaisaku sekkei (Power Supply Line EMC/Noise Countermeasure Design Made Simple),” Nikkan Kogyo Shimbun Ltd., 2006
9) “Noise Suppression by EMIFIL® Basics of EMI Filters,” Murata Manufacturing Technical Material, 1986
10) Larry D. Smith, “Frequency Domain Target Impedance Method for Bypass Capacitor Selection for Power Distribution Systems,” pp.119-136, Power Distribution Network Design Methodologies, IEC, 2008
11) Yukio Sakamoto, “Zukai Noizutaisakubuhin to EMC sekkei (EMI Suppression Components and EMC Design Illustrated),” Kogyo Chosakai Publishing Co., Ltd., 2005
12) Seiji Sakai, “Chip Ferrite Beads,” pp. 52-57, Electro Magnetic Compatibility (EMC), November 2007, No. 235
13) Tetsuo Ikeda, “Denki riron dai 2 han (Theory of Electricity 2nd Edition),” Morikita Publishing Co., Ltd., 2006
14) Stephan H. Hall, Garret W. Hall, James A. McCall, “High-speed Digital System Design; A Handbook of Interconnect Theory and Design Practices,” Wiley-Inter Science 2000
15) Mikhail Popovich, Andrey V. Mezhiba, Eby G. Friedman, “Power Distribution Networks with On-chip Decoupling Capacitors,” Springer, 2008
16) Madhavan Swaminathan, A. Ege Engin, “Power Integrity Modeling and Design for Semiconductor and Systems,” Prentice Hall PTR, 2008

17) Takahiro Yaguchi, “Purintohaisenban no pawainteguritei sekkei (Power Integrity Design of PCB),” Journal of Japan Institute of Electronics Packaging, vol. 12 No. 3, May 2009

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