

CMRR

TIPL 1231

TI Precision Labs – Op Amps

Presented by Collin Wells

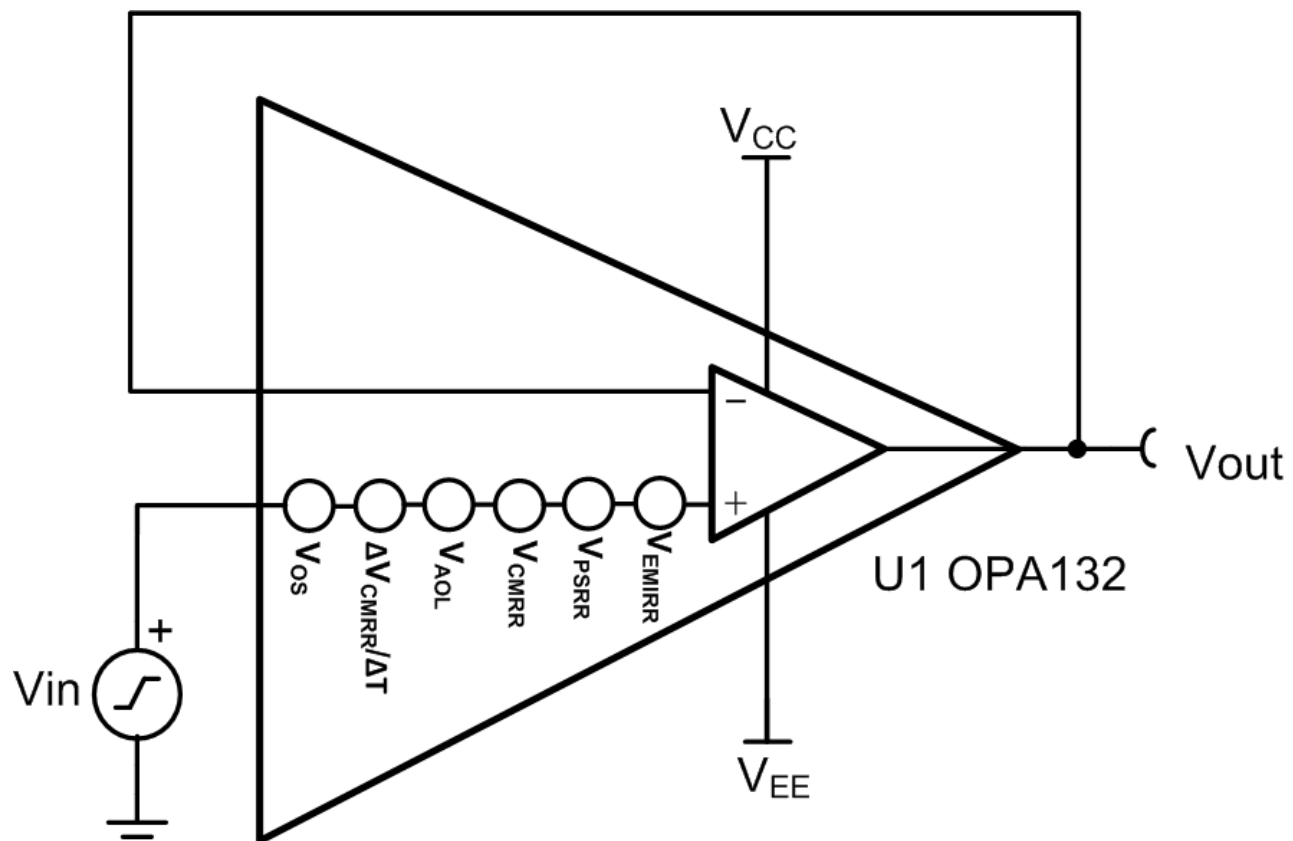
Prepared by Collin Wells, Art Kay, Ian Williams, and Tim Green

Prerequisites: Op Amp Bandwidth 1 – 3
(TIPL1221 – TIPL1223)



Hello, and welcome the TI Precision Labs video on common mode rejection. This video will discuss how changing the common mode voltage on op amps introduces a common mode rejection error. We will consider both ac and dc common mode rejection. Finally, we will consider how changing the input voltage can also introduce open loop gain errors, and methods for separating the common mode and open loop gain errors.

Referring Error to Input (RTI)



Common mode rejection errors, power supply rejection errors, open loop gain errors, and many other types of errors can be modeled as an input offset voltage connected to the non-inverting input of the op amp. This method of reflecting the error signal to the input simplifies the error analysis as the error sources can be added to find the total error. In practice, the error sources are often added as the square root sum of the squares because the error sources are uncorrelated and can be represented with Gaussian distributions.

CMRR and A_{OL} Combined

	Typical	Unit
A_{OL}	136	dB
CMRR	134	dB

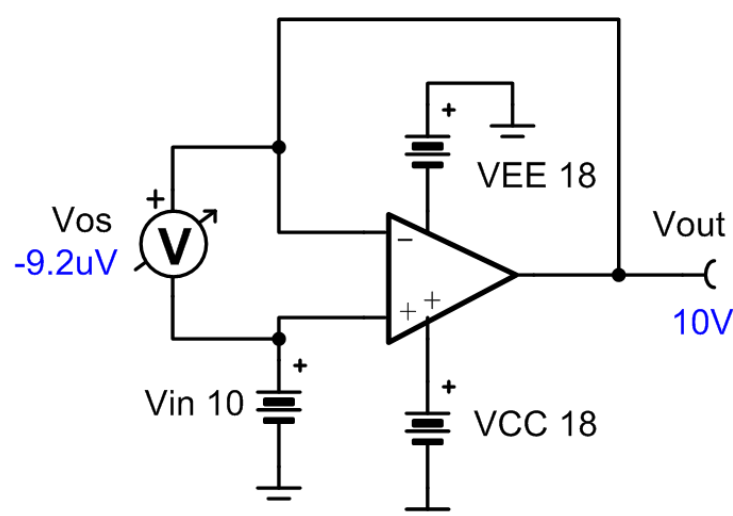
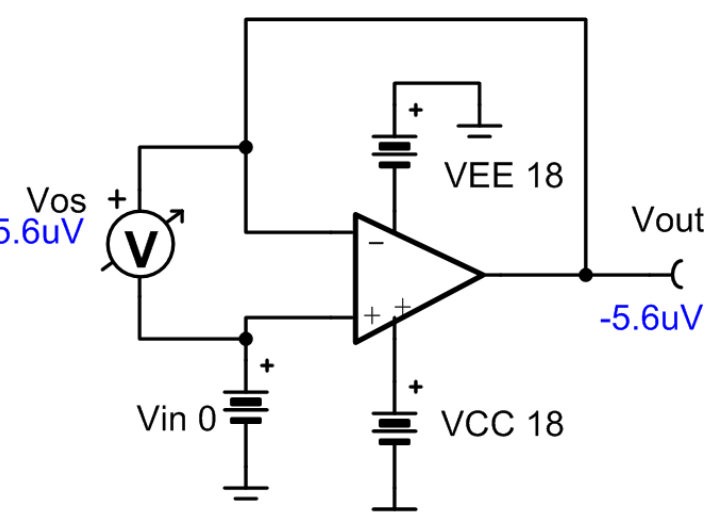
Combined Effects of A_{OL} and CMRR

$$V_{OS_{AOL}} = \frac{\Delta V_{OUT}}{A_{OL}} = \frac{10V}{10^{\frac{136}{20}}} = 1.6\mu V$$

$$V_{OS_{CMRR}} = \frac{\Delta V_{OUT}}{CMRR} = \frac{10V}{10^{\frac{134}{20}}} = 2\mu V$$

$$\Delta V_{OS_{Total}} = V_{OS_{AOL}} + V_{OS_{CMRR}} = 3.6\mu V$$

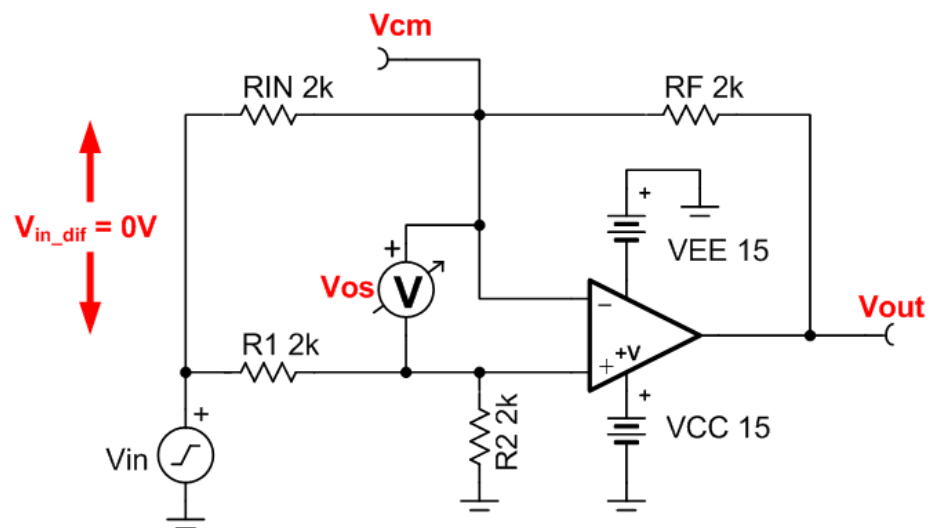
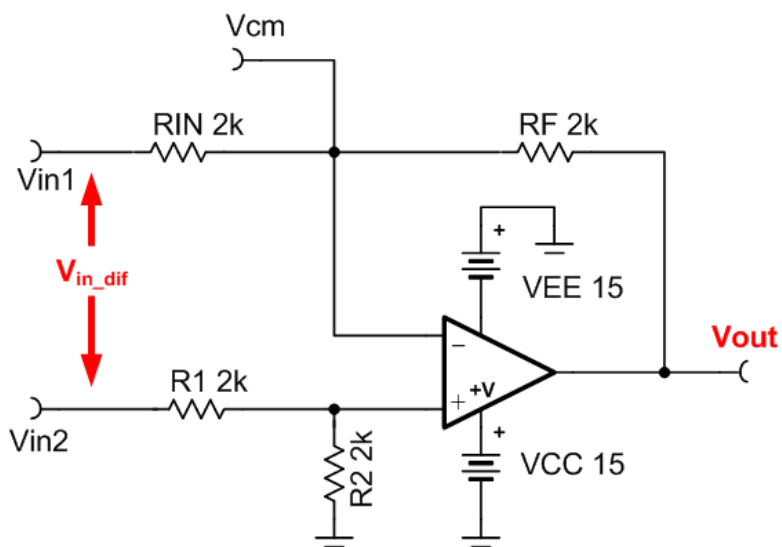
$$\Delta V_{OS_{Sim}} = V_{OS_{10V}} - V_{OS_{0V}} = 3.6\mu V$$



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This slide emphasizes how common-mode rejection ratio, CMRR, and A_{OL} errors are often combined in many common configurations. In this example the input voltage on a simple buffer is shifted from 0V to 10V. Therefore, the common mode voltage as well as the output voltage shifts from 0V to 10V. The shift in the output voltage introduces an error reflected to the input from open loop gain, or A_{OL} . For this example, dividing the output voltage change of 10V by the open loop gain yields an offset shift of 1.6uV. Performing a similar calculation for CMRR yields 2uV of offset shift. Directly adding the two errors yields 3.6uV of total error. Notice that the simulated and calculated results match well.

Introducing the Dif Amp for testing CMRR



Gain of a Dif-Amp

$$R_f = R_2 \text{ and } R_{in} = R_1$$

$$G_{dif} = \frac{R_F}{R_{IN}} = 1 \text{ V/V}$$

$$V_{out} = G_{dif} \cdot V_{in_dif}$$

CMRR of a Dif-Amp

$$V_{out} = (0V) \cdot (1 \text{ V/V}) = 0V$$

$$V_{cm} = V_{in} \cdot \left(\frac{R_2}{R_1 + R_2} \right) = \frac{V_{in}}{2}$$

$$CMRR(V/V) = \frac{\Delta V_{os}}{\Delta V_{cm}}$$

Ideal output.

Common Mode Voltage

Common Mode Rejection

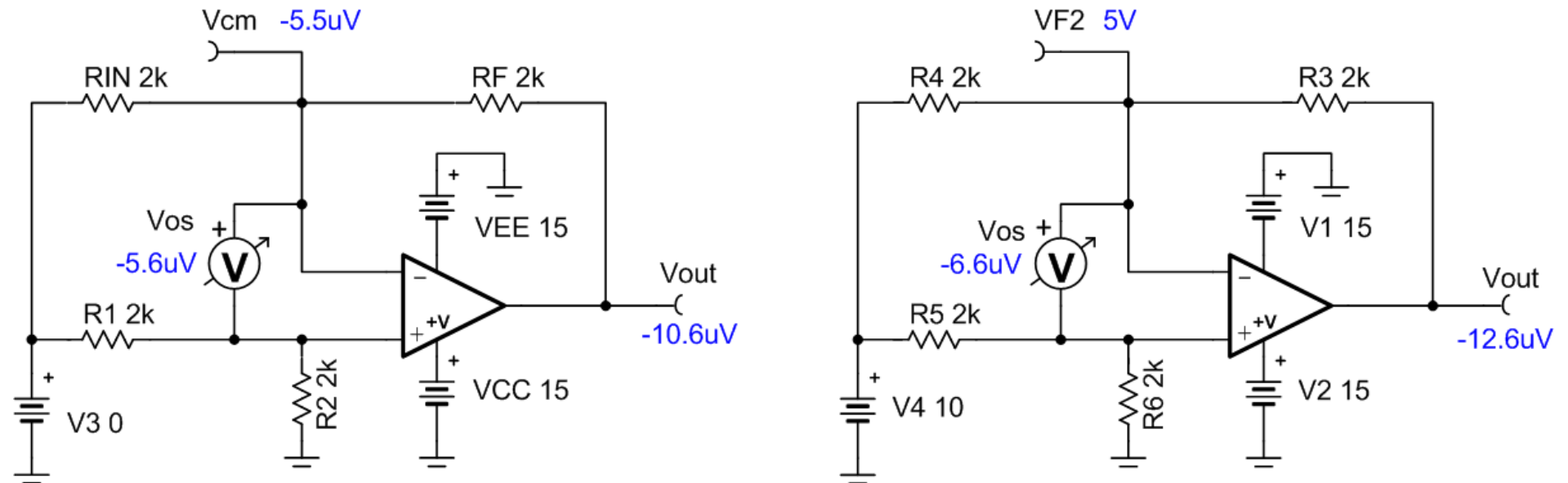
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A specialized circuit is needed to separate the effects of CMRR and A_{OL} from each other. The Difference amplifier, commonly called a "Diff Amp", is one approach to isolating the effects of CMRR. Before looking at how it is used to measure CMRR, let's just look at how the Diff Amp works. The typical Diff Amp configuration shown on the left takes the differential input voltage and multiplies it by a gain. Assuming $R_f = R_2$ and $R_{in} = R_1$ the gain is calculated by dividing R_f by R_{in} . In the example shown on the left, the gain is 1V/V, and the output is the differential input voltage multiplied by the gain.

In the second diagram the differential inputs are shorted together such that the differential input voltage is always 0V. The input source, V_{in} , does not generate any differential input voltage, so the ideal output is 0V. As the input signal changes, so does the common mode voltage of the op amp. In this example, the common mode voltage is equal to the input source divided by 2. Using this circuit, the common mode rejection can be calculated as the change in offset divided by the change in common mode voltage. Note that the effects from A_{OL} are eliminated because the differential input and output are held constant at zero volts.

DC CMRR Test



CMRR of a Dif-Amp

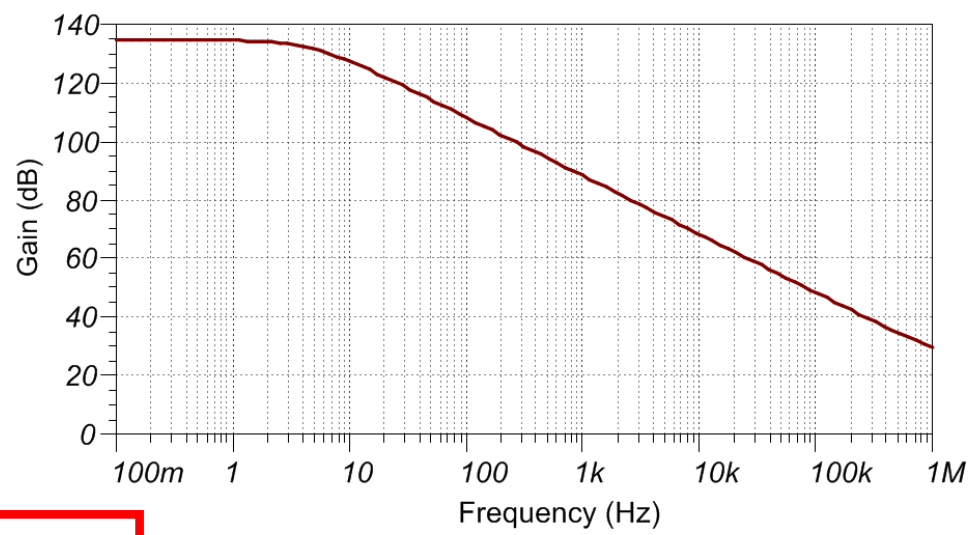
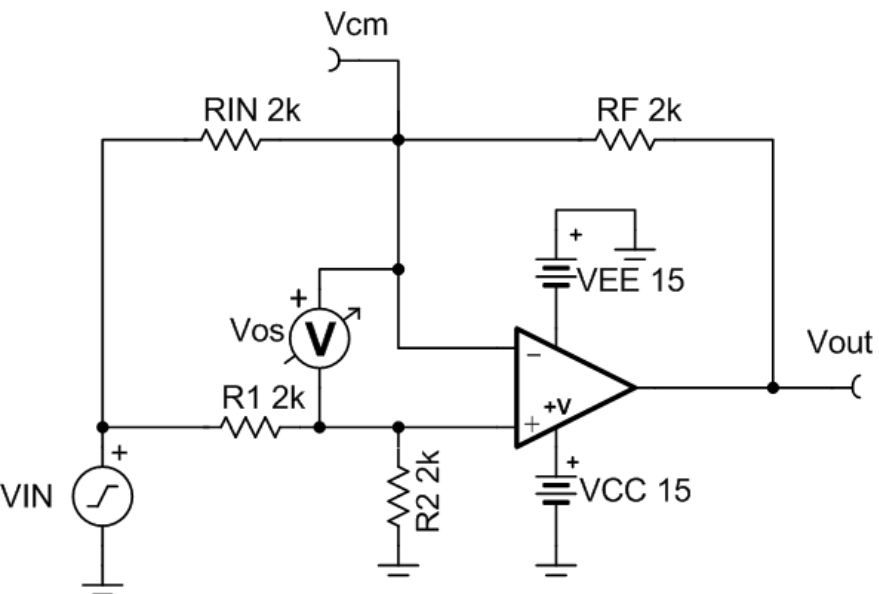
$$\text{CMRR(V/V)} = \frac{\Delta V_{os}}{\Delta V_{cm}} = \frac{|-6.6\mu\text{V} - (-5.6\mu\text{V})|}{|5\text{V} - 0\text{V}|} = 0.2 \cdot 10^{-6} \text{ V/V}$$

$$\text{CMRR(dB)} = -20 \cdot \log[\text{CMRR(V/V)}] = 134\text{dB}$$

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This slide shows a simulation of the dc CMRR test circuit. The input signal ranges from 0V to 10V which translates to a 0V to 5V common mode signal. The common mode rejection is calculated as the change in offset over the change in common mode. For this example CMRR is 0.2μV/V or 134dB. Again, note that the effects of Aol are eliminated because the output is kept nearly constant at 0V.

AC CMRR Test



CMRR of a Dif-Amp

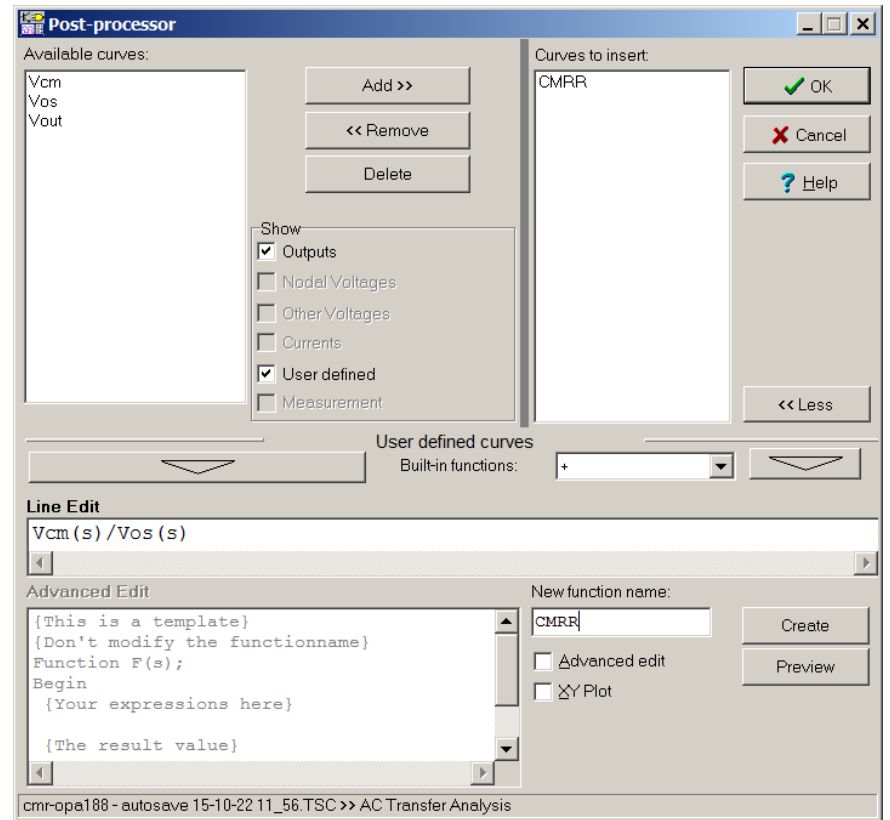
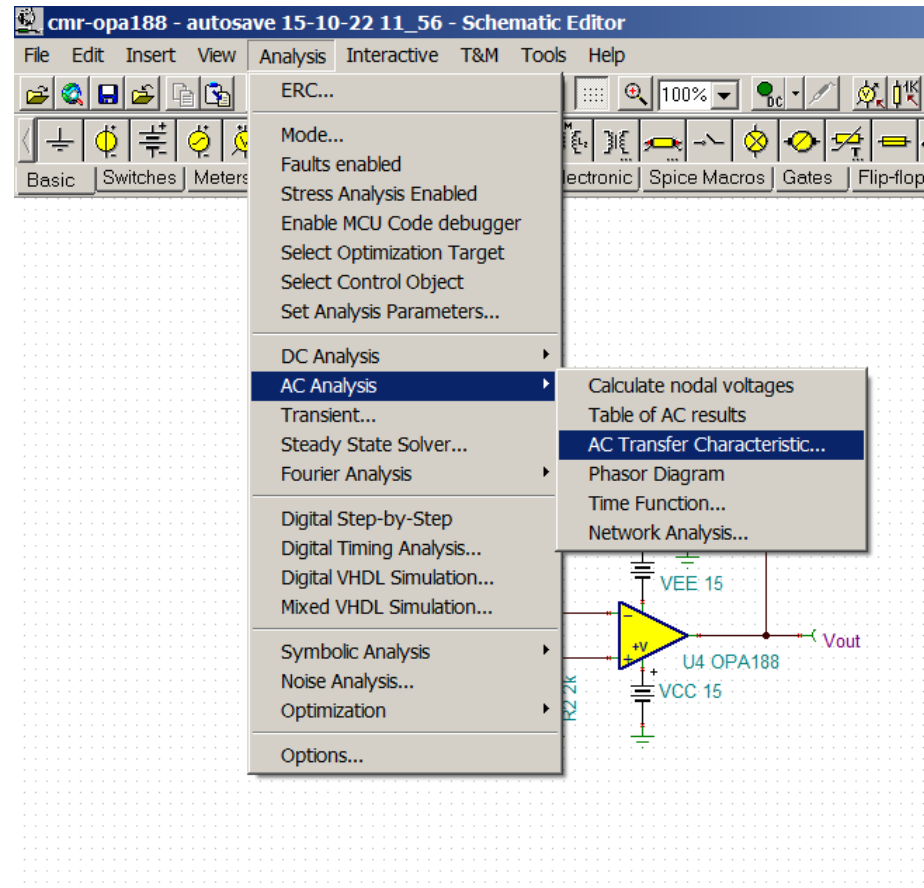
$$\text{CMRR(V/V)} = \frac{\Delta V_{os}}{\Delta V_{cm}}$$

$$\text{CMRR(dB)} = -20 \cdot \log[\text{CMRR(V/V)}]$$

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AC common mode rejection is simulated using the same test circuit that was used for dc CMRR. To get the best results make sure that test conditions such as load resistance are observed. Also, a post processor tool will be needed to generate the curve using the standard CMRR equations.

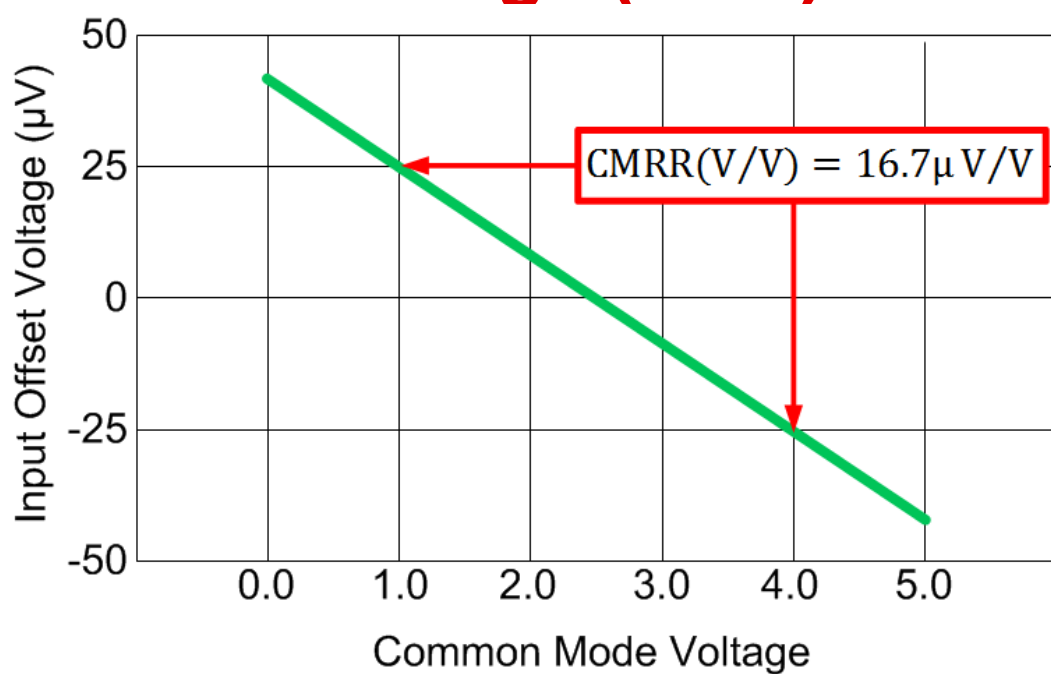
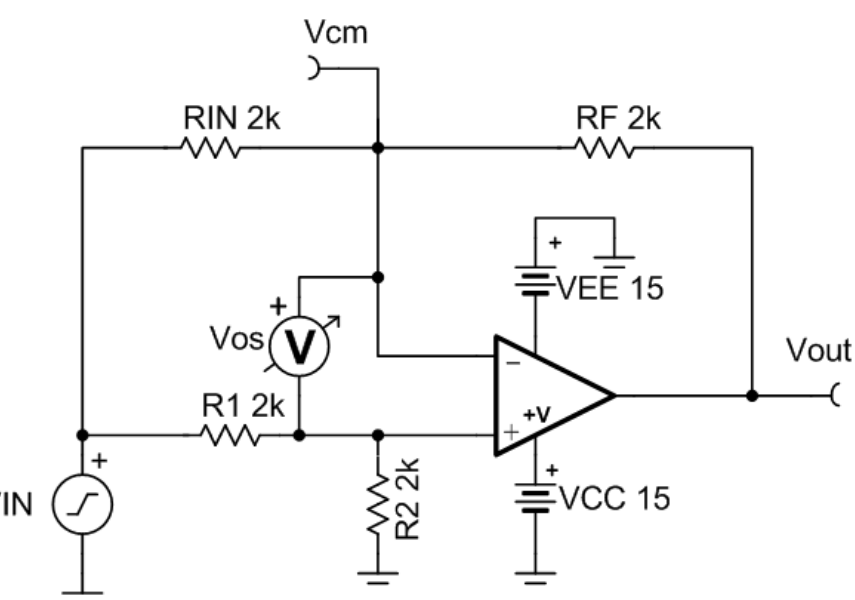
Post Processor – Generating the Curve in Tina



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This slide shows the Tina Spice post processor tool. This tool can be used with any analysis that generates curves such as transient, dc sweep, or ac analysis. In this case we use the post processor to perform math on the ac transfer characteristic to generate the ac CMRR curve. To use this tool, first select the appropriate curve from the “available curves”. Next use the line editor to apply the math function. Finally enter the function name, CMRR in this case, and press create. Although the specific procedure here is for TINA spice, other simulators will have a similar tool.

Offset (V_{os}) vs. Common Mode Voltage (V_{cm})



$$CMRR(V/V) = \frac{\Delta V_{os}}{\Delta V_{cm}} = \frac{|25\mu V - (-25\mu V)|}{|1V - 4V|} = 16.7 \cdot 10^{-6} V/V$$

$$CMRR(dB) = -20 \cdot \log[CMRR(V/V)] = 96dB$$

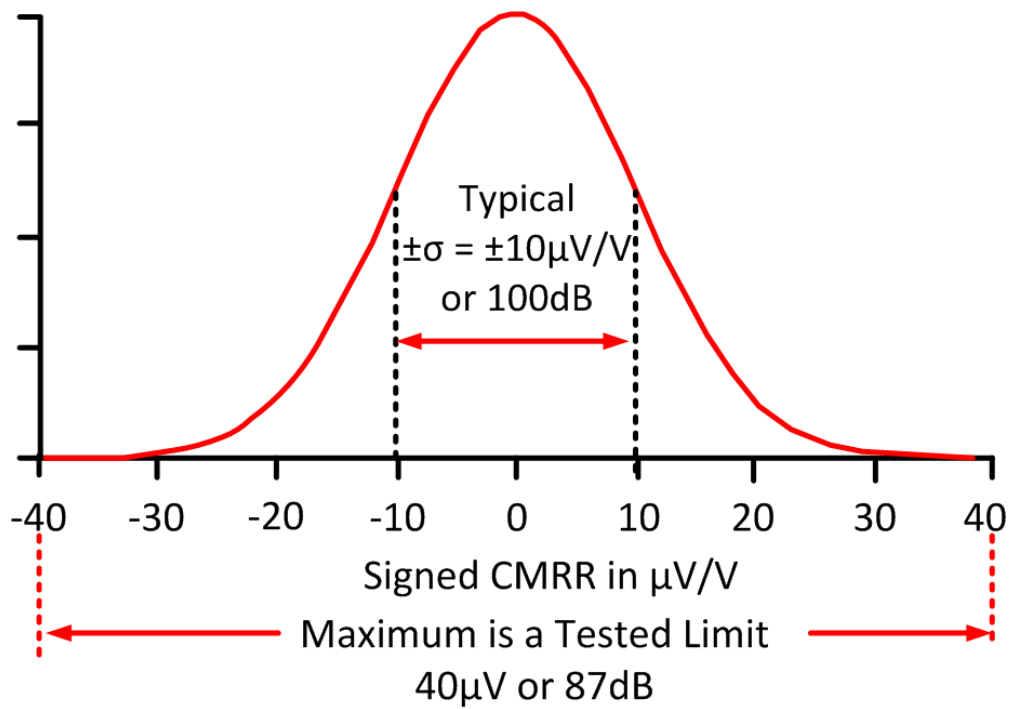
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Graphing the input offset voltage versus the common mode voltage for an op amp will generally produce a linear function as shown in this graph. Of course, there are some exceptions, and we will look at one soon. Notice that the slope of the straight line is equal to the common mode rejection of the device. The slope of this line can be either positive or negative indicating that the common mode rejection can cause the input offset voltage to shift in either direction. Note, however, that the absolute value is applied to the CMRR function so that CMRR is always positive regardless of the direction of the input offset voltage change.

Distribution of CMRR

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Common-Mode Rejection	$V_{CM} = -12.5V$ to $12.5V$	87	100		dB

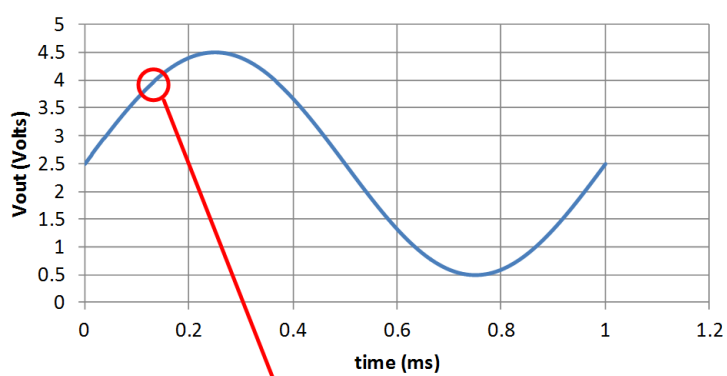


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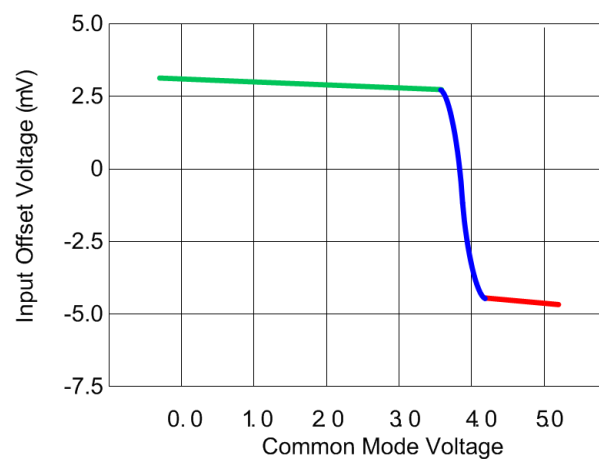
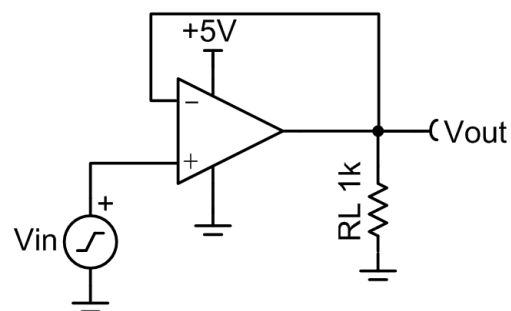
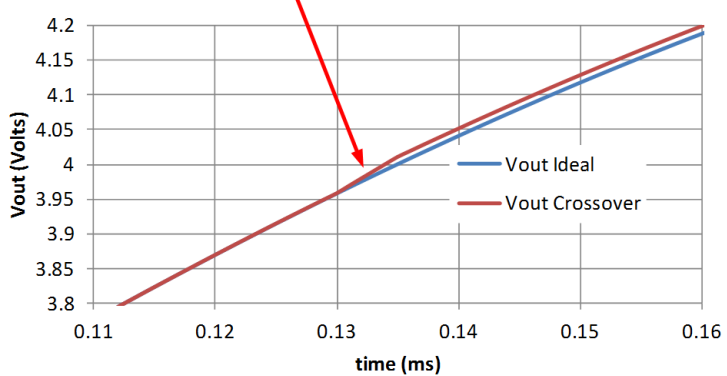
Common mode rejection relates to how well the Early voltage of the input transistors match. It's possible for the V_{os} vs Common Mode Voltage to have a positive, or negative slope. In fact, if you were to look at a distribution of common mode rejection, you would get a Gaussian distribution. The typical value of the CMRR specification is set to the mean plus one standard deviation. In the example shown the mean CMRR is zero and one standard deviation is $10\mu V/V$, so the typical CMRR is $10\mu V/V$ or 100dB. When the data sheet table provides a minimum value for CMRR, this means that CMRR is tested and that any device with CMRR worse than the minimum level is considered a failure and discarded. So for this example amplifier, any device with CMRR less than 87dB is discarded. Of course, the minimum value of CMRR also corresponds to the tails of the distribution which in this case are at $\pm 40\mu V/V$ or 87dB. Again notice that the sign of the CMRR in volts per volt can be either positive or negative, but that the sign of decibels will always be positive.

Crossover Distortion Caused by CMRR

Vout vs. Time (Crossover Distortion)



Zoom in on Crossover Distortion

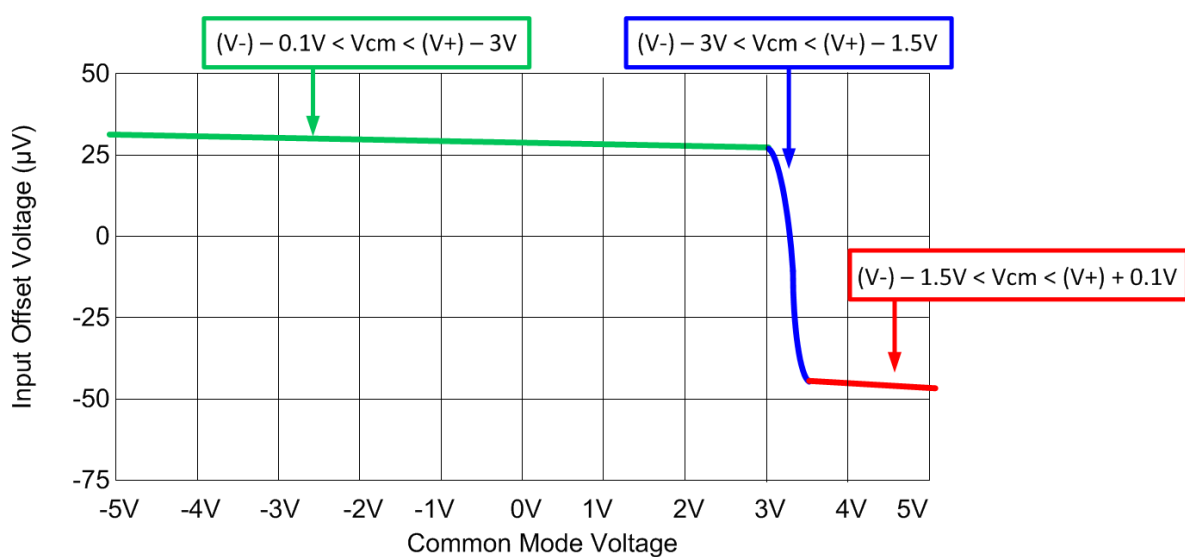
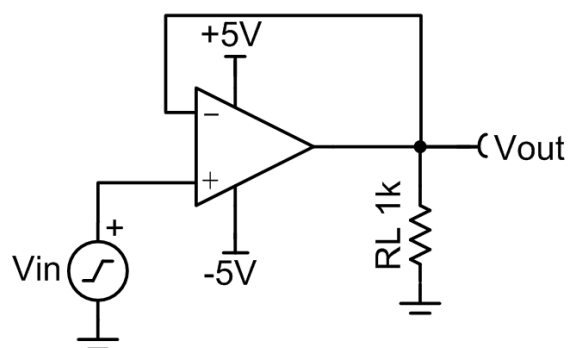


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Rail to rail amplifiers use two different internal input stages to achieve input range from the negative supply to the positive supply. The problem with most rail to rail amplifiers is that they will have a jump in the offset voltage when the common mode voltage reaches the point where we transition between two input stages. This generates a type of distortion called input crossover distortion. Since common mode rejection is determined by looking at the change in offset voltage over common mode voltage, this jump in offset will also affect CMRR. For this reason, CMRR specifications are often separated into different common-mode voltage ranges to show the performance of each region.

CMRR for Amplifiers with Crossover Distortion

PARAMETER	TEST CONDITIONS	OPA192			UNIT
		MIN	TYP	MAX	
CMRR Common-mode rejection ratio	$(V-) - 0.1\text{ V} < V_{CM} < (V+) - 3\text{ V}$	120	140		dB
	$(V+) - 3\text{ V} < V_{CM} < (V+) - 1.5\text{ V}$	See Typical Characteristics			
	$(V+) - 1.5\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	100	120		dB

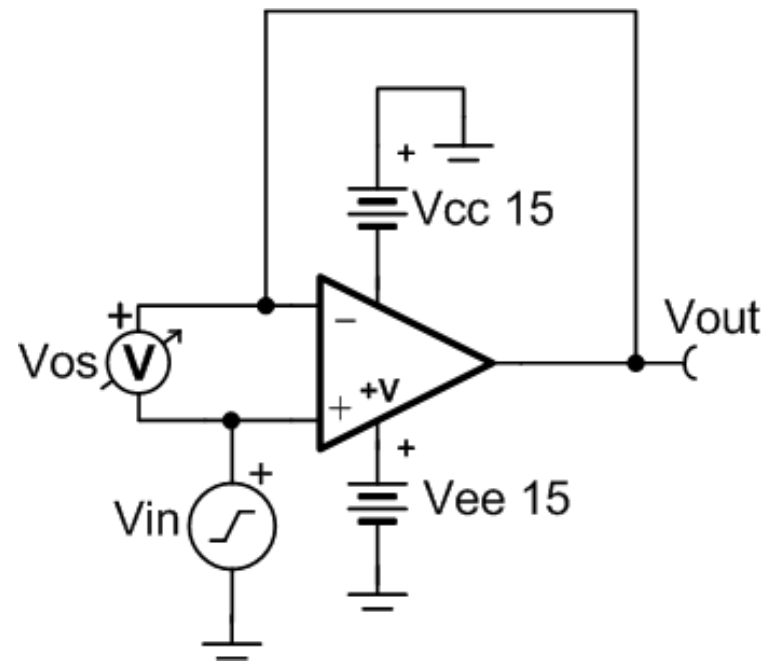
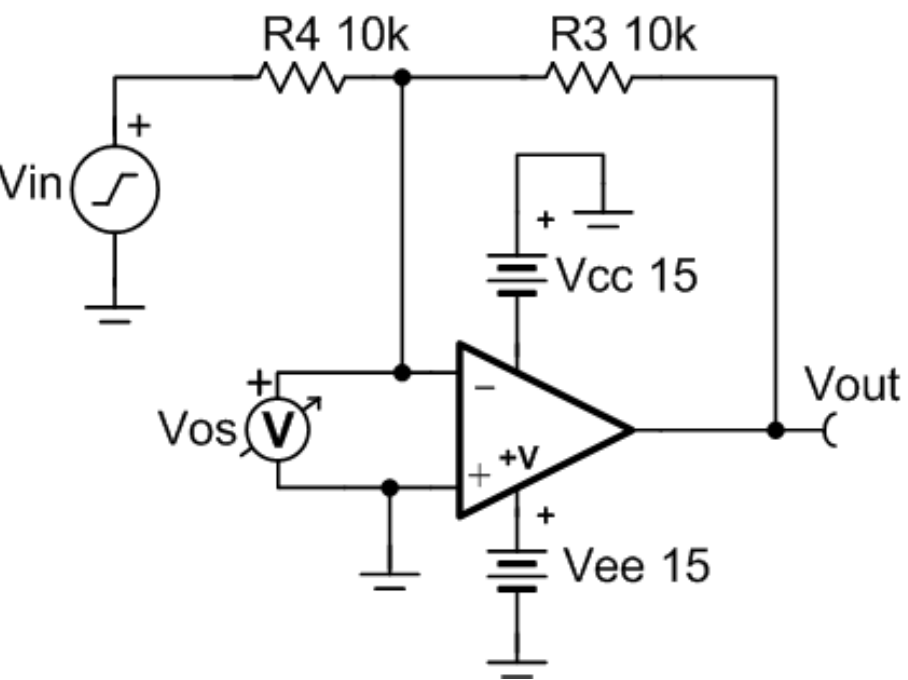


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Here you can see the CMRR specification is broken into three regions corresponding to the three separate regions of operation. In the green region the PMOS input pair is operating and the common mode rejection in that region is typically 140dB. The blue region is where the device transitions from the PMOS input pair to the NMOS input pair. In this region the CMRR is poor and unpredictable, so the data sheet directs you towards characteristic curves similar to the Vos vs Vcm plot given here. In the red region the NMOS input pair is operating and the common mode rejection in that region is typically 120dB.

Inverting vs. Non-inverting (Impact on CMRR)



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An easy way to avoid common-mode voltage errors is to use the inverting op amp topology instead of the non-inverting topology. In the non-inverting configuration the op amp common-mode voltage varies with the input voltage. In the inverting configuration the common-mode voltage of the op amp is held at the constant dc voltage applied to the non-inverting input of the amplifier. Therefore, with a constant common-mode voltage the inverting topology avoids common-mode errors as the input voltage changes.

Thanks for your time! Please try the quiz.

This video discussed common-mode rejection and how changing the common mode voltage on op amps introduces a common mode error. We discussed how to isolate common-mode errors from open-loop gain errors and how to properly simulate common-mode rejection ratio.

Thank you for time! Please try the quiz to check your understanding of this video's content.