

PCN Number:	20260706000.1	PCN Issued	July 07, 2026
Qualification of RFAB as an additional Fab site option, Die Revision, Datasheet and MLA as an additional Assembly site options for select devices		Sample request deadline:	September 05, 2026
		Estimated 1st ship date:	October 05, 2026
September 05, 2026* will not be supported.			

Change type(s)
Assembly Site Assembly Process Assembly Material Packing/Shipping/Labeling Design Data Sheet/Electrical Specification Wafer Fab Site Wafer Fab Material Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of RFAB as an additional Fab site option & MLA as additional Assembly site options for the devices listed below.

Current Fab Site			Additional Fab site		
Current Fab Site	Process	Wafer Diameter	Additional Fab site	Process	Wafer Diameter
MAINEFAB	VIP050	200mm	RFAB	HPA9	300mm

The die was also changed as a result of the process change.

Construction differences are as follows:

	Current Site	Additional Site
Assembly/Test site	TIEM	MLA
Wire bond diam/type	0.9mil Au	0.8mil Cu
Mount compound	8075531	4147858
Mold compound	8096859	4211880
Lead finish	Matte Sn	NiPdAu
Marking appearance (pin 1 ID)	Embossed	Dot

Data sheet update

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.



LMP8601, LMP8602, LMP8603

SLVSJ15 – JUNE 2026

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release. of this data sheet Commercial device split from Automotive data sheet (SNOSAR2).

The LMP860x device is moved from [SNOSAR2](#) "I" revision data sheet to the current standalone datasheet. The changes from the SNOSAR2 "I" revision to this document are as follows:

- Updated the numbering format for tables, figures, and cross-references throughout the document.
- Deleted ESD Classification from the [Features](#) section.
- Updated applications with links in [Applications](#) section.
- Added Abs Max differential input voltage specification in [Absolute Maximum Ratings](#) table.
- Deleted Machine Model ESD rating from [ESD Ratings](#) table.
- Updated Thermal Information for D (SOIC) package in [Thermal Information](#) table.
- Changed common-mode input impedance for SOIC (D) package in [Electrical Characteristics: \$V_s = 3.3V\$](#) table.
- Changed differential-mode input impedance for SOIC (D) package in [Electrical Characteristics: \$V_s = 3.3V\$](#) table.
- Changed typical input bias current specification in [Electrical Characteristics: \$V_s = 3.3V\$](#) table.
- Changed common-mode input impedance for SOIC (D) package in [Electrical Characteristics: \$V_s = 5V\$](#) table.
- Changed differential-mode input impedance for SOIC (D) package in [Electrical Characteristics: \$V_s = 5V\$](#) table.
- Changed typical input bias current specification in [Electrical Characteristics: \$V_s = 5V\$](#) table.
- Changed Input Bias Current Over Temperature (A2 pin) at $V_s = 5V$ curve in [Typical Characteristics](#).
- Added V_{os} Distribution at $V_s = 3.3V$ and $V_s = 5V$ plots for SOIC (D) package in [Typical Characteristics](#).
- Added V_{os} drift vs Temperature plots for SOIC (D) package in [Typical Characteristics](#).
- Added Gain Error Distribution plots for SOIC (D) package in [Typical Characteristics](#).
- Added Gain drift vs Temperature plots for SOIC (D) package in [Typical Characteristics](#).
- Added CMMR Distribution plots for SOIC (D) package in [Typical Characteristics](#).
- Added CMRR drift vs Temperature plots for SOIC (D) package in [Typical Characteristics](#).
- Added the [Related Documentation](#) section.

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
LMP8601, LMP8602, LMP8603	SNOSAR2I	SLVSJ15	LMP860x, -22V to 60V, Bidirectional Current Sense Amplifier With In-Line Filter Capability datasheet

Qual details are provided in the Qual Data Section.

Test coverage, insertions, conditions will remain consistent with current testing.

Reason for Change:

Supply Continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability:

These devices include new die based on existing schematics in a larger diameter wafer fab with a die shrink. There are changes in the electrical tables. Physical aspects of the device have changed. Review updated datasheets and/or the Standard Data Packet for more details on the changes. Evaluating samples is encouraged.

Impact on Environmental

Checked boxes indicate the status of

Ratings	environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.										
	<table border="1"> <tr> <th>RoHS</th> <th>REACH</th> <th>Green Status</th> <th>IEC 62474</th> </tr> <tr> <td>☒ No Change</td> <td>☒ No Change</td> <td>☒ No Change</td> <td>☒ No Change</td> </tr> </table>	RoHS	REACH	Green Status	IEC 62474	☒ No Change	☒ No Change	☒ No Change	☒ No Change		
RoHS	REACH	Green Status	IEC 62474								
☒ No Change	☒ No Change	☒ No Change	☒ No Change								
Changes to product identification resulting from this PCN:	Fab Site Information										
	Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City							
	MAINEFAB	CUA	USA	South Portland							
	RFAB	RFB	USA	Richardson							
	Die Rev: Current New <table border="1"> <tr> <td>Die Rev [2P]</td> <td>Die Rev [2P]</td> </tr> <tr> <td>A</td> <td>A</td> </tr> </table>				Die Rev [2P]	Die Rev [2P]	A	A			
Die Rev [2P]	Die Rev [2P]										
A	A										
	Assembly Site Information										
	Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City							
	TIEM	CU6	MYS	Melaka							
	MLA	MLA	MYS	Kuala Lumpur							
	Sample product shipping label (not actual product label):										

Products Affected:			
LMP8601MAX/NOPB	LMP8602MAX/NOPB	LMP8603MAX/NOPB	

Qualification Report

Automotive Qualification Summary

(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 31-March-2026

Product Attributes

Attributes	Qual Device: LMP8603QMAX/NOPB	Qual Device: LMP8602QMAX/NOPB	Qual Device: LMP8601QMAX/NOPB	QBS Process Reference: IA223AQGSRQ1	QBS Package Reference: TLV984QDRQ1	QBS Package Reference: OPA4991QDRQ1	QBS Package Reference: TLC355QDRQ1	QBS Product Reference: TLC355QDRQ1	QBS Package Reference: OPA2991QDRQ1	QBS Product Reference: TLC355QDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain
Wafer Fab Supplier	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB	RFAB
Assembly Site	MLA	MLA	MLA	ASESHAT	MLA	MLA	FMX	MLA	FMX	FMX
Package Group	SOIC	SOIC	SOIC	VSOP	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	D	D	D	DGS	D	D	D	D	D	D
Pin Count	8	8	8	10	14	14	8	8	8	8

QBS: Qual By Similarity, also known as Generic Data
Qual Device LMP8603QMAX/NOPB is qualified at MSL1 260C
Qual Device LMP8602QMAX/NOPB is qualified at MSL1 260C
Qual Device LMP8601QMAX/NOPB is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SB / Lot	Test Name	Condition	Duration	Qual Device: LMP8603QMAX/NOPB	Qual Device: LMP8602QMAX/NOPB	Qual Device: LMP8601QMAX/NOPB	QBS Process Reference: IA223AQGSRQ1	QBS Package Reference: TLV984QDRQ1	QBS Package Reference: OPA4991QDRQ1	QBS Package Reference: TLC355QDRQ1	QBS Product Reference: TLC355QDRQ1	QBS Package Reference: OPA2991QDRQ1	QBS Product Reference: TLC355QDRQ1
Test Group A - Accelerated Environment Stress Tests																	
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	1/800	-	-	-	-	1/800	1/1320	1/800	3/8240	1/800
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	3/2310	3/2310	-	-	-	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/770	-	-	3/2310	3/2310	3/2310	1/770	1/770	3/2310	1/770
ACAHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	-	-	-	3/2310	-	-	-	-
ACAHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	1/770	-	-	3/2310	3/2310	-	1/770	1/770	3/2310	1/770
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/770	-	-	3/2310	3/2310	1/770	1/1090	1/770	3/2310	1/770
TC-BP	A4	ML-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/50	-	-	1/50	-	-	-	-	1/50	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	3/1350	-	1/500	1/450	3/1350	1/450
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	1/770	-	-	3/2310	-	1/450	-	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests																	
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	-	3/2310	3/2310	-	-	-	-	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	300 Hours	3/2310	-	-	-	-	-	-	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	-	3/24000	3/24000	-	-	-	-	-
EDR	B3	AEC Q100-005	1	77	NW Endurance, Data Retention, and Op Life	Per Q55-009-018	1 Step	3/2310	-	-	-	-	-	-	-	-	-
Test Group C - Package Assembly Integrity Tests																	
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/500	-	-	-	3/900	1/500	1/500	-	3/900	-
WBP	C2	ML-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/500	-	-	-	3/900	1/500	1/500	-	3/900	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	-	-	1/150	-	1/150	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/150	-	-	-	1/150	-	1/150	-	-	-
PD	C4	JEDEC JESD22-B100 and B109	3	10	Physical Dimensions	Cpk>1.67	-	1/100	-	-	-	3/300	-	1/100	-	3/300	-
Test Group D - Die Fabrication Reliability Tests																	
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDOB	D2	JESD95	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests																	
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/30	-	-	-	-	-	-	-	-	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	1000 Volts	1/30	-	-	-	-	-	-	-	-	-
LU	E4	AEC Q100-004	1	3	Latch-Up	Per AEC Q100-004	-	1/30	-	-	-	-	-	-	-	-	-
ED	E5	AEC Q100-009	3	30	Electrical Disturbances	Cpk>1.67 Room, Ind, and cold	-	1/1000	1/1000	1/1000	-	-	-	-	-	-	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual process samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>
TI Qualification ID: R-NPD-2405-032

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.