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1 MHz, Single-Supply, Photodiode Amplifier Reference Design



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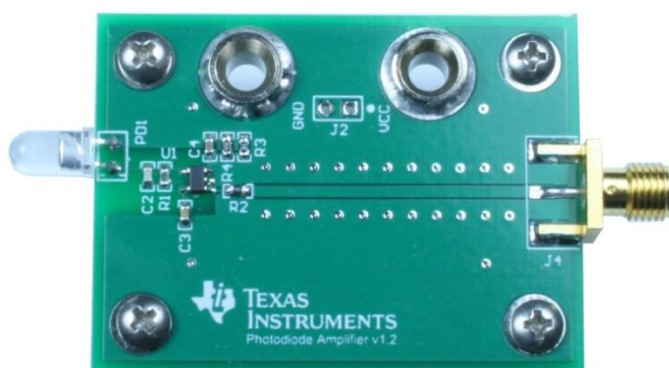
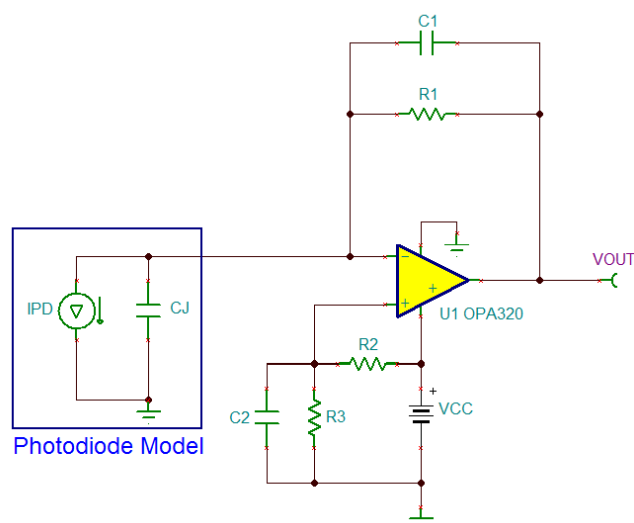
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Circuit Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode. A small bias voltage derived from the positive supply and applied to the op amp's non-inverting input. This prevents the output from saturating at the negative supply rail in the absence of input current.



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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5V
- Supply Current: <2mA
- Input current 0 - 90 μ A
- Output: 100mV – 4.9V

The design goals and performance are summarized in Table 1

Table 1. Comparison of Design Goals with Simulated and Measured Performance

	Goal	Simulated	Measured
Gain	53.6 kV / A (94.58dB)	53.6 kV / A (94.58dB)	53.48 kV / A (94.56dB)
Vout (0 μ A)	100 mV	100.096 mV	100.256mV
Vout (90 μ A)	4.9 V	4.924 V	4.913 V
-3dB Bandwidth	>1 MHz	1.464 MHz	1.59MHz
Phase Margin	>45 Degrees	68.59°	62.108°

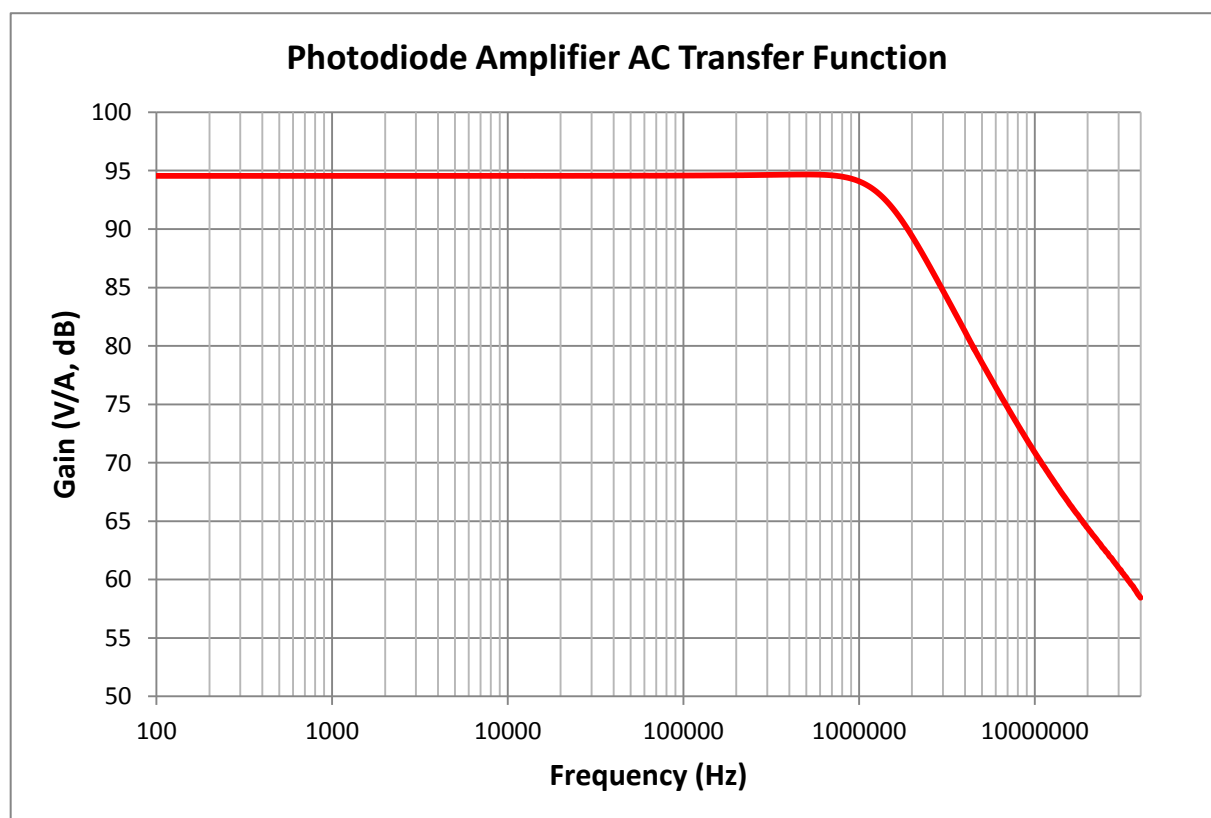


Figure 1: Measured Transfer Function

2 Theory of Operation

Transimpedance amplifiers are commonly used to amplify the light-dependant current of photodiodes. These circuits are deceptively simple; the proper design of a single supply photodiode amplifier requires the consideration of many factors including stability and input and output voltage range limitations. Furthermore, the effects of dc error sources such as input bias current and input offset voltage are often ignored and can degrade the transient response of these circuits. This design will examine the proper design process for photodiode amplifiers used in single supply applications.

In its most simple form, a transimpedance amplifier consists of an op amp and a feedback resistor. The current to be amplified is applied to the inverting input, causing the output voltage to change according to the equation:

$$V_{OUT} = -I_{IN} R_F \quad (1)$$

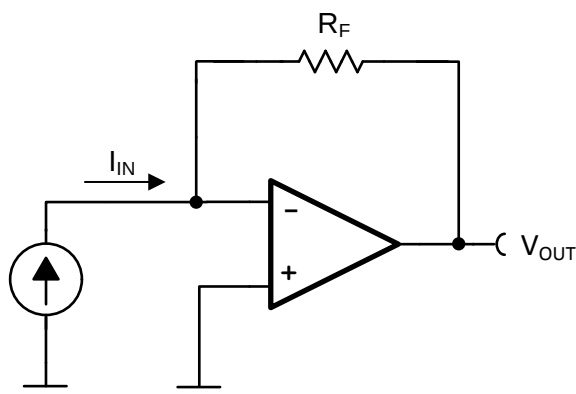


Figure 2: A basic op amp transimpedance amplifier

For this design, the photodiode will be operated in photoconductive mode: exposure to light will cause a reverse current through the photodiode. The diode is connected such that this current causes the op amp output voltage to increase.

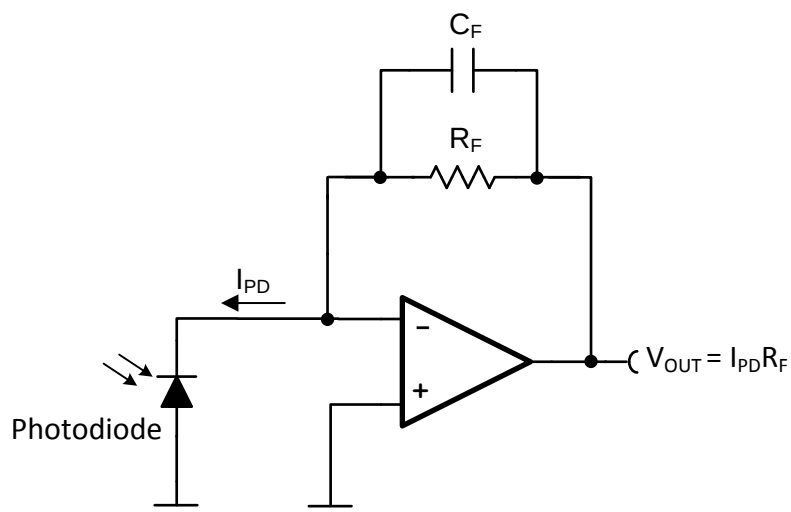


Figure 3: Connection of a photodiode to the transimpedance amplifier (photoconductive mode).

For most photodiode amplifiers, a feedback capacitor, C_F , is necessary to maintain stability. This capacitor compensates for the photodiode capacitance at the inverting input of the op amp.

Finally, in the absence of any photodiode current, the amplifier output will attempt to settle at the voltage applied to the non-inverting input. If the non-inverting input is grounded, the output voltage would ideally be 0V. However, the output voltage can never reach 0V because this is also the value of the negative power supply. Therefore, the op amp output will “saturate” near its negative power supply. This condition is undesirable and can delay the amplifier’s response to an input signal. In order to avoid saturation, a resistor divider from the positive supply is used to bias the amplifier input above ground.

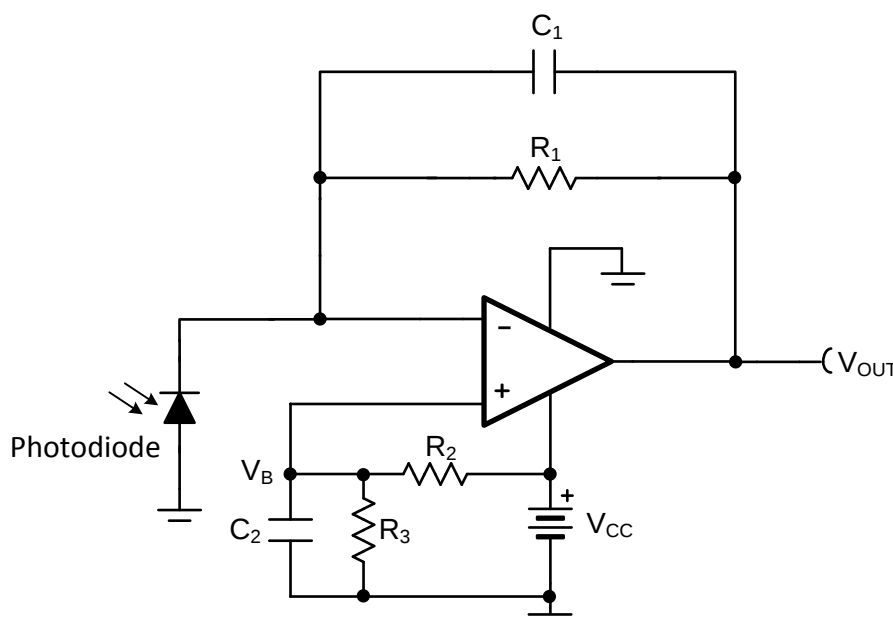


Figure 4: A bias voltage is applied to the op amp’s non-inverting input to prevent saturation at the negative power supply

The output transfer function including the bias voltage is:

$$V_{OUT} = i_{PD}R_1 + V_B = i_{PD}R_1 + V_{CC} \frac{R_3}{R_3 + R_2} \quad (2)$$

2.1 Photodiode Parameters

An OSRAM SFH213 photodiode was selected for this design. In this design the photodiode is minimally reverse biased and therefore the junction capacitance when $V_R = 0V$ will be used for stability calculations. Also, because of the minimal reverse bias, the effects of dark current on the amplifier output can be neglected.

Table 2: Selected photodiode parameters

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Diode Capacitance	$V_R = 0V$	C_J		11		pF
Reverse Light Current	$E_e = 1mW/cm^2$	I_{PD}		90		μA

2.2 Gain Calculation

The reverse light current specification in Table 2 will be used as the maximum input current to the amplifier. The value of the feedback resistor can be calculated by dividing the maximum output voltage (limited by the amplifier’s power supply) by the maximum input current:

$$\frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{I_{IN(MAX)}} = R_1 \rightarrow \frac{4.9V - .1V}{90\mu A} = 53333.3\Omega \rightarrow 53.6k\Omega \quad (3)$$

2.3 Feedback Capacitor Calculation

The feedback capacitor, in combination with the feedback resistor, forms a pole in the frequency response of the amplifier:

$$f_P = \frac{1}{2\pi C_1 R_1} \quad (4)$$

Above this pole frequency, the amplification of the circuit will decline. The maximum feedback capacitor value can be determined from the feedback resistor value and the desired bandwidth:

$$C_1 \leq \frac{1}{2\pi R_1 f_P} \leq \frac{1}{2\pi (53.6k\Omega)(1MHz)} \leq 2.97pF \rightarrow 2.7pF \quad (5)$$

By keeping the feedback capacitor at or below the value calculated in equation 3, we ensure that our circuit will meet the stated bandwidth requirements.

2.4 Amplifier Gain Bandwidth Calculation

Having calculated the maximum feedback capacitor value allowable to meet the design requirement for bandwidth, it is necessary to calculate the necessary op amp gain bandwidth for the circuit to be stable.

In Figure 5, the circuit in Figure 4 has been redrawn to show the junction capacitance of the photodiode (C_J) and the differential (C_D) and common-mode (C_{CM1} , C_{CM2}) input capacitances of the amplifier. The bias voltage applied to the non-inverting input is considered an ac ground.

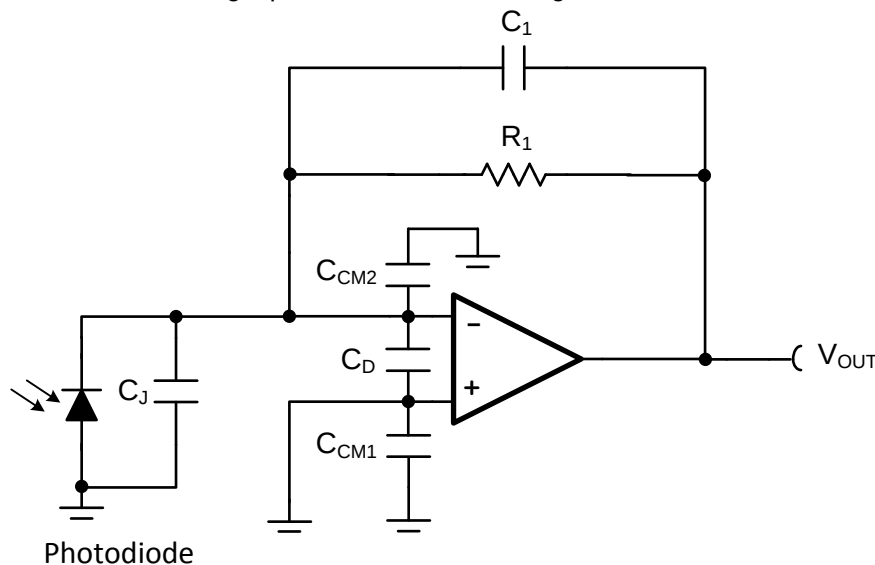


Figure 5: Transimpedance amplifier circuit showing capacitances at the inverting node.

From this illustration it is apparent that C_J , C_D , and C_{CM2} are in parallel and the capacitance at the inverting input is:

$$C_{IN} = C_J + C_D + C_{CM2} \quad (6)$$

C_{CM1} is shorted by the ac ground at the non-inverting input and does not contribute to the input capacitance calculation.

Figure 6 shows the open loop gain (A_{OL}) and inverse feedback factor ($1/\beta$) curves for a typical transimpedance amplifier. A rate-of-closure (ROC) analysis is one method to infer the stability of a system by graphically observing the rate of closure between the A_{OL} and $1/\beta$ where they intersect. For a stable system these curves should intersect with a rate-of-closure of 20dB/decade. For example, if the A_{OL} curve of an amplifier decreases at 20dB/decade and the $1/\beta$ curve is increasing at 20dB per decade at the point of intersection, the rate of closure is 40dB/decade and the system is potentially unstable.

The capacitance at the inverting input of the op amp produces a zero in the $1/\beta$ curve at:

$$f_z = \frac{1}{2\pi(C_1 + C_{IN})R_1} \quad (7)$$

Above this zero, the $1/\beta$ curve will rise at 20dB/decade. If the A_{OL} curve intersects the $1/\beta$ curve in this rising portion (as illustrated by the dashed line in Figure 6) the system will potentially be unstable.

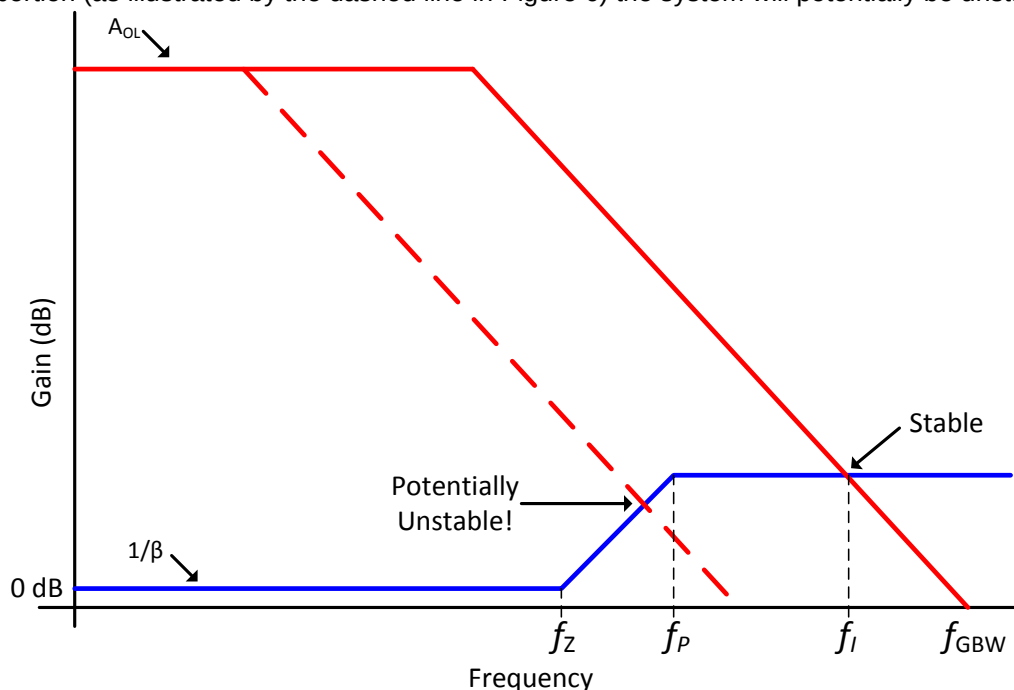


Figure 6: The open loop gain (red) and inverse feedback factor (blue) curves of a typical transimpedance amplifier.

For the amplifier to be stable, the A_{OL} curve should intersect the $1/\beta$ curve after the pole created by the feedback capacitor:

$$f_p = \frac{1}{2\pi C_1 R_1} \quad (8)$$

In the region above the pole, the frequency of intersection is:

$$f_I = \frac{C_1}{C_{IN} + C_1} f_{GBW} \quad (9)$$

where f_{GBW} is the unity gain bandwidth of the op amp. Therefore, in order to ensure stability, the unity bandwidth of the op amp must obey the rule:

$$f_I > f_p \quad (10)$$

Inserting the equations for f_I and f_p into this rule and solving for unity gain bandwidth, we arrive at a useful equation:

$$\frac{C_1}{C_{IN} + C_1} f_{GBW} > \frac{1}{2\pi R_1 C_1} \quad (11)$$

$$f_{GBW} > \frac{C_{IN} + C_1}{2\pi R_1 C_1^2} \quad (12)$$

To calculate the unity gain bandwidth requirement for this design, C_{IN} must first be determined. C_D and C_{CM2} are not known at this time since we haven't selected a specific op amp. 10pF can be used as a reasonable guess for the sum of these values. The exact value can be substituted later to confirm the appropriateness of an op amp.

$$C_{IN} = C_J + C_D + C_{CM2} = 11pF + 10pF = 21pF \quad (13)$$

Now, the values for C_1 , R_1 and C_{IN} can be inserted into equation 13:

$$f_{GBW} > \frac{21pF + 2.7pF}{2\pi(53.6k\Omega)(2.7pF)^2} > 9.653MHz \quad (14)$$

2.5 Bias Network

The photodiode acts as a reverse biased diode at dc, so the gain from the non-inverting terminal of the op amp is 1. Therefore when the photodiode current is 0A, $V_{OUT} = V_B$. A bias voltage of 100mV is derived from the positive supply and applied to the non-inverting input to prevent the amplifier output from saturating at the negative power supply rail. The bias at the non-inverting input is given by the equation:

$$V_B = V_{CC} \frac{R_3}{R_2 + R_3} \quad (15)$$

For a 100mV bias voltage:

$$\begin{aligned} .1 &= 5 \frac{R_3}{R_2 + R_3} \\ .02 &= \frac{R_3}{R_2 + R_3} \\ R_2 &= 49R_3 \end{aligned} \quad (16)$$

The closest 1% resistor values which conform to this ratio is R_2 : 13.7k Ω , R_3 : 280 Ω .

Capacitor C2 is placed in parallel with resistor R3 to reduce the noise contribution of the resistor divider and prevent power supply noise from affecting the amplifier output. Selecting a value of 1 μ F for C2 produces a corner frequency of:

$$f_p = \frac{1}{2\pi C_2 (R_2 || R_3)} = \frac{1}{2\pi * 1\mu F * (13.7k || 280)} = 580.028Hz \quad (17)$$

This corner frequency should be low enough to prevent power supply noise from passing to the output.

3 Component Selection

3.1 Amplifier

The basic requirements for the op amp used in this application are outlined in Table 3.

Table 3: Basic op amp requirements

Parameter	Value
Minimum Supply Voltage	<5V
Quiescent Current	<2mA
Input Voltage Range	(V-)+0.1
Output Voltage Range	(V-)+0.1, (V+)-0.1
Gain Bandwidth Product	>9.653 MHz

The requirements for supply voltage and current were given in Table 1. The input and output voltage range requirements are selected to ensure linear operation over the desired signal amplitudes. Finally, the gain bandwidth requirement was calculated in section 2.

In addition to these basic requirements, the op amp should contribute negligible errors from voltage offsets and noise. Op amps with JFET or CMOS inputs are the most commonly selected type because these op amps typically have much lower bias current than those with BJT input devices. This results in reduced dc error voltages and lower noise due to reduced input current noise. A complete noise analysis of this amplifier is beyond the scope of this document, please see reference [1] for more information on noise in photodiode amplifiers.

The OPA320 was selected for this design because of its excellent combination of low bias current, offset voltage, power consumption and wide bandwidth. Relevant OPA320 specifications are given in Table 4.

Table 4: Relevant OPA320 specifications

Parameter	Required	OPA320
Minimum Supply Voltage	<5V	1.8V
Quiescent Current	<2mA	1.5mA
Input Voltage Range	(V-)+0.1	(V-)-0.1
Output Voltage Range	(V-)+0.1, (V+)-0.1	(V-)+0.01, (V+)-0.01
Gain Bandwidth Product	>9.653 MHz	20 MHz
Input Bias Current	-	0.2pA
Input Offset Voltage	-	40μV
Input Capacitance (CM DM)	-	4 pF 5 pF
Slew Rate	-	10 V/μs

The OPA320 meets or exceeds all required specifications for the design. Also, the parallel combination of the differential and common mode input capacitances is 9pF, slightly less than the estimated value used to calculate the required gain bandwidth product. The gain bandwidth requirement previously calculated is still adequate to achieve a stable design.

The slew rate of the OPA320 does impose a limitation to the full power bandwidth of the circuit. The full power bandwidth is the highest frequency sinusoid that can be reproduced at the full output swing of the amplifier. The full power bandwidth can be calculated using the equation:

$$f_{FP} = \frac{SR}{2\pi A} \quad (18)$$

SR is the slew rate of the op amp in Volts per second, and A is the amplitude of the sinusoid. The full output swing of this amplifier is from .1V to 4.9V, or a swing of 4.8V. Therefore the amplitude of the sinusoid would be $4.8V/2 = 2.4V$. The resulting full power bandwidth is:

$$f_{FP} = \frac{10 \times 10^6}{2\pi(2.4)} = 663.146kHz \quad (19)$$

Above this frequency the amplifier will produce a distorted output for full-scale signals.

3.2 *Passive Components*

Resistors

1% resistors were used throughout the design. If greater precision is required higher tolerance resistors may be used.

Capacitors

The compensation capacitor, C1, should be a NP0/C0G type ceramic capacitor to avoid affecting the frequency response or output distortion of the amplifier. Capacitor C2 can be a high-k dielectric type with a suitable voltage rating. The decoupling capacitors used on the PCB were also high-k ceramic capacitors.

4 Simulation

Figure 7 is the TINA-TI™ simulation schematic of the photodiode amplifier. Current source IPD and 11pF capacitor CJ form a simple simulation model for the photodiode.

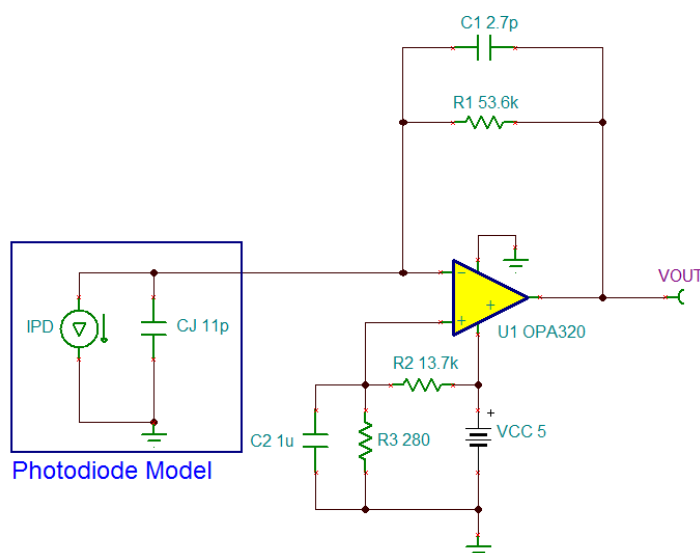


Figure 7: TINA-TI™ simulation schematic used to verify photodiode amplifier performance

4.1 DC Transfer Function

A dc transfer characteristic analysis is used to verify the gain and output voltages of the circuit. The output current of IG1 is swept from 0 to 90μA and the output voltage is plotted.

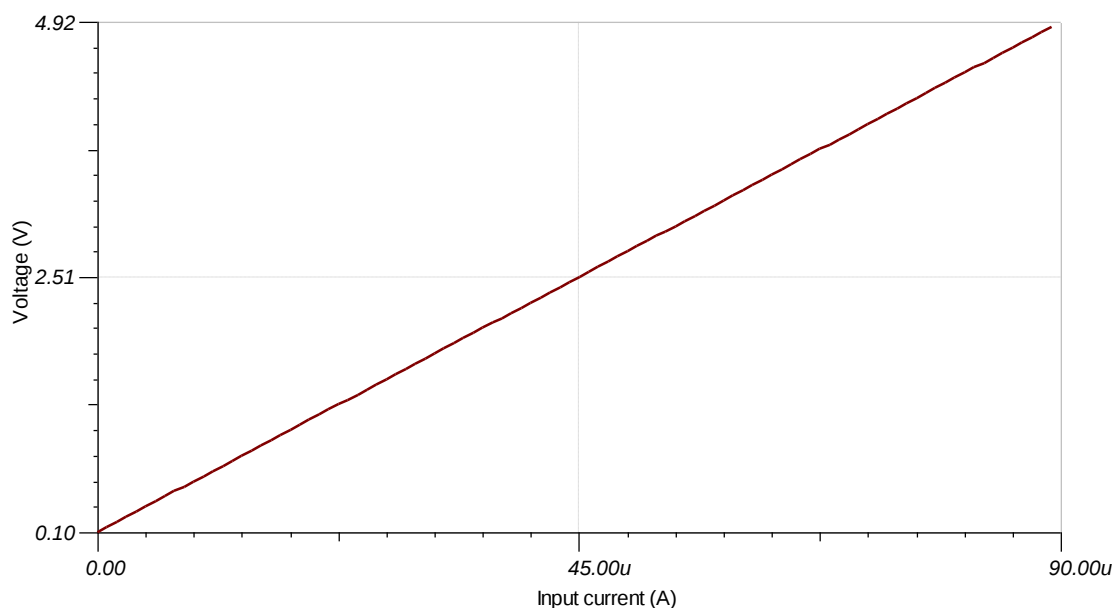


Figure 8: Simulated output voltage of photodiode amplifier for 0 to 90uA input current.

For zero input current, the simulated output voltage is 100.096mV. At 90μA input current, the simulated output voltage is 4.924V and the gain is 53.6 kV / A.

4.2 AC Transfer Function

The ac transfer function was measured using an ac transfer characteristic analysis in TINA-TI™. The simulated -3dB point was 1.464MHz.

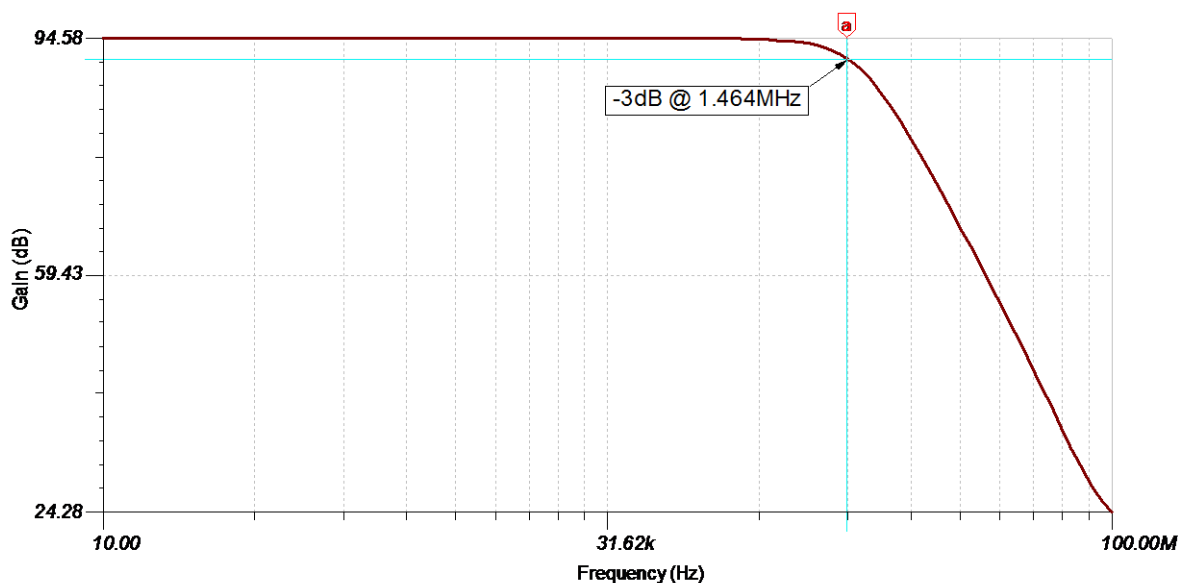


Figure 9: AC transfer function of the photodiode amplifier. The -3dB point is 1.464 MHz.

4.3 Stability Analysis

For simulation of the loop stability, the feedback path of the amplifier is broken at the output using a large inductor (L1). This inductor allows the circuit to converge to the proper dc bias point but acts as an open circuit in an ac transfer characteristic simulation. Voltage source VG1 is ac coupled into the feedback loop by capacitor C4 and the loop gain is measured by voltage probe VOUT.

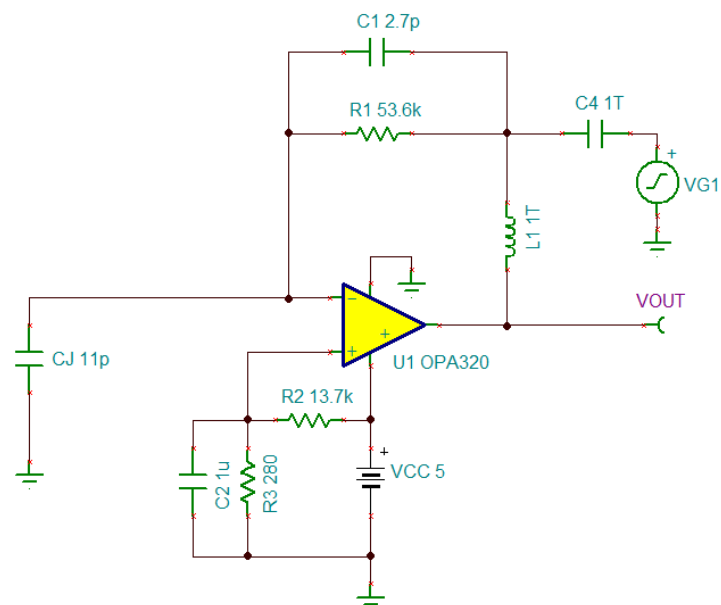


Figure 10: TINA-TI™ simulation schematic for measuring loop gain.

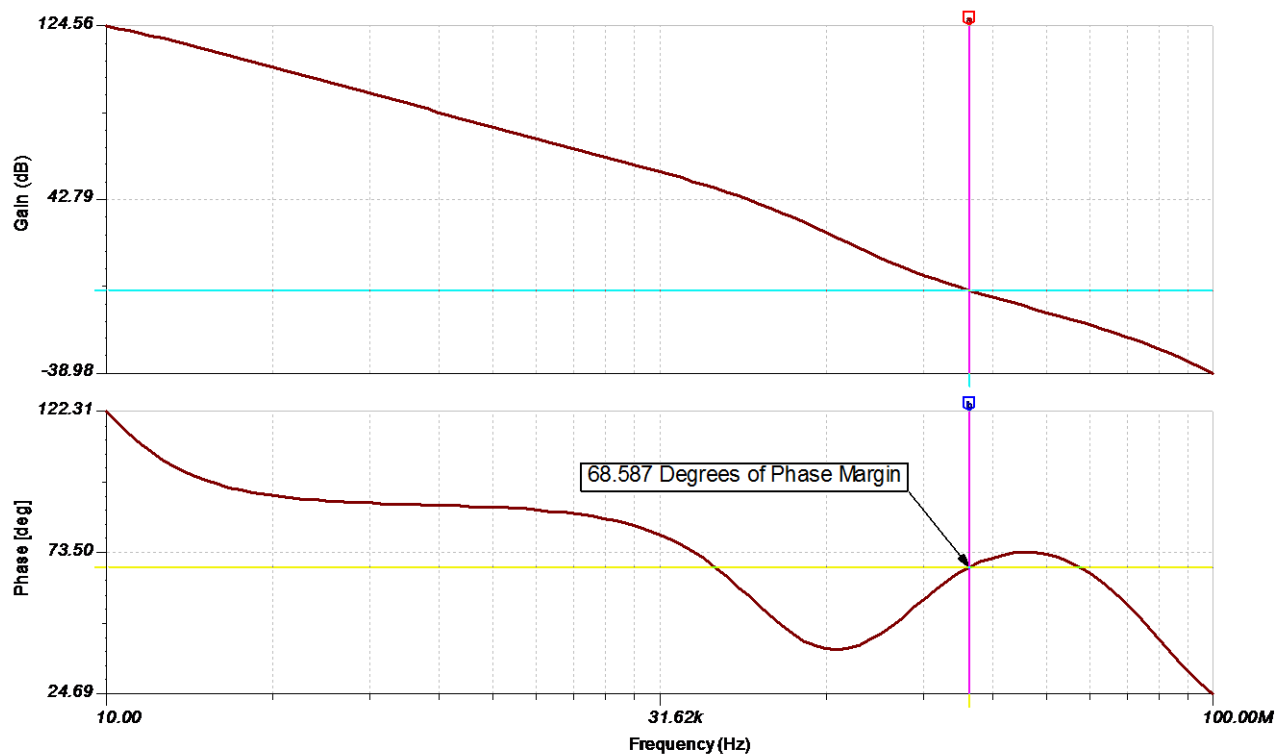


Figure 11: Bode plot of the photodiode amplifier loop gain.

The loop gain plot shows the loop closure point (loop gain is 0dB) at 2.92MHz with 68.59 degrees of phase margin

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

Special care must be taken in the PCB layout of photodiode amplifiers because additional parasitic capacitance added to the inverting input of the amplifier can make the circuit unstable. For this reason, the ground pour of the PCB is removed in the areas around the inverting input of the op amp on both layers.

An output resistor, R4, is added for two reasons. First, this resistor isolates the capacitance of the output connector and any attached cables from the amplifier output to avoid stability issues. Second, by choosing a value of 49.9 ohms for R4, the output impedance of the amplifier is matched to the characteristic impedance of typical coaxial cables and the input impedance of wide bandwidth lab equipment. The trace between the output resistor R4 and output connector J4 is a microstrip transmission line with a 50 ohm impedance. Matching of the output impedance to coaxial cables and measurement equipment prevents ringing in the transient response of wide-bandwidth systems.

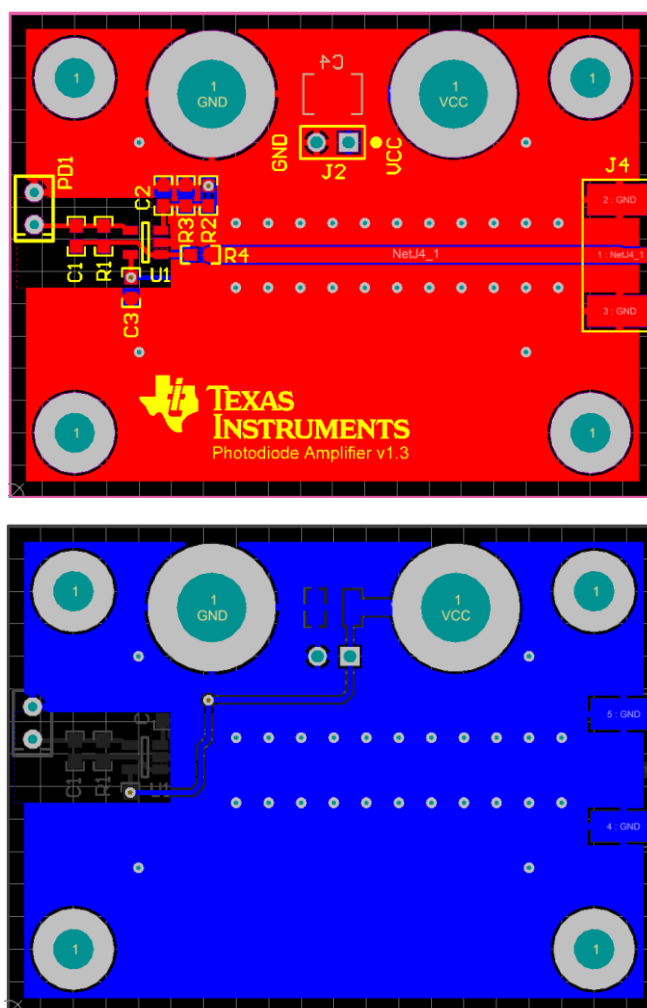


Figure 12: PCB layout of the photodiode amplifier. The top layer is shown in red and the bottom layer is shown in blue.

6 Verification & Measured Performance

6.1 DC Transfer Function

A precision current source was used to measure the dc transfer function. The measured gain of the circuit was 53.479kV/A and the offset was 100.256mV.

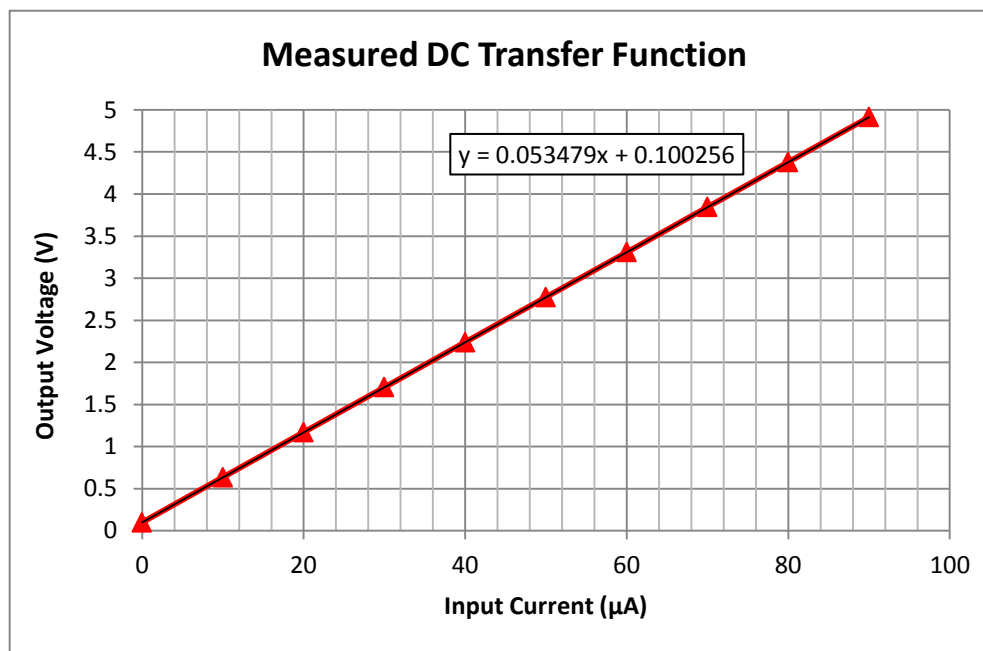


Figure 13: Measured DC transfer function of the photodiode amplifier

6.2 AC Transfer Function

An RC circuit was added to the output of a network analyzer to convert it from a voltage source to a current source, mimicking a photodiode. In Figure 14, resistor R5 was selected to produce an output current of approximately 1μA at the network analyzer's reference output level. Capacitor C4 is a standard value COG capacitor chosen to be very close to the photodiode junction capacitance used in the design.

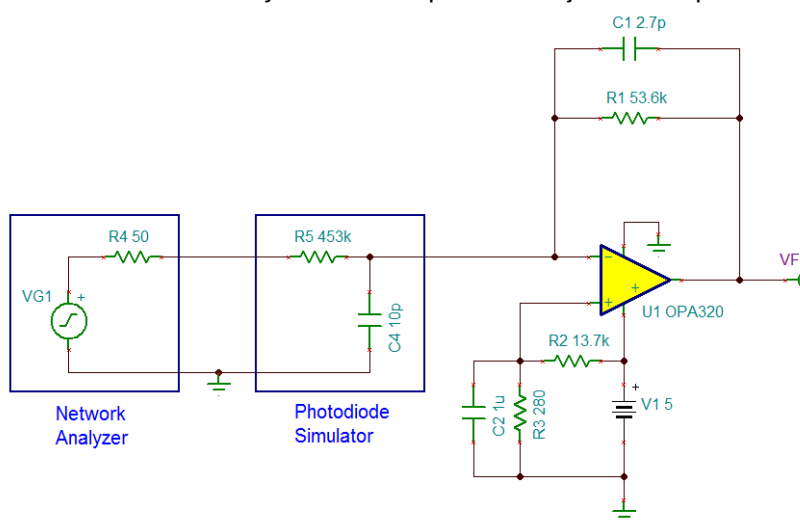


Figure 14: Schematic of test configuration for ac performance measurement

The AC transfer characteristic was measured from 100Hz to 40MHz and is shown in Figure 15. The measured -3dB point was 1.59MHz.

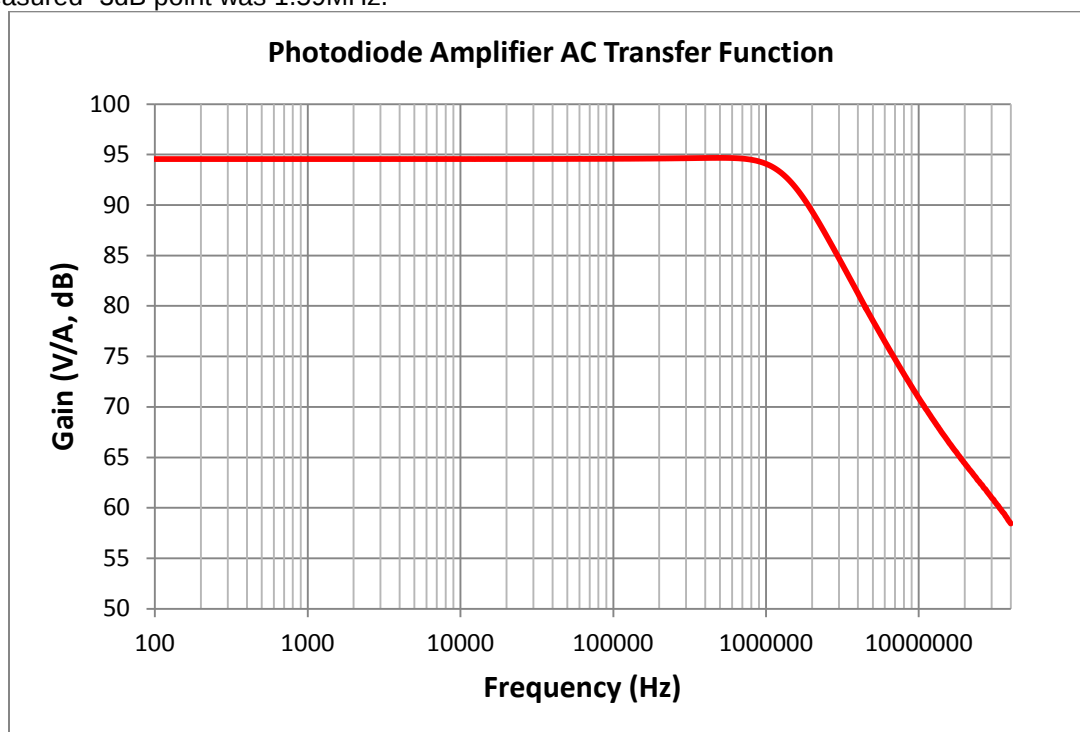


Figure 15: Plot of the ac transfer function from 100Hz to 40MHz

Figure 16 is a high resolution plot of the AC transfer characteristic below the roll-off. The peaking in this point of the curve can be used to estimate the phase margin of the system.

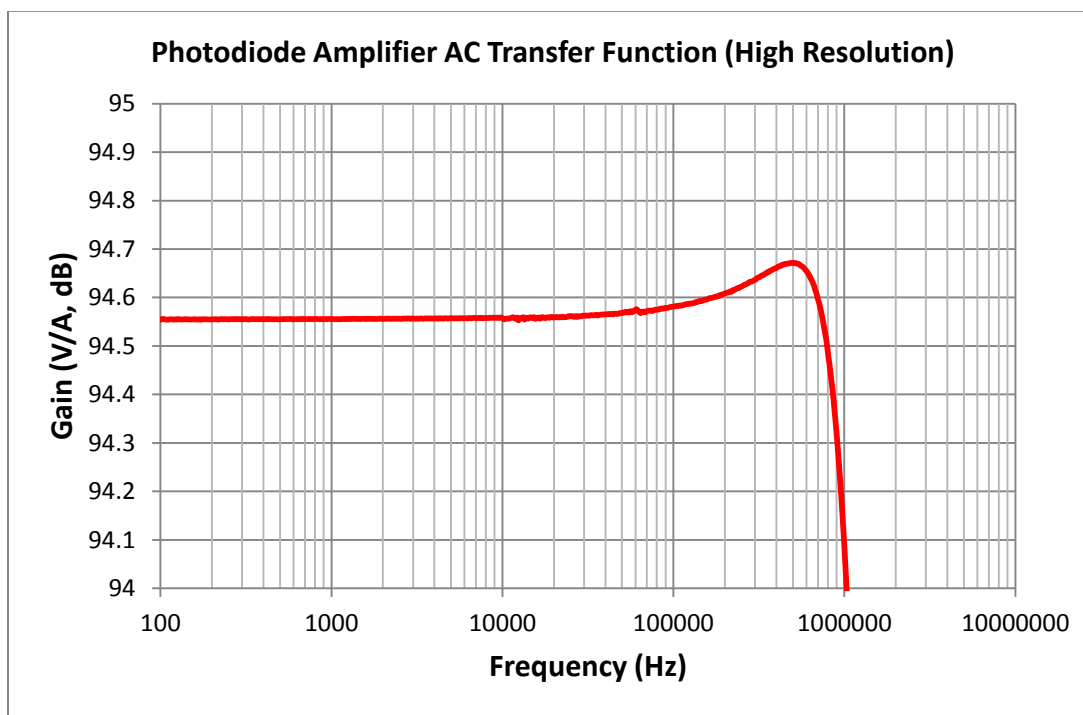


Figure 16: High resolution plot of the ac transfer function below roll-off.

The amplifier transfer function shows 0.12dB of peaking. This amount of peaking can be related to the damping factor of the system using the equation:

$$Peak(dB) = -10\log(4\zeta^2(1 - \zeta^2)) \quad (20)$$

Inserting a value of 0.12dB and solving for the damping ratio ζ gives 4 possible solutions. However, the only valid solutions for the damping ratio are: $0 < \zeta < 1/\sqrt{2}$. With this criteria, 3 solutions are eliminated and $\zeta = .646111$.

The value for damping ratio can determine the phase margin of the system using the equation:

$$\phi_M = \tan^{-1} \left(\frac{\sqrt{2}}{\sqrt{1 + \frac{1}{4\zeta^4} - 1}} \right) \quad (21)$$

Inserting the previously determined value for damping ratio, results in a phase margin of 62.108°.

The slightly higher bandwidth and reduced phase margin are most likely due to the actual value of the compensation capacitor, C1. Decreasing the compensation capacitor will increase the bandwidth and decrease the phase margin. Although the nominal value for this capacitor is 2.7pF, it has a tolerance of +/- .25pF.

The RC photodiode simulator was also used with a standard function generator to inject a small-signal square wave into the amplifier in order to observe the system step response. Figure 18 shows the output of the amplifier for a small-signal step. The response is completely devoid of ringing which indicates a stable system.

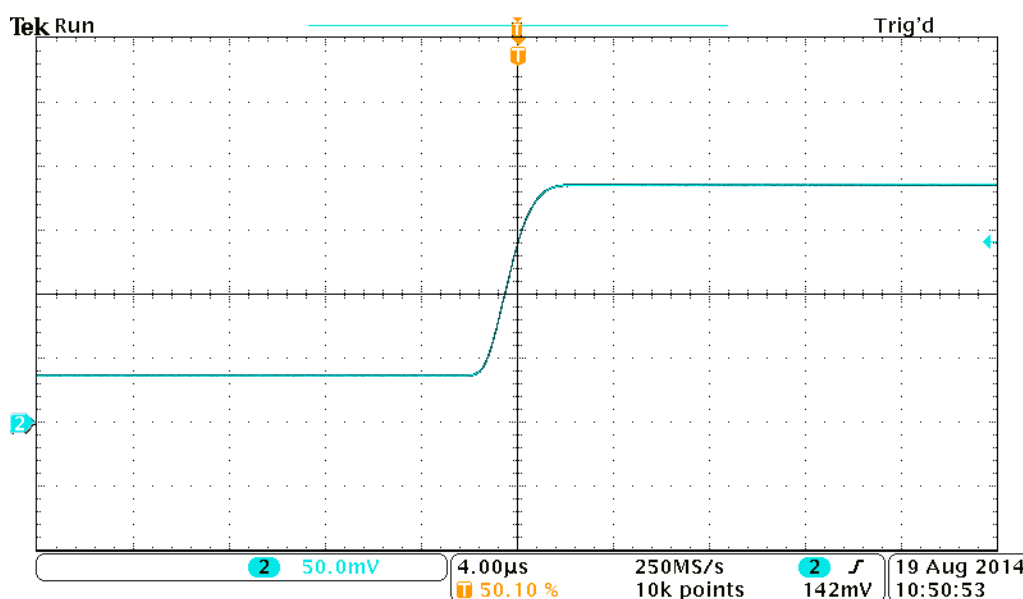


Figure 17: Small signal step response produced using the RC photodiode simulator.

A final test of the system ac performance was performed by installing the SFH213 photodiode onto the PCB and illuminating the photodiode with a light source. For this test, a blue LED and 162 ohm resistor were installed onto the output of [TIPD108](#), the output light signal is a square wave at 500kHz. The amplifier output is shown in Figure 18 and is devoid of ringing.

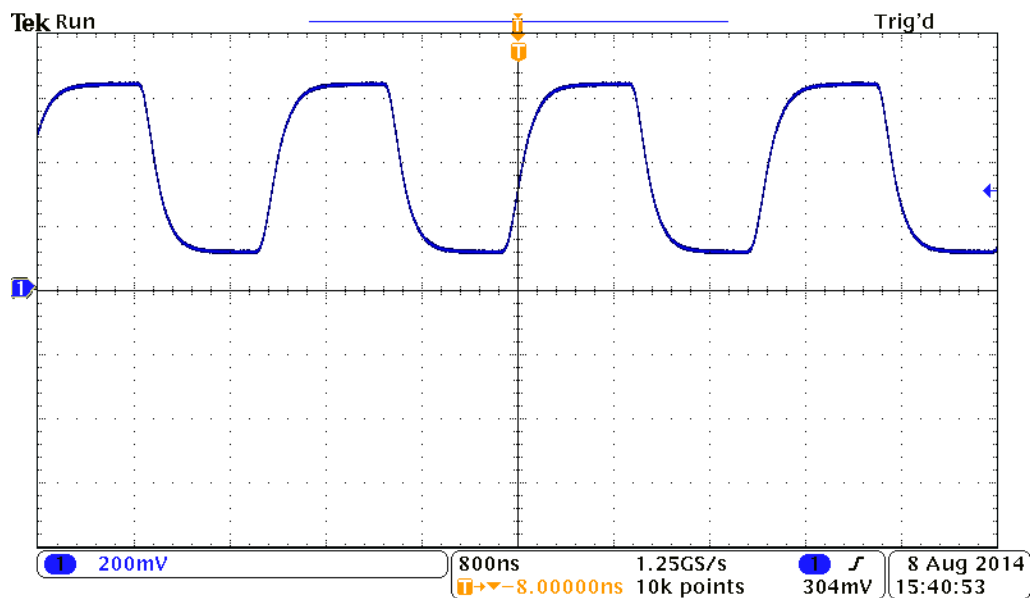


Figure 18: Photodiode amplifier output with SFH213 photodiode illuminated by a blue LED flashing at 500 kHz.

7 Modifications

Several alternate op amps are available which may be used to increase the bandwidth or reduce the power consumption of the system. For example, the OPA354 is a CMOS amplifier with a gain bandwidth product of 250MHz. The wider bandwidth of the OPA354 would allow for the compensation capacitor value to be reduced, achieving greater overall system bandwidth. Alternatively, a decompensated op amp such as the LMP7717 may provide both wider bandwidth and lower power consumption but will require a different compensation scheme.

8 About the Author

John Caldwell is an applications engineer with Texas Instruments Precision Analog, supporting operational amplifiers and industrial linear devices. He specializes in precision circuit design for sensors, low-noise design and measurement, and electromagnetic interference issues. He received his MSEE and BSEE from Virginia Tech with a research focus on biomedical electronics and instrumentation. Prior to joining TI in 2010, John worked at Danaher Motion and Ball Aerospace.

9 Acknowledgements & References

1. A. Kay, *Operational Amplifier Noise: Techniques and Tips for Analyzing and Reducing Noise*. Elsevier, 2012.

Appendix A.

A.1 Electrical Schematic

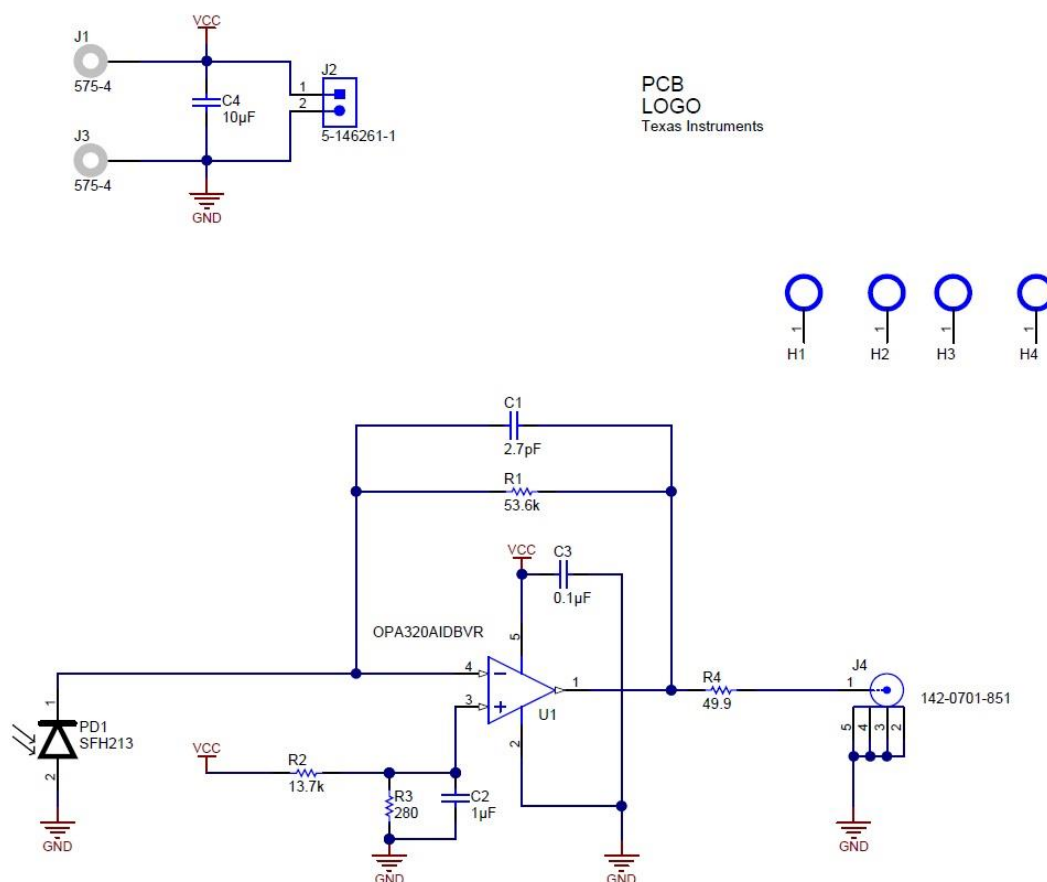


Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	Qty	Value	REF DES	Description	Manufacturer	Part Number
1	1	2.7pF	C1	CAP, CERM, 2.7pF, 50V, +/-9%, C0G/NP0, 0603	AVX	06035A2R7CAT2A
2	1	1uF	C2	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603	Kemet	C0603C105K4PACTU
3	1	0.1uF	C3	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
4	1	10uF	C4	CAP, CERM, 10uF, 10V, +/-10%, X5R, 1210	Kemet	C1210C106K8PACTU
5	2		J1, J3	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4
6	1		J2	Header, 100mil, 2x1, Gold, TH	TE Connectivity	5-146261-1
7	1		J4	Connector, SMT, End launch SMA 50 ohm	Emerson Network Power	142-0701-851
8	1		PD1	Silicon PIN Photodiode	Osram	SFH213
9	1	53.6k	R1	RES, 53.6k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060353K6FKEA
10	1	13.7k	R2	RES, 13.7k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060313K7FKEA
11	1	280	R3	RES, 280 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603280RFKEA
12	1	49.9	R4	RES, 49.9 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060349R9FKEA
13	1		U1	Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier	Texas Instruments	OPA320AIDBVR

Figure A-2: Bill of Materials

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