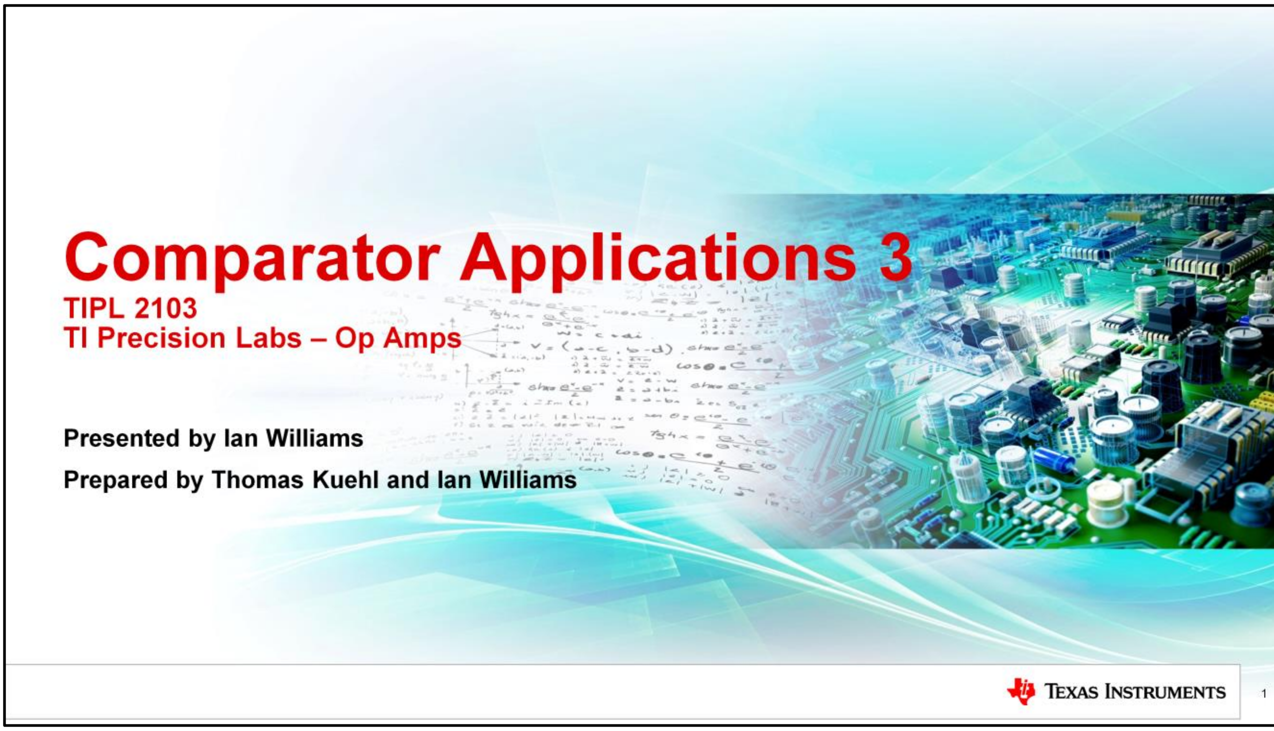
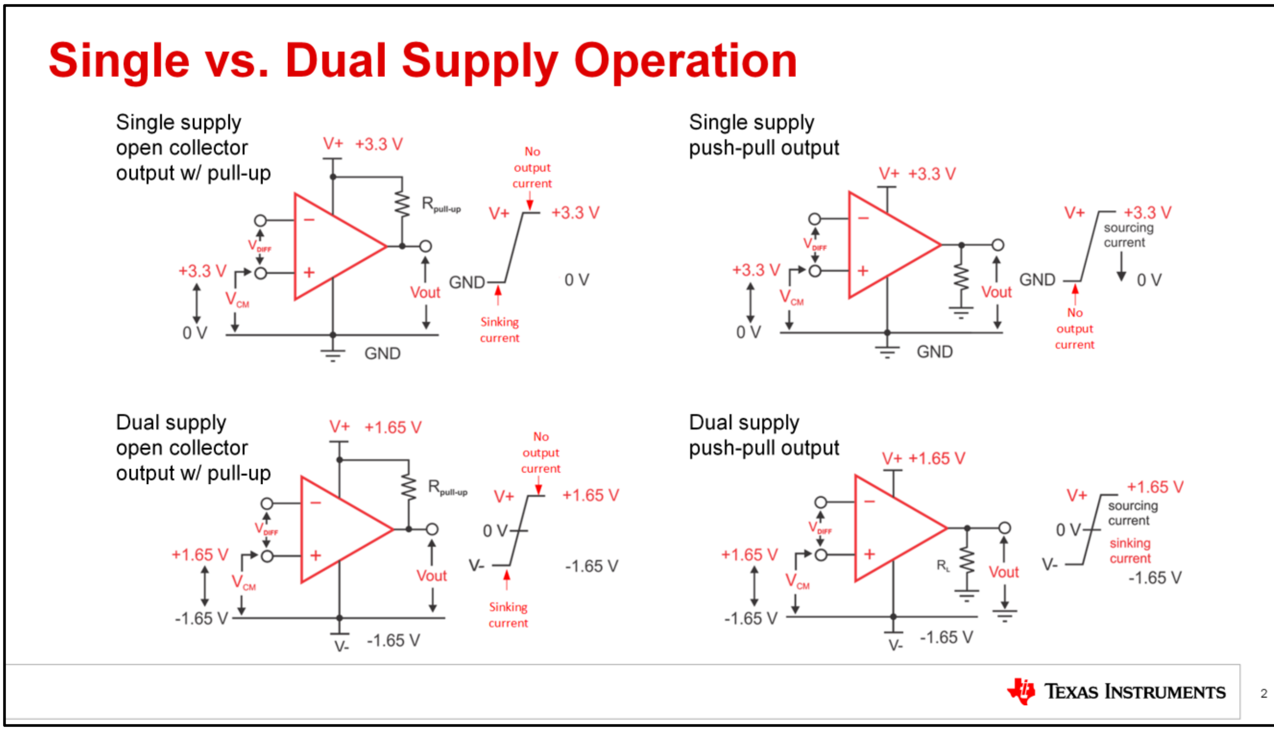


Hello, and welcome to the TI Precision Labs video discussing comparator applications, part 3. In this video we will discuss several comparator topics, including the difference between using single and dual power supplies in comparator designs, the common mode voltage limitations of comparators, start-up uncertainty in the output signal of a comparator, and the AC considerations of shoot-through current, propagation delay and maximum toggle frequency.



Engineers frequently wonder if comparators can be used successfully with dual power supplies. Although comparators are most often shown and specified in a single supply configuration, they can almost always be configured for dual supply. This slide shows four examples of 3.3V open collector and push-pull output comparators being used with both single and dual supplies. The main differences between configurations are the input and output voltage range and the output current behavior.

In the upper left hand corner we have an **open collector** comparator configured for **single supply**.

When the output of this circuit is a logic **high**, the output stage transistor is **off** and the pull-up resistor pulls the voltage up to the supply. In this state no current is being drawn by the comparator's output and no current flows through the pull-up resistor. When the output is driven low to 0V, the comparator's output stage transistor is **on** and the full supply voltage of 3.3V is present across the pull-up. The current in the output stage can be computed to be the supply voltage divided by the pull-up resistance.

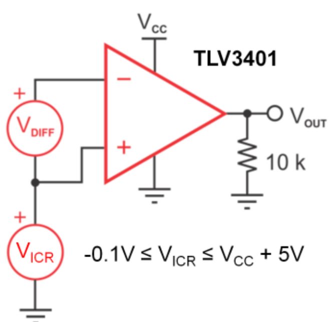
In the lower left hand corner we have the **open collector** comparator configured for **dual supply**. The total supply voltage from V+ to V- is still 3.3V, just shifted such that the mid-supply is equal to 0V. Now V+ is +1.65V and V- is -1.65V. For this circuit, the input common mode range and output swing range extends across the supply range from -1.65V to +1.65V. Like the single supply circuit, this configuration will require no current when the output is high at +1.65V, and will sink current when the output is low at -1.65V.

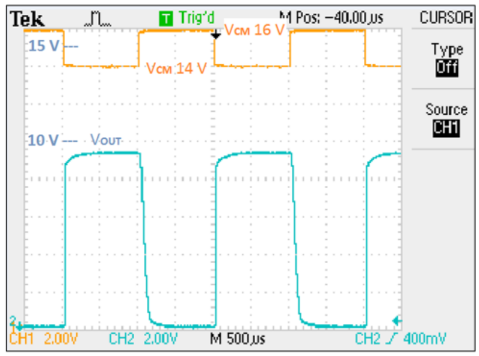
On the upper right is the **push-pull** comparator configured for **single supply**. In this case, the output is connected to a load resistor. When the output of the comparator is low at 0V, the output current is zero because the voltage across the load is zero. When the output is high at 3.3V, the comparator sources current equal to 3.3V divided by the load resistance.

Finally, on the lower right we have the **push-pull** comparator configured for **dual supply**. In this case the comparator must source current when it drives the output high to +1.65V, and must sink current when it drives the output low to -1.65V.

Comparator Input Common Mode Voltage (V_{ICR})

	MIN	MAX	UNIT
Common-mode input voltage, V_{ICR}	–0.1	V_{CC} + 5	V





V_{CC}	V_{ICR}	$V_{DIFFmin}$ (pk-to-pk)
12 V	17 V	1.8 V
10 V	15 V	1.6 V
5 V	10 V	1.2 V
3 V	8 V	1.0 V

As V_{CC} and V_{ICR} increase, higher V_{DIFF} is required

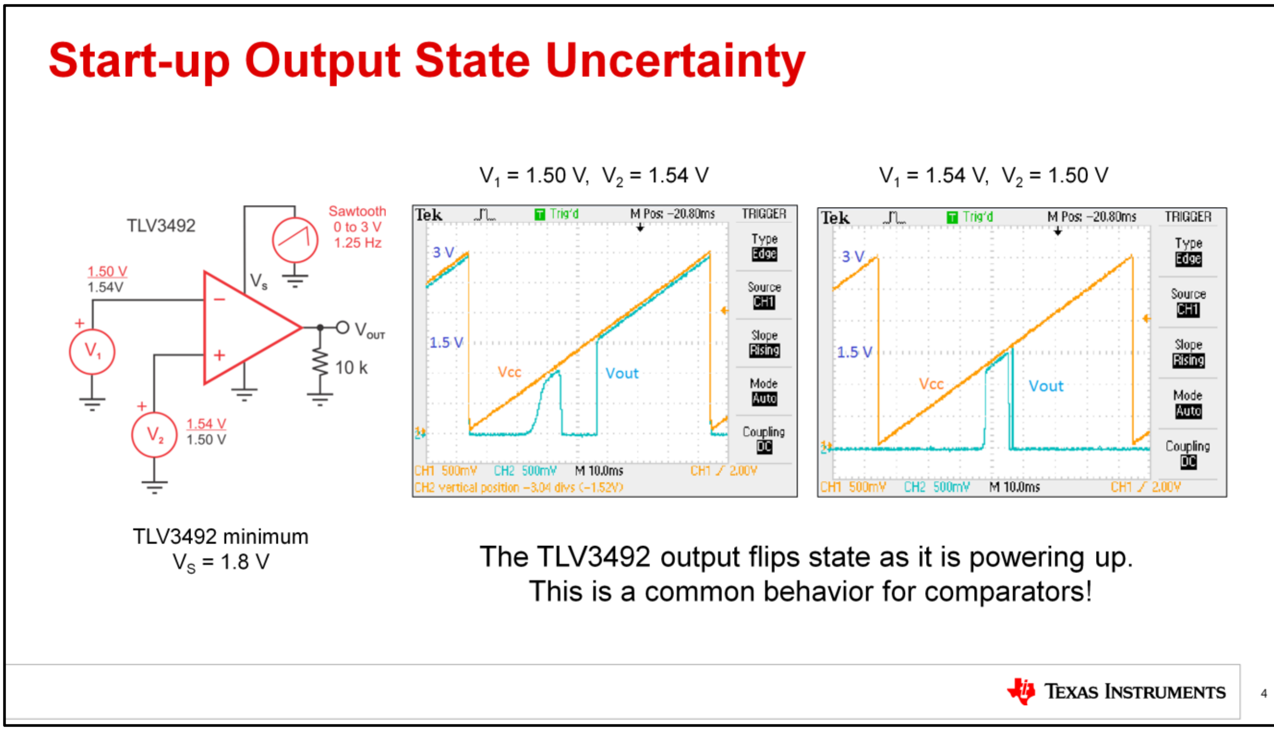
Texas Instruments 3

Let's move on to discussing the input common mode voltage range of comparators. While for many comparators the allowable common mode voltage is straightforward and extends from the negative supply to the positive supply, there are some interesting exceptions.

For example, the TLV3401 and TLV3701 nanopower comparators offer an input common-mode range $\mathbf{V_{ICR}}$ that extends +5V above the positive supply voltage $\mathbf{V_{CC}}$. Engineers often ask if these devices still behave as comparators when operated in that extended common-mode voltage region. Since this is a specification given in the electrical characteristics table of the device data sheet, it is implied that the product will still operate as specified in this condition.

Nevertheless, it is unusual for the common mode range to extend so far above the supply, so we built the circuit shown on the left and tested it on the bench in order to show its operation with input signals 5V above the positive supply. The oscilloscope capture of the circuit operation is given in the center of the slide, where the input signal is shown in orange and the output signal is shown in blue.

The TLV3401 did indeed operate correctly, but interestingly, the differential input voltage required in order to make the output change states was found to increase as V_{CC} increased. These results are summarized in the table on the right. Despite the somewhat larger differential input voltage requirement, this capability might provide a simpler solution for applications where the input voltage has a common mode level that is greater than V_{CC}.

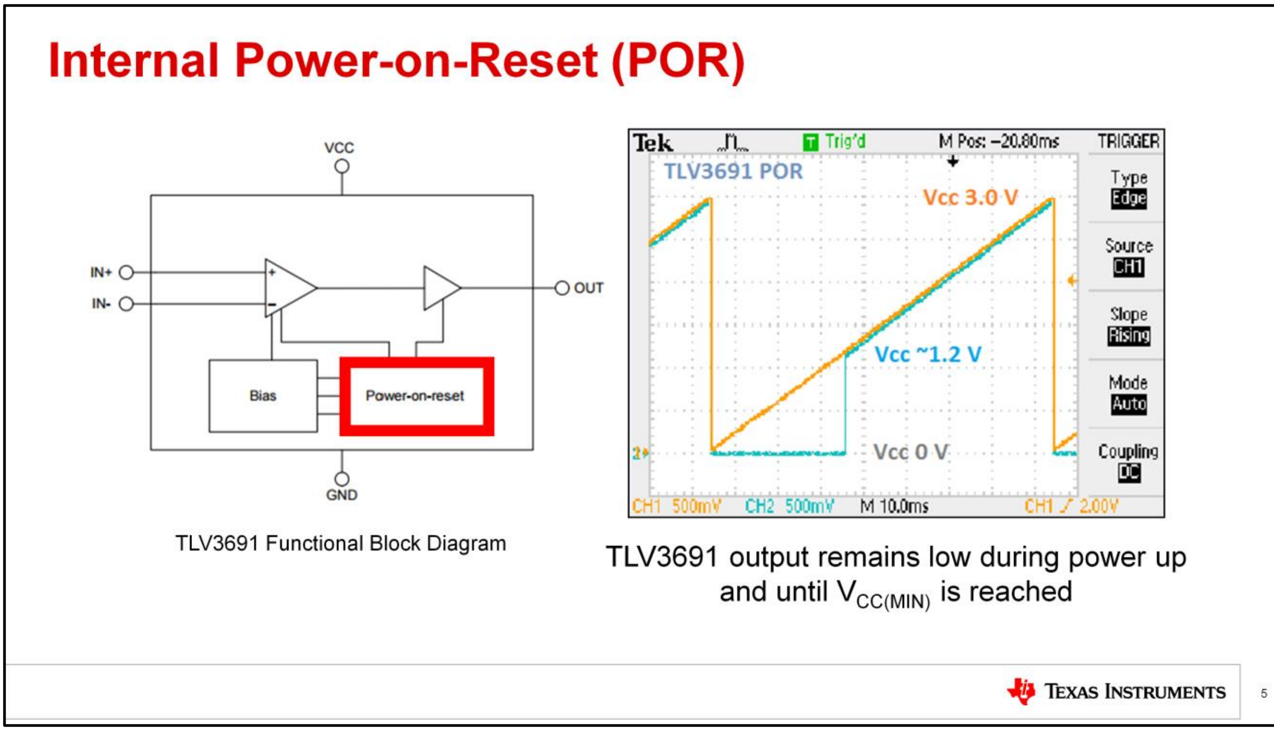


A common issue encountered in comparator circuits is known as start-up output state uncertainty. Start-up state uncertainty means that as the comparator’s power supply is ramped, the output may transition back and forth between states regardless of the input signal. Thus, the output may intermittently provide a false or incorrect state during start-up until the supply voltage reaches the comparator’s minimum specified operating voltage and the device stabilizes. This can be an issue if a circuit following the comparator comes to life quicker during start-up and acts upon an unintended output state coming from the comparator.

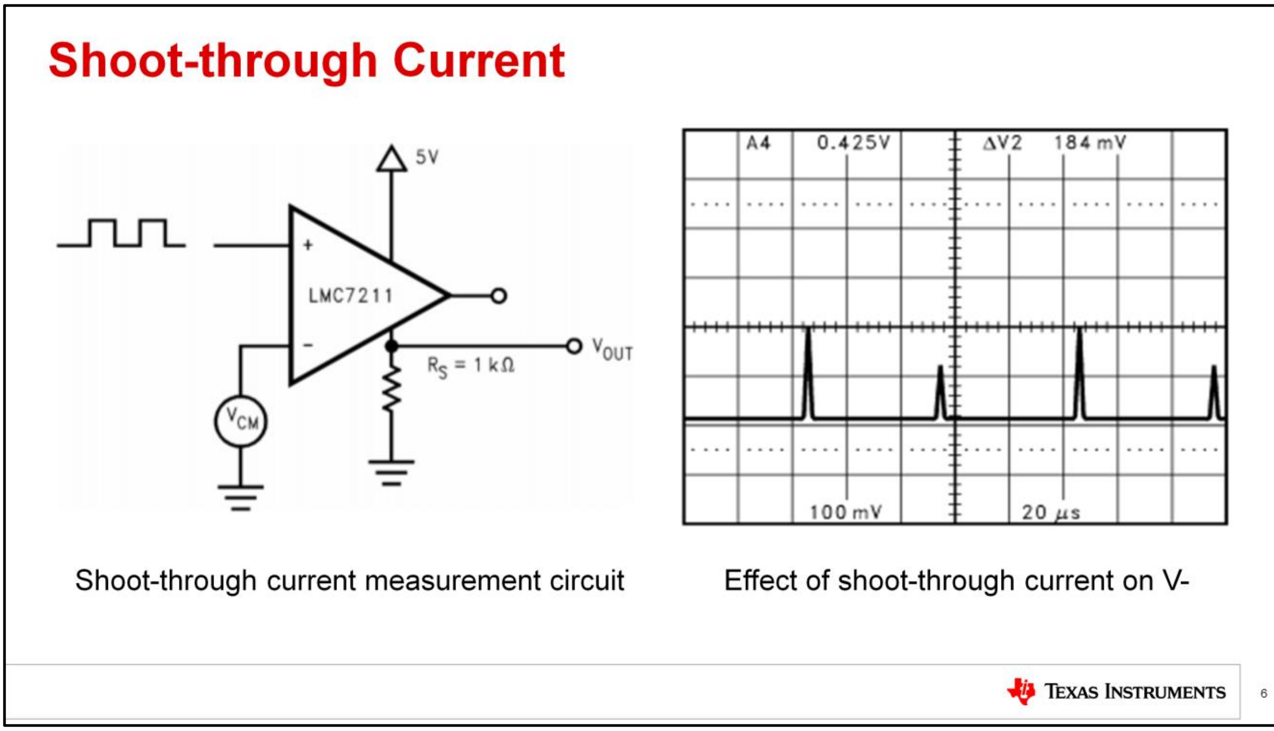
This behavior is illustrated in the circuit shown here using the TLV3492. In this example, the supply voltage is slowly ramped up using a sawtooth generator. Two different sets of input conditions are shown in red and black. For the first case, shown in red, the voltage on the non-inverting input is greater than the voltage on the inverting input, the output should be a logic high. We see that as the supply voltage ramps from 0V to 3V, the output actually flips state from logic low, to logic high, and back to logic low before stabilizing at logic high once the supply reaches 1.5V. After this point, the output of the comparator remains at logic high as expected. Keep in mind that 1.5V is actually below the minimum supply requirement of 1.8V for the TLV3492.

For the second case, shown in black, the inverting input voltage is higher than the non-inverting input voltage. In this case the expected output is logic low, but the actual output briefly transitions to logic high as the supply ramps up.

This uncertain start-up behavior is not unusual, and can be observed in many comparators.



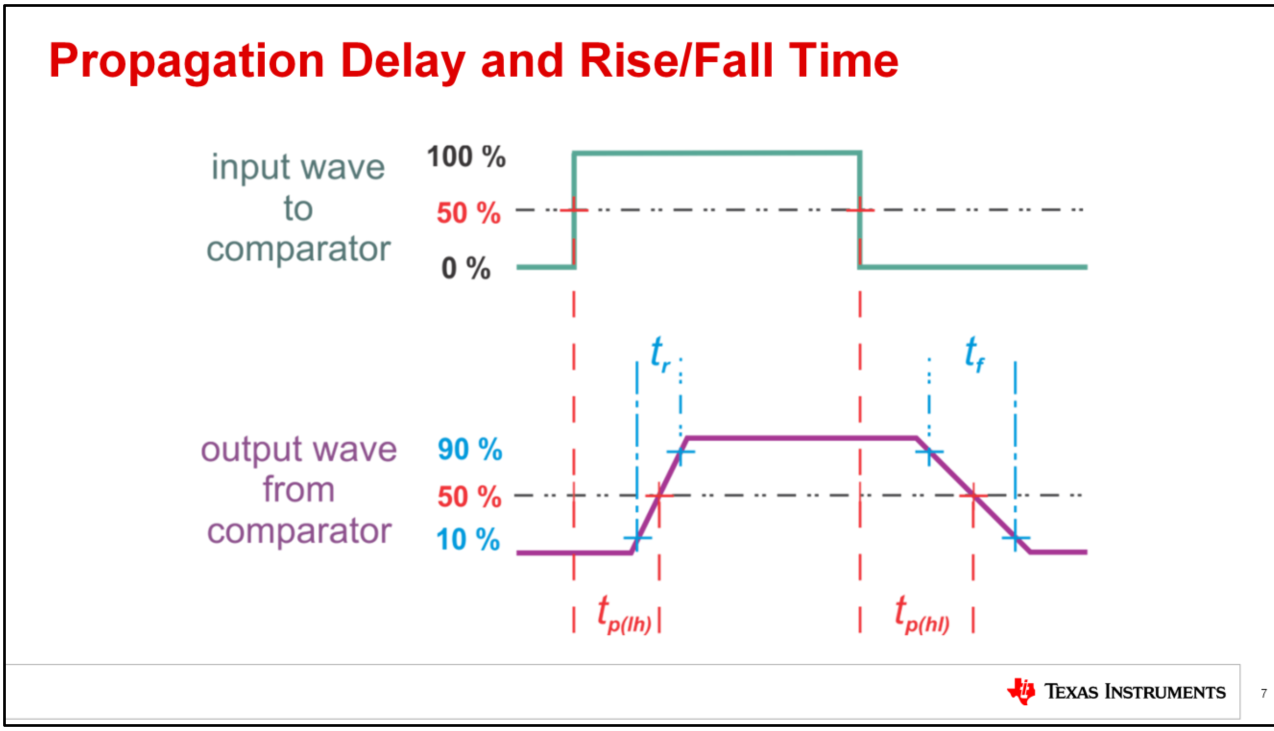
Thankfully, some more modern comparators have internal circuitry which addresses this issue. The TLV3691, for example, has a power-on-reset, or POR, circuit which forces the comparator output low during start-up. If we repeat the supply ramp test from the previous slide, we can observe that the comparator output remains low until the minimum V_{CC} is reached. This can be an important feature in certain applications, where reliable start-up behavior is critical.



An important AC consideration for comparators with push-pull output is something called “shoot-through current”. This is a current surge that flows from the positive supply to the negative supply under certain conditions.

The shoot-through current occurs when the output of the comparator changes state and both output transistors are on for a brief instant in time. This creates a current path from the positive to negative supply through the on resistance of the output transistors, resulting in a short duration “glitch” in the power supply current. These glitches can affect adjacent comparators, especially when using dual or quad-package devices. The supply glitches may also affect adjacent devices connected to the same power supply, as the glitches are fairly high in frequency where the power supply rejection of many devices isn’t necessarily very good.

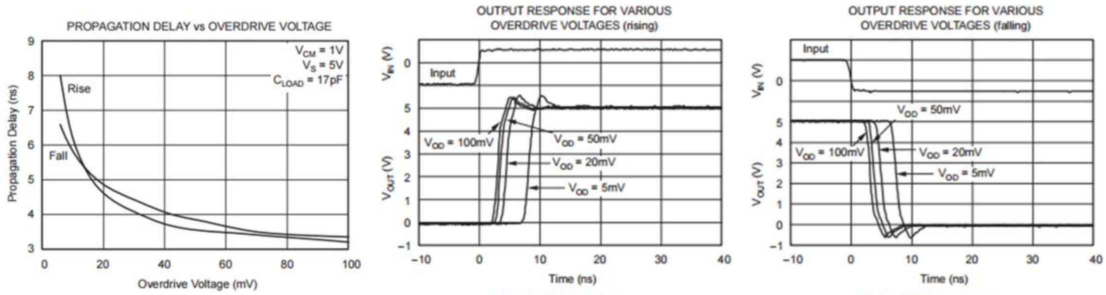
Thankfully, this problem can usually be remedied through proper selection of power supply decoupling capacitors, The LMC7211 data sheet, for example, gives very information on how to select a capacitor for this purpose. Remember to follow good printed circuit board layout techniques which provide a low inductance path for the capacitor.



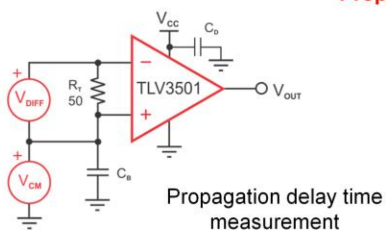
Another common AC consideration for comparators is propagation delay. This is the time required for the comparator output to reach 50% of its final output level when the input changes to 50% of its final input level. Notice that two propagation delays are specified: one for the output transition from low to high, designated $t_{P(LH)}$, and another for the transition from high to low, designated $t_{P(HL)}$.

Besides the propagation delay, a rise time t_R and fall time t_F for the output waveform are also specified. This is the time required for the output to transition from 10% to 90% of its final value. Note that the propagation delay of a comparator can be different for the rising edge and falling edge, due to the sizing and impedance of the output stage transistors.

Input Overdrive vs. Propagation Delay



Prop delay $t_{P(LH)}$ Prop delay $t_{P(HL)}$



Propagation delay time measurement

Temp	Overdrive	Typical	Maximum
25°C	5 mV	7.5 ns	10 ns
-40°C to 85°C			12 ns
25°C	20 mV	4.5 ns	6.4 ns
-40°C to 85C			7 ns

Propagation delay t_{PD} , ΔVin = 100 mV

Texas Instruments 8

The propagation delay time of a comparator is affected by the amount of input overdrive. In this case, overdrive is defined as additional input signal amplitude relative to the reference level applied to the other input. For example, if the reference input is set to 1V, and the signal input is 1.02V, the overdrive level is equal to 20mV.

Overdriving the comparator input results in a reduced propagation delay time. The reduction is limited, but can be significant as the overdrive is stepped from 5 mV to 100 mV. The most significant reductions occur at the lower end of the overdrive range, such as from

5mV to 20mV. The plots on the top of the slide show the change in propagation delay vs. overdrive voltage for the TLV3501.

Maximum Toggle Frequency

From datasheet numbers and lab measurements:

$$f_{toggle} \cong (t_r + t_f + t_{P(LH)} + t_{P(HL)})^{-1}$$

Using **TLV3501** datasheet typical timings:

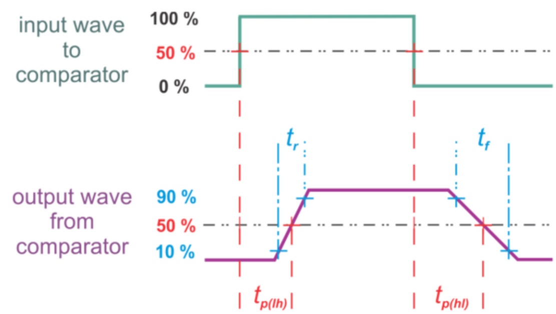
$$f_{toggle} \cong (1.5\,ns + 1.5\,ns + 4.5\,ns + 4.5\,ns)^{-1} = \mathbf{83.3\ MHz}$$

- Datasheet lists $f_{max(toggle)}$ as 80 MHz typical

Using **TLV3201** datasheet typical timings:

$$f_{toggle} \cong (2.9\,ns + 3.7\,ns + 43\,ns + 42\,ns)^{-1} = \mathbf{10.9\ MHz}$$

- Verified in lab to be about 10 MHz



Comparator input to output timing relationships

The final comparator specification we'll discuss in this video is called "maximum toggle frequency," or the maximum switching frequency of the comparator. This specification gives an impression of the overall "speed" of a comparator and can be calculated using the equation shown here. Simply add the rise time, fall time, propagation delay from low to high, and propagation delay from high to low, and take the reciprocal of the result.

For example, if we use the TLV3501 timing parameters, we can calculate an approximate maximum toggle frequency of 83.3 MHz. The data sheet gives a value of 80 MHz, quite close to our calculation.

Taking the TLV3201 as another example, we an calculate an approximate maximum toggle frequency of 10.9 MHz. The data sheet does not specify a value, but lab tests verified that the limit is around 10 MHz.

Thanks for your time!
Please try the quiz.

Texas Instruments 10

That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.