Stability Issues for High Speed Amplifiers – Introductory Background and Improved Analysis (The Signal Sped Up, Insight #5)

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Abstract: Probably no single issue faces more high-speed signal path designers (and supplier support teams) than the risk of instability in higher speed op amps and fully differential amplifiers. Some legacy literature assumes approximations that might not be prudent. Background on how to think about signal path stability issues will be first reviewed. Some detailed improvements in stability simulation approaches will then be presented. More detailed caveats on the 40dB closure rate warnings will then be developed using the transimpedance application circuit as an illustration vehicle. This will be followed up with VFA, CFA and FDA stability hazards "and fixes" in subsequent insights.

Common Sources of Instability in High Speed Signal Channel Solutions

By far the most common instability issues arise from low phase margin is the overall loop gain for these negative feedback amplifiers. There are other, less common, sources that should be considered in special cases – such as,

1. Cascaded high gain amplifiers stages oscillating through a power supply feedback loop.
2. Emitter follower input stage local oscillation through an inductive source impedance – e.g. trace inductance looking out to a grounded input.
3. Internal bias lines finding instability through external capacitive de-coupling with low self-resonant frequencies – arising from poor cap placement with higher trace inductance.
4. Differential I/O stages showing a common mode loop instability (section 8.1.5, ref. 1)

These special cases will not be considered here, but some appear in earlier application notes. (ref. 2).

Finding a sustained, or intermittent, oscillation in EMC, or final board, testing is the wrong place to discover an issue. Actually, finding a sustained oscillation in a signal path design is relatively trivial. Finding a "potential" for instability is far more difficult, but the right place and time to apply the effort – and, the topic for this discussion. These always come down to assessing the "nominal" stage Phase Margin (PM) and then judging the chance of moving down in production and over temperature to an unstable condition. Numerous earlier publications of Loop Gain (LG) analysis establish the framework for this discussion (ref. 3,4,5). There are slight variations in these sources, but they are fundamentally looking for the difference between a -180deg phase shift around the loop at the frequency the LG magnitude drops to "1" (or 0dB) will give the "phase margin". It is rare that an op amp or Fully Differential Amplifier (FDA) application will have good phase margin, but poor "Gain Margin" and we will focus on phase margin here. Some sources simply reverse the polarity of the LG sense to produce a +180deg at DC. This then shows PM directly as it transitions towards 0deg.

Various "rules of thumb" have emerged over time. Those really need to be in the context of the application circuit and what opportunities are available for variation in the direction of reduced phase margin from nominal. Legacy VFA op amp data sheets often would target a nominal 45deg PM at the lowest gain to get a higher reported small signal bandwidth (especially National Semiconductor) along with the nominal 2.3dB small signal response peaking that comes with 45° PM. In more recent device

applications, much lower PM's are sometimes allowed. However, while one source might claim a "min. 30deg phase margin" to be perfectly suitable and safe in the context of a particular source of lower nominal phase margin, some other more aggressive targets like a minimum 20deg nominal PM might be perfectly acceptable when the terms creating that nominal have minimal variation in production or over temperature – and, the effects of that low nominal phase margin are acceptable in the context of the intended application.

Generally, phase margins <55deg will start to show more ringing and longer settling times if the application is pulse response oriented. Really low nominal phase margins in these time domain oriented channels are normally not acceptable unless post filtering places these resonances far into the cutoff band. Similarly, phase margins <55deg will start to show response peaking in frequency domain oriented applications. This is sometimes a secondary effect to an intentional effort to increase the loop gain (improving distortion) at lower frequencies where that peaking at higher frequencies will either be cut off by passive postfilters or can be ignored since that peaking is above the signal "band" of interest. However, if it shifts in production or over temperature into oscillation, it can rarely be ignored!

One important reference point in closed loop amplifier phase margins is that a θ_m = 65.5deg will give a closed loop Butterworth response. Ideally, that 2nd order shape will have no response peaking in the passband but will give a 4.3% step response overshoot. More generally, the ideal mapping from phase margin to response Q, dB peaking, and step response overshoot are shown in Figures 1→3. These are small signal effects where encroaching into an output slew limited response will depart widely from these relationships (ref. 6, 7).

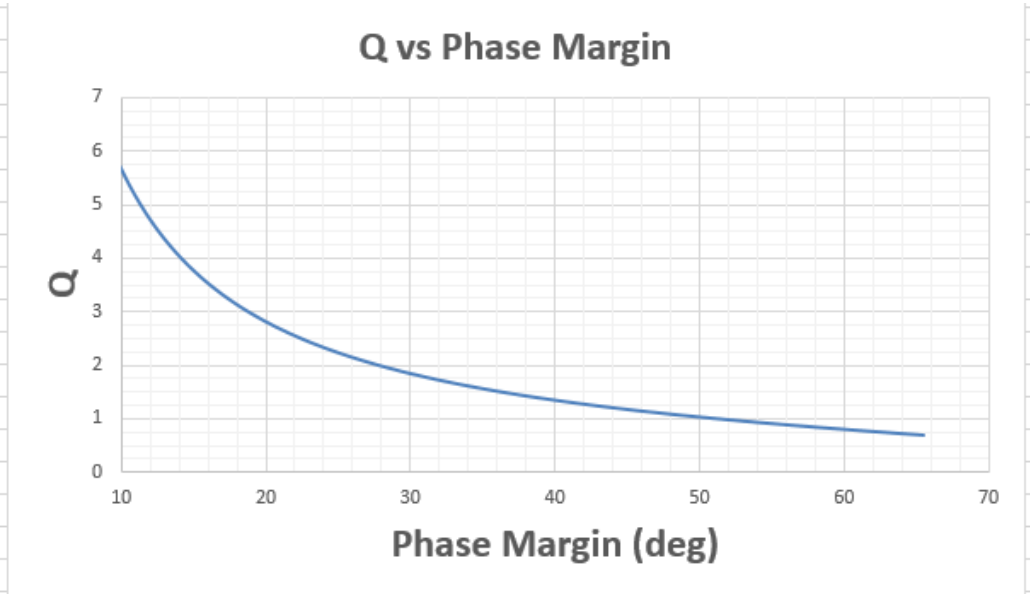

Figure 1. Closed loop response Q vs. LG phase margin.

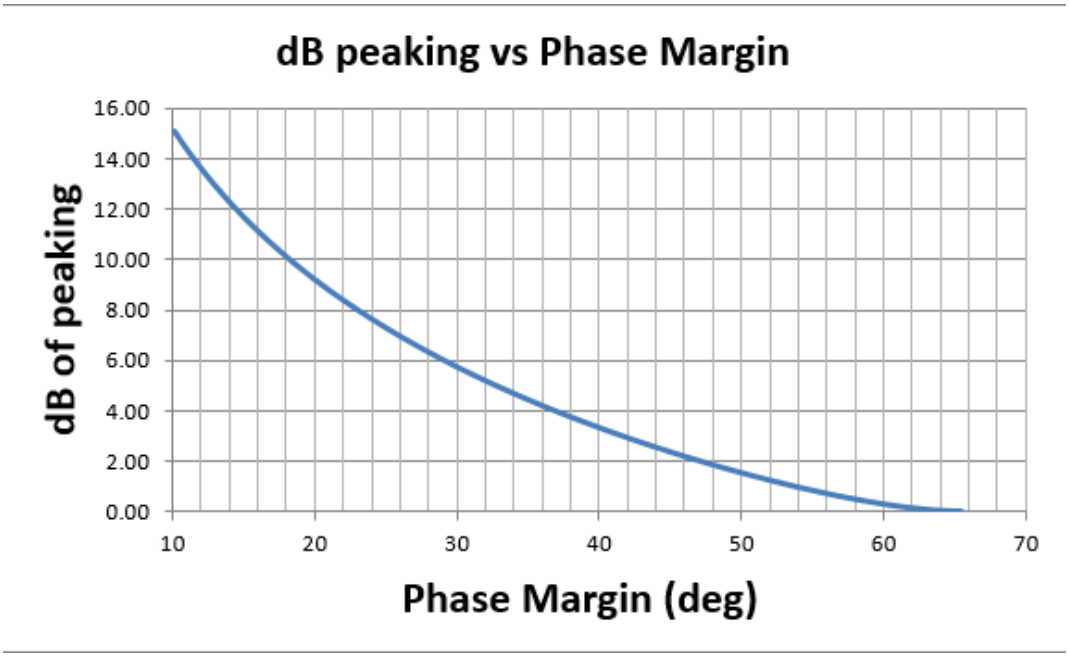

Figure 2. Small Signal (non-slew limited) Response peaking vs. LG phase margin.

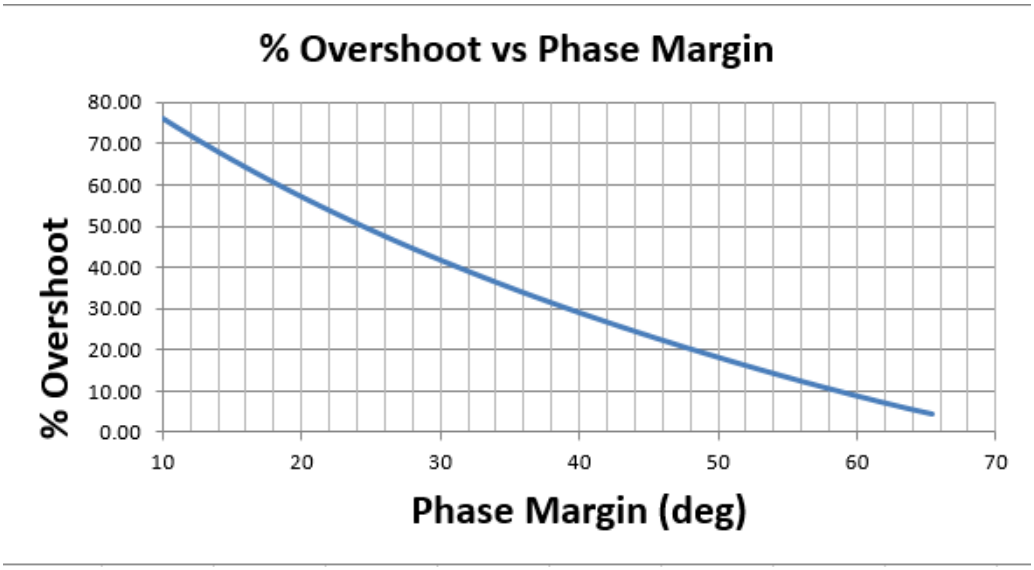

Figure 3. Small Signal (non-slew limited) Step Response Overshoot vs LG phase margin.

One of the more confusing (and rarely discussed) aspects to LG analysis at a particular LG=0dB (F_{xover}) crossover frequency and Phase Margin (PM), what then will be the closed loop Small Signal BandWidth (SSBW)? The commonly reported Gain Bandwidth Product (GBP) idea only applies if the PM=90° (a single pole system). A good approximation to the F_{-3dB}/F_{xover} ratio shown in Figure 4 applies to a 2-pole system. Higher order LG situations depart from this again, but this gets one step closer to explaining the measured SSBW vs gain in VFA devices. This curve goes flat at 1.57X for PM < 35°. Going back to the

nominally Butterworth shape with θ_m=65.5° will predict an $F_{-3dB} = 1.55*F_{xover}$ – far higher than the simple GBP concept would predict.

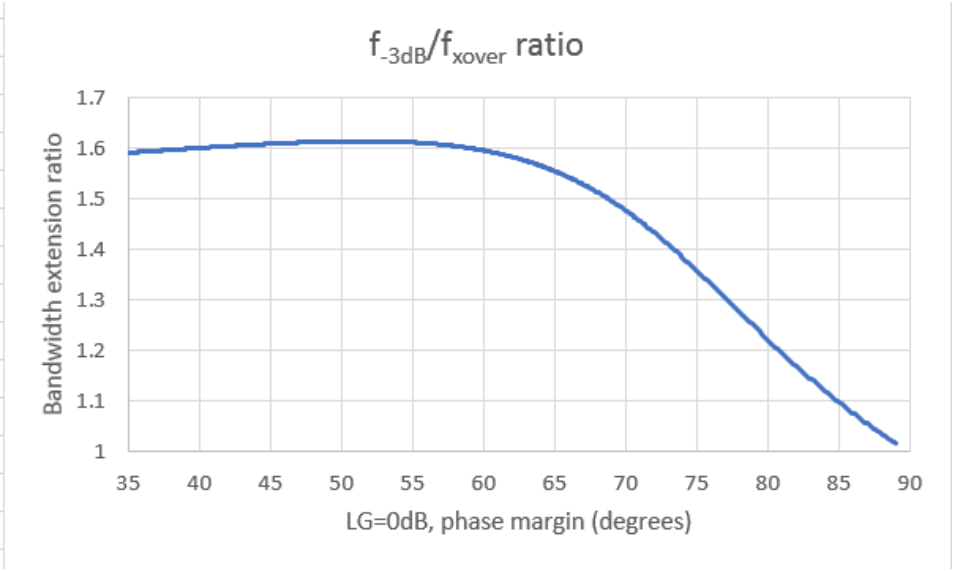

Figure 4. SSBW extension from LG=0dB F_{xover} vs Phase Margin at Crossover.

An op amp or FDA will get into a lower phase margin condition due to added poles around the loop (kind of by definition). These most commonly arise from capacitive loads interacting with the open loop output impedance or capacitance on the device feedback node(s) introducing a feedback pole in conjunction with the feedback impedance. More recently, devices with lower nominal phase margin, and highly reactive open loop output impedance characteristics, increase the risk of low nominal phase margin. Sometimes, the intended application circuit can also create a low phase margin condition that will require attention. But first, what methods can be used to estimate nominal phase margin in simulation?

Simulation Approaches to Estimating Nominal Phase Margin.

A signal path that is already oscillating has one set of tools to locate the suspect loop. But once isolated, and for the wider range of circuits with low (but not oscillating) phase margins, it is normally necessary to then go into simulation to prove paths to increase the phase margin if needed. At that point, the accuracy and feature set in the vendor models become paramount. These models have improved over time where the key elements required to have some hope of efficacious Loop Gain (LG) phase margin estimates include –

1. Parasitic input impedance (normally a common mode and differential mode RC network)
2. Open loop gain and phase from the error signal to the output voltage – sometimes this should be no load initially as the open loop output impedance will be added separately. The dominant open loop pole setting the GBP is critical, but no more so than the correct gain and phase near A_{ol}=0dB.
3. Open loop output impedance (Z_{ol}) over frequency. This has received a lot of attention lately (ref.8), and is indeed critical to accurate PM estimates. It seems many of the older amplifier

models (device library, ref. 9) have a very simplified resistive only Z_{ol} model that might not be enough for accurate PM estimates in more complicated load and/or feedback network conditions using higher frequency devices.

There are certainly multiple approaches to arrive at an op amp or Fully Differential Amplifier (FDA) LG simulation. The most thorough approaches apply a 2-pass simulation with either the loop broken (Rosenstark's, ref. 10) or with two inside the loop simulations (Middlebrook's, ref. 11). A recent discussion compares these two (ref. 12). Those approaches all note that if the signal injection point is widely different in impedance looking each direction, a single simulation will be enough. This is the approach most application teams take where then there is some disparity in where the loop is broken. There are some concerns that breaking the loop for simulation gets into DC operating point issues – those can be easily handled as shown here. Some legacy material using this approach had simplifying assumptions that might not be as effective using modern higher speed device models (ref. 13). Both this older approach, and a slight modification that will improve the accuracy, will be shown using a very recent device model for the OPA837 (ref. 14).

It is very typical for suppliers to illustrate a LG phase margin simulation with fairly benign external circuit conditions. It is not uncommon for end systems to immediately depart from those towards lower phase margin designs in the course of setting up the desired signal path characteristics. A fairly straightforward closed loop design using the OPA837 is shown in Figure 5. Here, an initial gain of -1V/V is bandlimited at 796kHz using a simple 100pF feedback capacitor. Combined with even a modest capacitive load (like a scope probe), this will immediately produce a low phase margin design – primarily due to the very reactive open loop output impedance (shown in Figure 6) for the OPA837. Setting that feedback C_f to 0pF shows the wideband result with minimal peaking in Fig. 5.

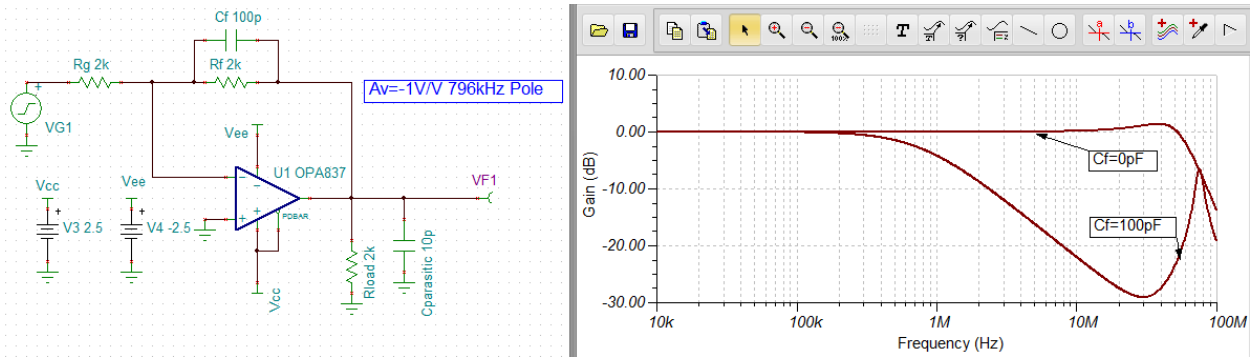

Figure 5. Closed loop gain of -1V/V with 796kHz feedback pole and 10pF capacitive load.

The noise gain (NG) in this circuit starts at 6dB (NG of 2V/V) at DC, then transitions to 0dB as the feedback capacitor shorts out. The resonance with C_f= 100pF at 66MHz arises from the open loop output impedance interacting with the feedback C_f. To extract the open loop output impedance (Z_{ol}) within the OPA837 model, use the technique of very high L & C in Figure 6 to setup the DC operating point. For the AC simulation, that L opens up and the C shorts out leaving an open loop model sitting at a mid-supply DC operating voltage. The odd LC values reduce numeric chatter while the small series R with the feedback L helps find a DC operating point in some cases. The complicated Z_{ol} shape of Figure 6 has started to show up in rail-to-rail output (RRO) devices but has only recently been captured in the

vendor models. Many older models have a simple fixed resistive Z_{ol}. That might be correct for higher quiescent current bipolar non-RRO output designs but might not be for RRO type devices. Use the approach of Fig.6 to evaluate the model for Z_{ol} in the device you are using.

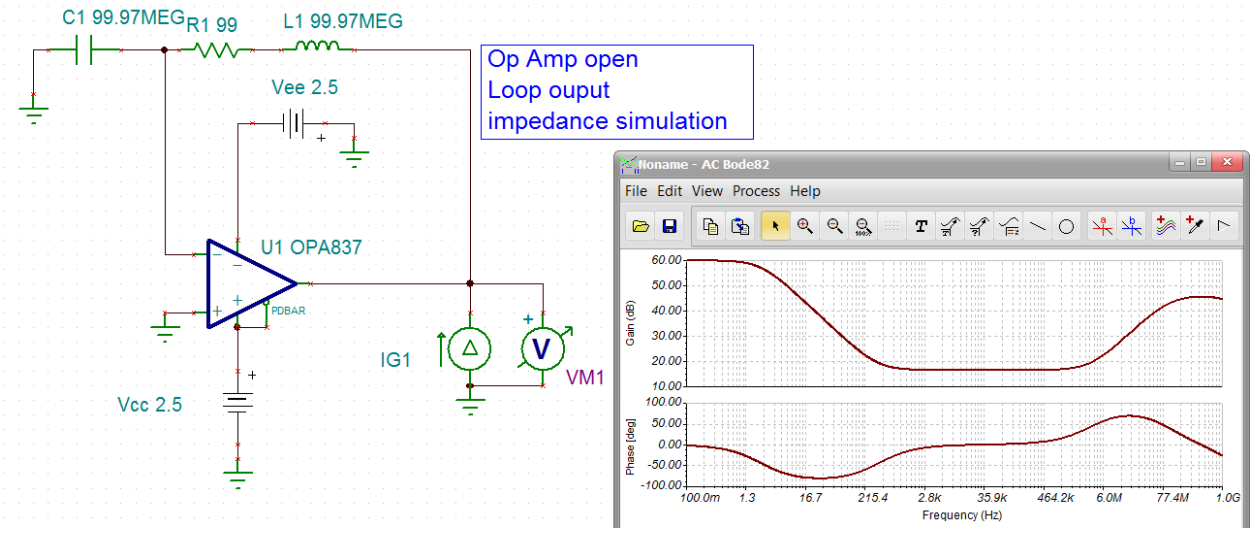

Figure 6. Open loop output impedance for the OPA837 – note the gain scale is dBohms.

To test if this effect is dominant, modify the schematic of Figure 5 to isolate the Z_{ol} from the load and feedback network using a dependent source. Doing this removes the resonance effect in fig. 7.

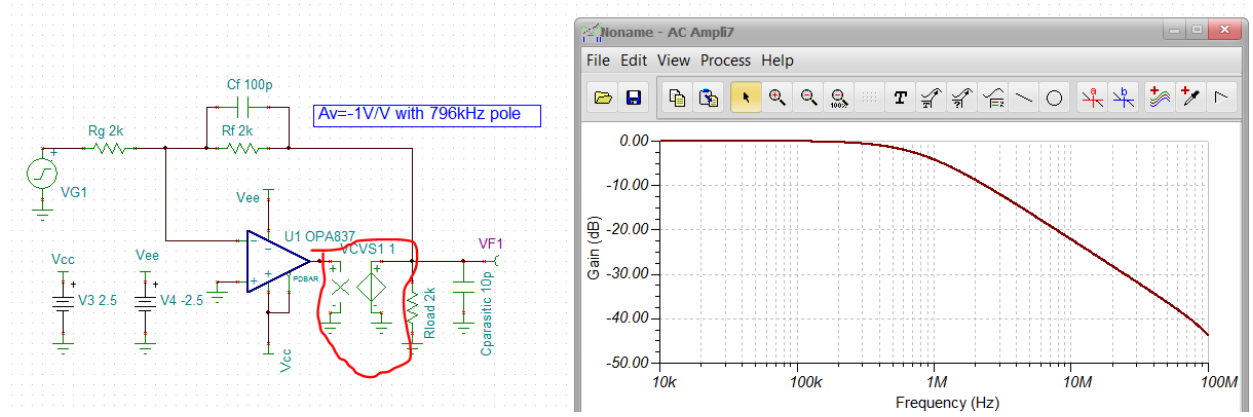

Figure 7. Inverting gain of -1V/V with bandlimiting and isolated Z_{ol}.

Simply adding a bandlimiting capacitor in the feedback path has pushed this design into an obviously low phase margin condition. The next step would be to set up for a phase margin simulation to assess where we are before moving on to testing improvement techniques. An older technique will be shown first with a slight improvement to follow.

One approach commonly shown (ref. 15) breaks the loop going into the feedback network then injects a signal back into the feedback path and sensing the Loop Gain (LG) back around to the output of the op amp. Figure 8 shows this approach where it is estimating a 30deg phase margin for the example of Fig.

5. The polarity of VM1 is showing the phase shift around the loop. Starting at -90deg from the op amps' dominant pole at lower frequencies it shifts down to -150deg at the LG=0dB xover point. That is then subtracted from -180deg to get that 30deg phase margin. Reversing this sense voltmeter polarity would add 180deg to what is plotted allowing the "phase margin" to be read off directly.

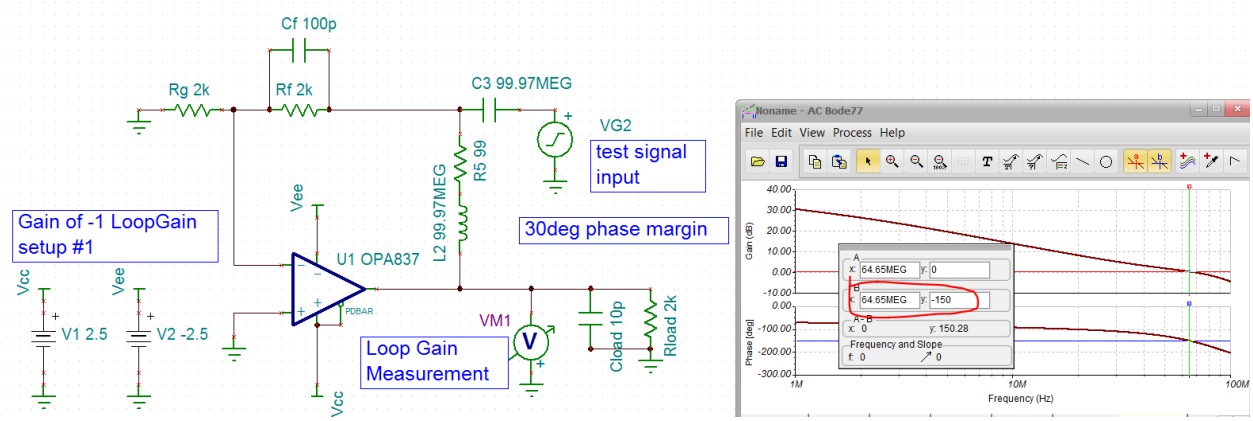

Figure 8. Loop Gain simulation setup #1 - breaking the loop at the output.

This approach captures most of what we are after and is very often adequate to the task. The models' Z_{ol} correctly sees the load and the feedback network correctly sees the inverting input parasitic capacitance in the model before it gets into the Aol response of the op amp. However, this legacy approach isolates the feedback impedance from the Z_{ol}. Often, that is not an issue if the feedback network is purely resistive and/or the Z_{ol} is a simple low R model. In the more general case, the setup of Figure 9 is slightly more accurate. Here, the loop is broken at the input where the output Z_{ol} is connected to both the load and feedback network. The only new requirement is to manually place RC elements for the inverting input impedance at the summing junction where the LG measurement is made. This more accurate approach shows a very low 20.3deg phase margin where here the VM1 polarity has been reversed to allow "phase margin" to be read off directly. The lower phase margin vs. Fig. 8 is a direct result of the open loop Z_{ol} seeing the added reactive loading of the feedback network. Reducing Cf to 0pF in this test simulation increases the phase margin to 52deg. Figure 2 predicts a 1.22dB peaking for that phase margin, closely matching the 1.37dB peaking in the Cf=0pF curve of fig. 5.

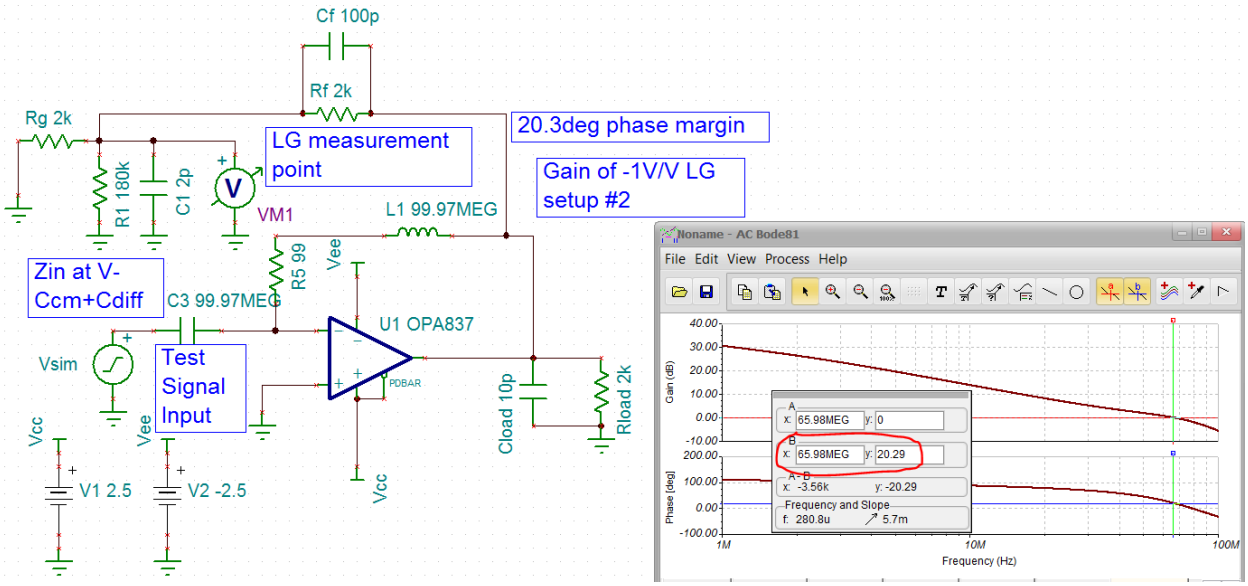

Figure 9. Loop Gain simulation setup #2 breaking the loop at the input.

It would seem this setup #2 might be the more accurate approach. And, going back to the two pass approaches, the input break point would seem to give a wider divergence in impedance looking the two directions at the break. This approach will be used in subsequent insights to show paths to improve PM, but first -

How hazardous is a 40dB closure rate at loop gain crossover – really?

Another common "rule of thumb" is that a 40dB closure rate between the one pole rolloff of an op amps' A_{ol} curve and the noise gain curve should be avoided at all costs (ref.16). There is good reason for this concern, but it is not 100% for sure a recipe of instability. As correctly noted in ref. 16, a 40dB rate of closure can be associated with a PM<45deg, but that is not automatically unacceptable as will be shown using a simple transimpedance amplifier design.

The transimpedance amplifier is probably the simplest case leading to a potential 40dB closure rate in the LG. Here, the source is intentionally a photodiode capacitance with a simple feedback resistor setting the gain. As such, the NG starts out at 1V/V then rises with the feedback pole caused by the feedback R to source C. That feedback pole is inverted to a zero for the NG. The task here is to set a feedback capacitor to set a pole location to achieve the desired closed loop peaking (Q).

First, transimpedance designs need the true Gain Bandwidth Product (GBP) for the op amp under consideration. That number is the "projected" 1pole rolloff intersection of the A_{ol} curve with 0dB. Figure 10 shows an example A_{ol} simulation using the "20MHz" OPA725 (ref. 17).

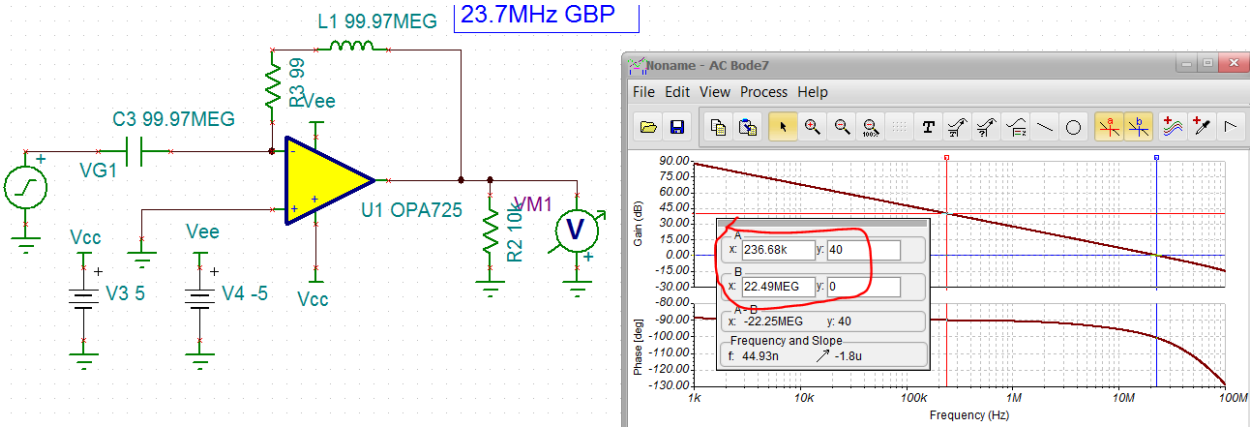

Figure 10. A_{ol} extraction for the OPA725 using the datasheet specified 10kΩ load.

This A_{ol} simulation is highlighting two magnitudes on the A_{ol} curve. The first, the 40dB gain number, is an easy way to "project" to the single pole intersection by multiplying that frequency times 100X – this gives the correct number to use in design to get good simulation matching. It is not uncommon (especially as the amplifier speed increases) to report the A_{ol}=0dB frequency as the GBP. As is often the case with higher frequency poles in the A_{ol} response (the phase in fig. 10 shows this model has them), that A_{ol}=0dB frequency is lower (22.5MHz here) than the projected 1pole crossover. It is a very common mistake to use this number instead of the true GBP in both datasheets and design. Another common mistake in transimpedance design (ref. 18) is to use the closed loop gain of 1 bandwidth instead of the GBP. This will give completely erroneous results as suggested by the relationship in Fig. 4.

The solution for the transimpedance feedback capacitor in ref. 18 is solving to place the feedback pole at the exact intersection of the Bode plot projection of the rising noise gain zero and the falling A_{ol} curve. That intersection is the F_o for the closed loop response and given by the geometric mean of the zero frequency and the (correct) GBP. A useful approximation for the closed loop transimpedance response shape is that its Q is the ratio of the feedback pole ($P_1=1/(2\pi R_f C_f)$) to the F_o (ref. 19). Executing that solution for C_f in Figure 11 is placing the feedback pole exactly at F_o indeed gives approximately the response peaking for a Q=1.

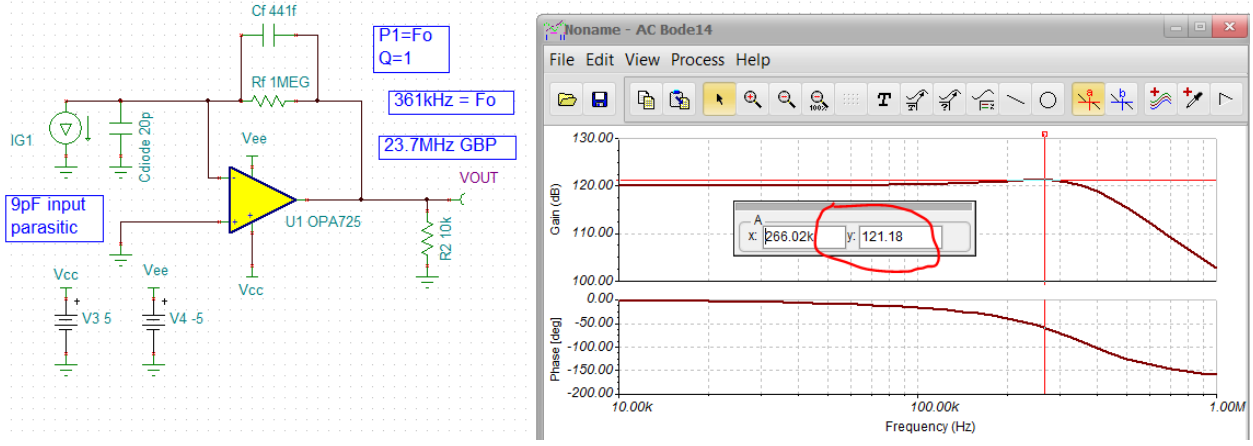

Figure 11. 1Mohm transimpedance gain from a 20pF source capacitor including 9pF input parasitic.

This solution for C_f is coming in a few steps using some simplifications from ref. 19. Working in Hz, first the F_o, or resonant frequency of the closed loop response, is the geometric mean of the noise gain zero and the true GBP – this is also the frequency of intersection for the projected one zero NG with the one pole A_{ol} shown in eq. 1 where C_s is the total capacitance on the inverting node.

$$F_0(Hz) = \sqrt{\left(\frac{1}{2\pi R_f C_s}\right) GBP} \qquad \text{Eq. 1}$$

Then using the simplification that the closed loop Q is approximately the ratio of P_1/F_o gives Eq. 2 where P_1 is the feedback pole.

$$Q \approx \frac{\left(\frac{1}{2\pi R_f C_f}\right)}{F_0} \qquad \text{Eq. 2}$$

Substituting F_o into the equation for Q and solving for C_f gives Eq. 3. Setting Q=1 here will match ref. 18 (eq.1).

$$C_f = \frac{1}{Q}\sqrt{\frac{C_s}{2\pi R_f GBP}} \qquad \text{Eq. 3}$$

Targeting a Butterworth response shape with Q=0.707 will give an Eq. 3 here that matches the transimpedance design discussion in the OPA725 data sheet (ref. 20, eq. 1).

To confirm the phase margin in this initial Q=1 design, use the LG phase margin extraction shown above. Figure 12 shows a PM= 51.8deg that maps to a Q=1 in Fig. 1. Here, VM1 is rotated to allow the PM to be read off directly.

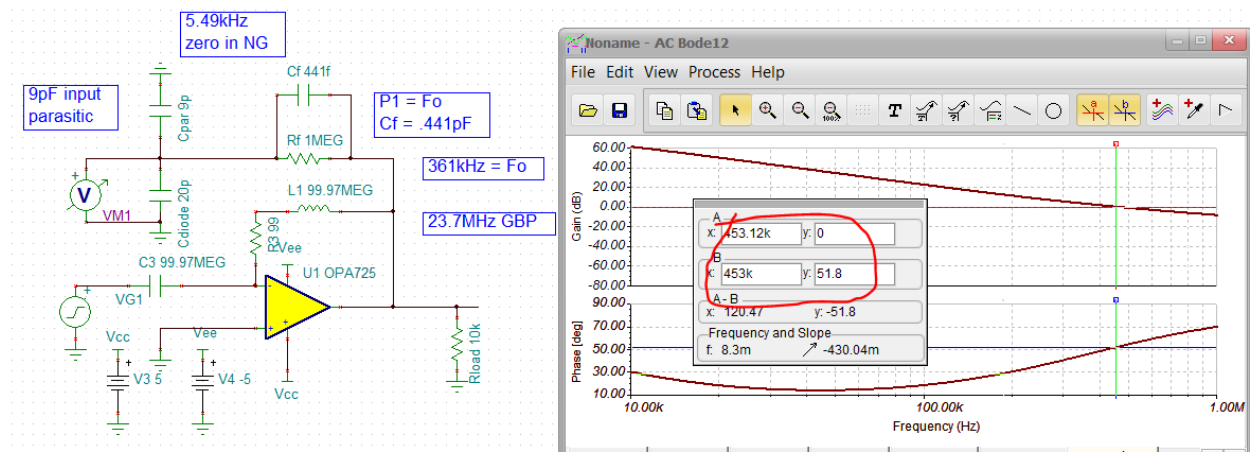

Figure 12. LG plot for transimpedance design of Fig. 11 showing phase margin

Going on to show the open loop gain with the NG separately gives the curves in Fgure13. The noise gain here is derived by simulating the response of the feedback network then inverting the polarity and

subtracting the phase from the Aol phase. Here, the crossover (NG = $A_{ol)}$ occurs with -128deg phase around the loop.

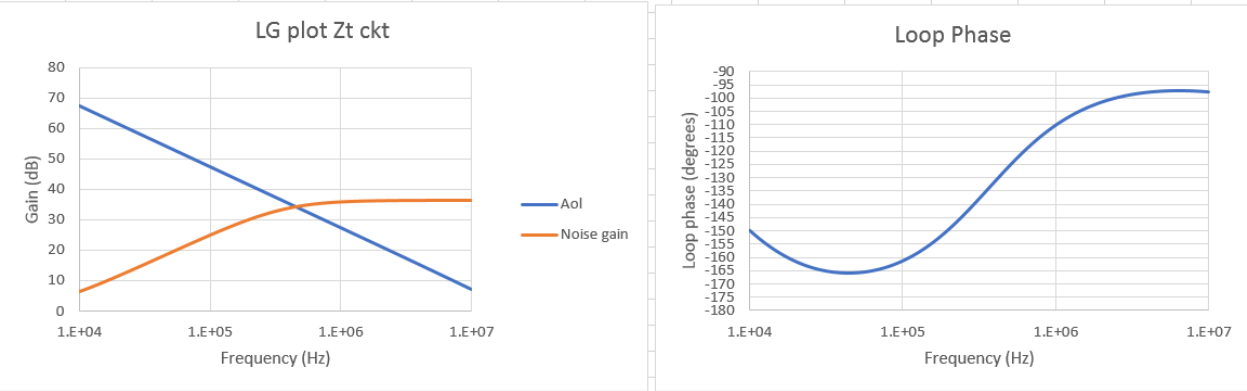

Figure 13. Open Loop gain with noise gain for the feedback pole at Fo in Figure 11.

This example shows a closure rate slightly below 40dB/dec and is certainly stable. However, what if this stage was intended to be part of a multistage active filter where a higher Q was a design goal in this stage? For instance, cutting the feedback capacitor in ½ will change from this initial Q of 1 to a Q=2 by moving P_1 out 2X. The closed loop response indeed hits the correct Q=2 peaking of 6dB as shown in Figure 14.

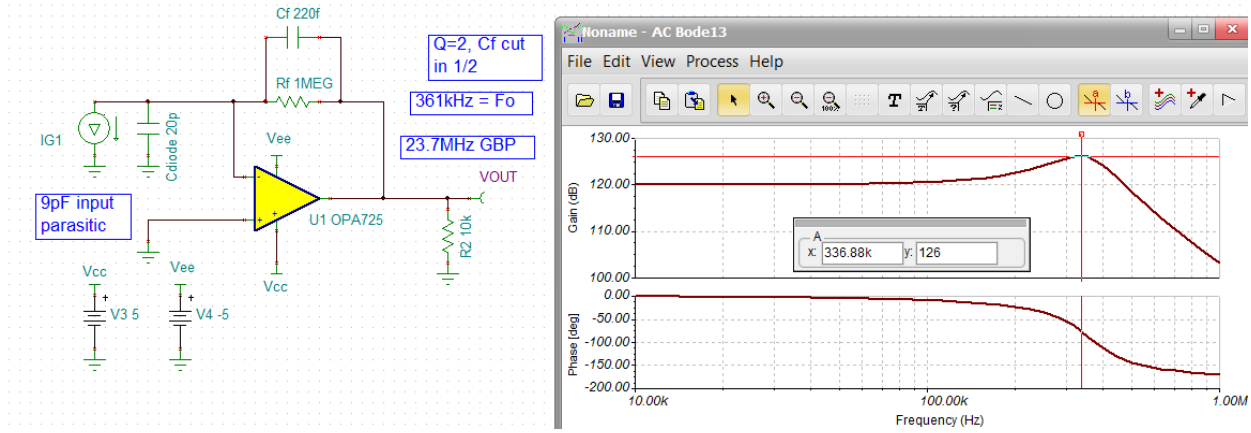

Figure 14. Doubling the feedback pole by cutting C_f in ½ to get a Q=2 design.

Repeating the LG simulation in Figure 15 shows the expected phase margin near 28deg per Fig. 1 to hit a Q=2.

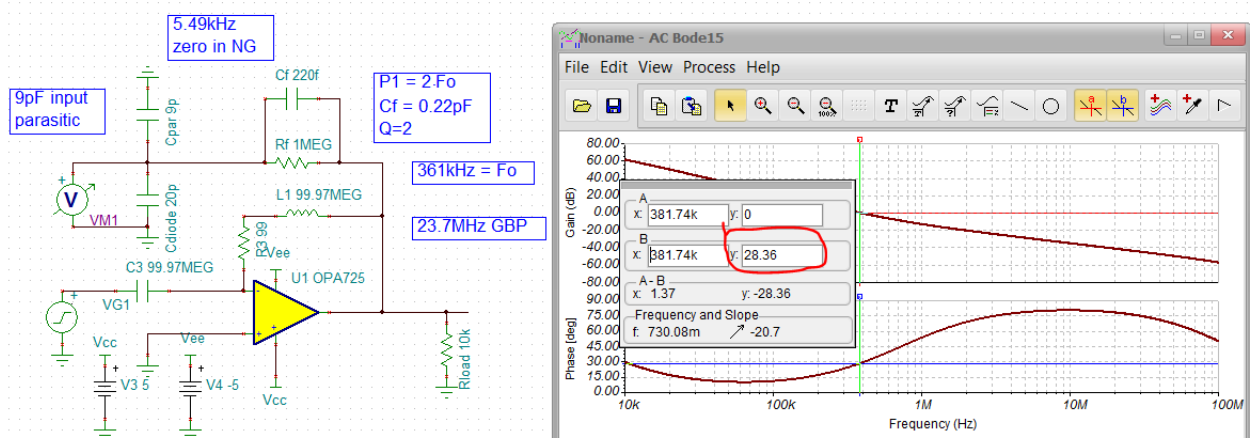

Figure 15. LG simulation with feedback pole moved out 2X giving a Q=2.

And then regenerating the separate A_{ol} and Noise gain plots with this 2X higher feedback pole gives this result where the magnitude closure rate is in fact 40dB/dec in Figure 16 with -152deg around the loop at LG=0dB xover.

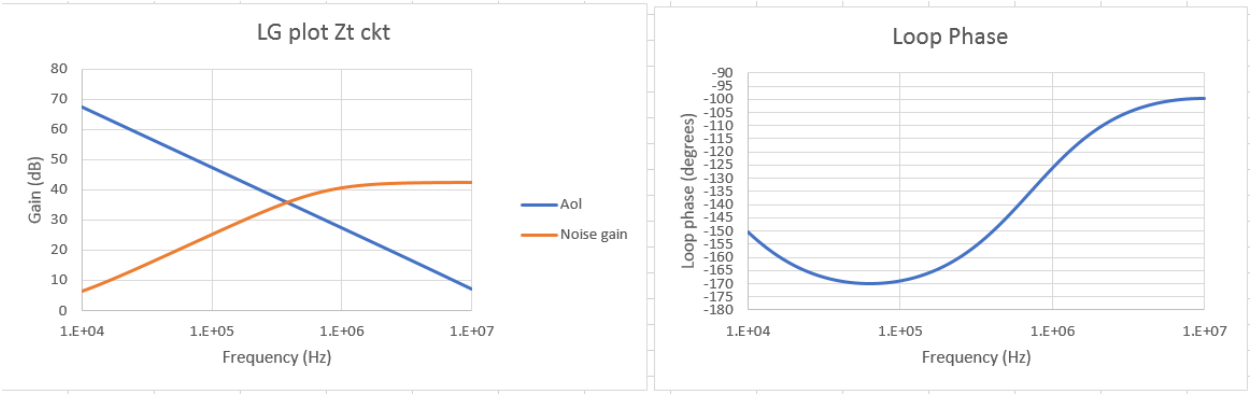

Figure 16. Open Loop gain with Noise Gain for the feedback pole at 2*Fo in Figure 14.

While this might look a little scary from a 40dB/dec closure rate perspective, this is in fact hitting the predicted 28deg phase margin to intentionally produce a Q=2 (6dB peaking) stage. Yes, a 40dB/dec closure rate should induce some caution, but it can also yield stages that might prove useful as shown here. This example will of course have the variation in the op amp's GBP to consider in PM variation. The more general point is that, while a 40dB/dec closure rate does give PM<45deg, that might be ok in the application - especially if the elements that might give PM variation are more controlled than in this simple example.

These examples also show (for the 2 pole A_{ol} and the simple Z_{ol} inside the OPA725 model) the LG phase margin to closed loop response shapes match exactly what might be expected from Figures 1&2. It appears this approach to loop gain extraction works pretty well and will form the basis for subsequent insights on stability. Up next - common high speed VFA op amp sources of low phase margin and fixes!!

Stability issues in high speed amplifier references

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