Stability Issues and Resolutions for High Speed Fully Differential Amplifiers (FDA's), Insight #8

The popular FDA comes in both Current Feedback (CFA) and Voltage Feedback (VFA) variants. The CFA versions tend to be used in AC coupled applications where their great full power bandwidth can be used to advantage while their poor DC precision will have no impact. The VFA versions emerged first (ref. 1) and have by far the largest representation in these product families. Early developments crossed many process nodes to deliver a range of higher voltage, slower, devices then on into >1GHz 5V supply versions (ref. 2). The most recent VFA FDA's focus on lower power, precision, solutions more aimed at SAR and delta sigma ADC support. Those will be focus in this FDA stability discussion - but the concepts are backward compatible to the earliest VFA FDA's.

Setting up for a Current Feedback FDA Loop Gain (LG) simulation.

Similar to the CFA op amp LG simulation approach (ref. 3), the key is to break the loop at the input, inject a test current signal, then trace the loop through the amplifier's internal forward "transimpedance" path and then back into the differential low impedance inputs as a "current feedback" while placing their differential input impedance in the sense path. The feedback is always differential, but the application circuit could have either single ended or differential inputs. A single ended stimulus will bring the internal common mode loop dynamics into play. Since those bring in another level of modeling accuracy, and the models appear uneven in their treatment of this loop, a simpler differential input condition will be the focus here using balanced supplies and a centered common mode control at ground. While there are relatively few CFA based FDA's, these do bring an unmatched level of slew rate to the available FDA universe as shown in Table 1.

Table 1. Current feedback based fully differential amplifiers

		Total Operating										
		Supply Voltage Range	Descending SSBW									
Supplier	Device	Min Vs	Max Vs	SSBW @ Gmin (MHz)	Gmin (V/V)	Slew Rate (V/µsec)	Icc Max/Ch (mA)	Vn_flatband (nV/√Hz)	Vos Max (mV)	Io (mA) (≈min. linear)	Output Headroom (V)	Part Description
NSM	LMH6554	4.7	5.3	2800.0	1	6200	57.0	0.9	16.000	120	1.100	2.8GHz Ultra Linear CFA Fully Differential Amplifier
ADI	ADA4927-1	4.5	11.0	2300.0	1	5000	22.1	1.4	1.300	65	1.200	Ultralow Distortion Current Feedback Differential ADC Driver
NSM	LMH6552	4.5	12.0	1500.0	1	3800	25.0	1.1	16.500	80	1.150	1.5GHz Fully Differential Amplifier
NSM	LMH6553	4.5	12.0	900.0	1	2300	33.0	1.1	5.000	100	1.300	900MHz Fully Differential Amplifier with Output Limiting

Select the fastest LMH6554 (ref. 4) for simulation testing where its model is transistor based as opposed to a lumped element macromodel. First, the open loop differential input impedance is required and can be extracted using the setup of Figure 1.

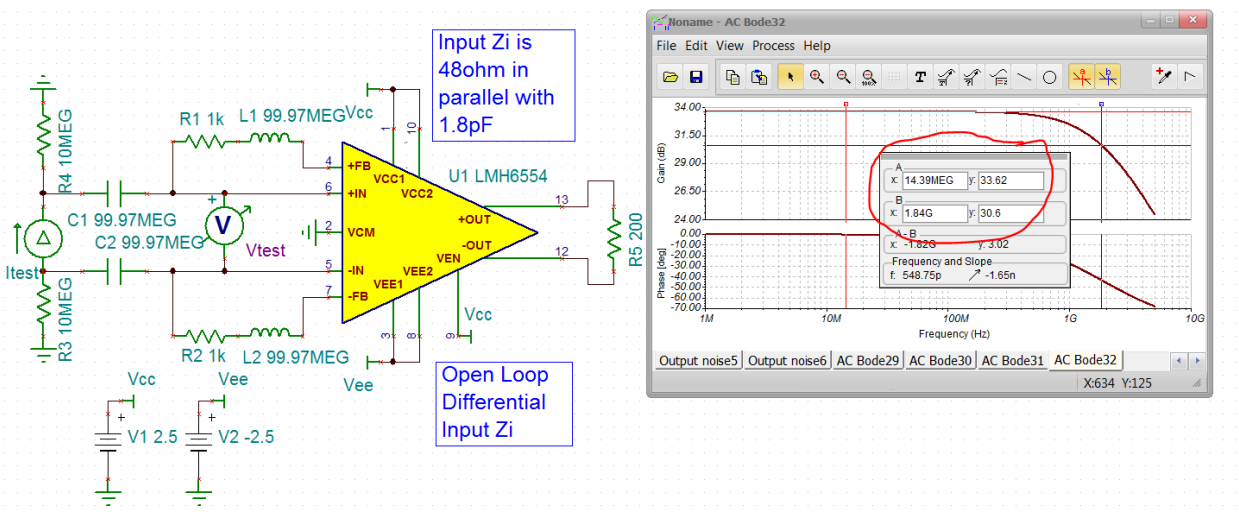

Figure 1. Extracting the open loop differential input impedance for the 2.8GHz LMH6554 FDA.

This dBohm plot is showing a low frequency differential input impedance of 48Ω with a -3dB frequency indicating a 1.8pF in parallel. (notes, this simulation showed a lot of numerical chatter that was resolved by switching to a Davis's KLU matrix solver under the Analysis "options" in TINA (ref. 5), the summing junction input pins are labelled backwards in the current TINA symbol for the LMH6554).

Moving on to a Loop Gain (LG) phase margin simulation, break the loop at the input pins, injecting a differential input current, then measure the resulting differential input error current through that input impedance model as shown in Figure 2. Here, the input error current sense ammeter reads phase shift around the loop where a -128deg at the 1.7GHz LG=0dB crossover indicates 52deg phase margin.

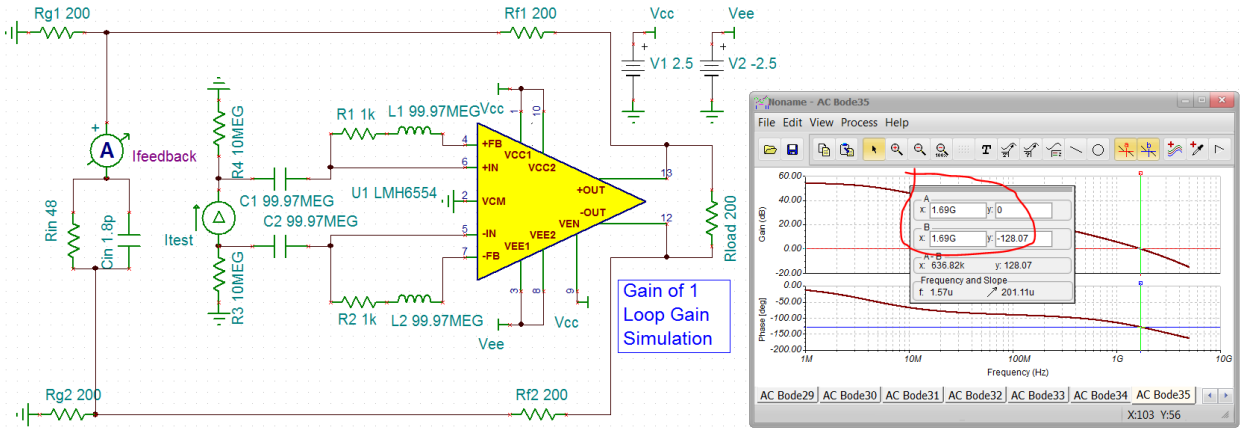

Figure 2. Nominal gain of 1 LMH6554 LG simulation

Using the 1.6X F_{-3dB} bandwidth multiplier (fig. 4, ref. 6) from this 1.7GHz F_{xover} predicts a 2.7GHz SSBW – closely matching the reported 2.8GHz (ref. 4).

Tuning in the Cload Driver Solution Using the LMH6554

Similar to the CFA op amp case (ref. 3), the current feedback FDA will have an open loop output impedance that will introduce an added pole in the loop if a capacitive load is added to the output. Normally, that capacitance will be either a layout parasitic, part of a postfilter, or an ADC input load. Using a similar approach (ref. 3) to simulating the open loop differential output impedance showed a remarkably low 1.9Ω. This certainly begs the question if that is correct and, if so, suggests a closed loop output stage. If accurate, this small Z_{ol} will have little impact on the loop phase margin as cap loads are added. Just like the CFA op amp capacitive load case, the response to the cap load is combination of whatever might be happening across the output pins then rolled off by the RC filter to the load. The recommended curves from the LMH6554 datasheet (fig. 3) show what appear to be relatively high R_o's for such low open loop output impedance. This may be a consideration for a secondary effect (like local oscillations in a closed loop output stage), but at this point can only depend on the model accuracy and proceed.

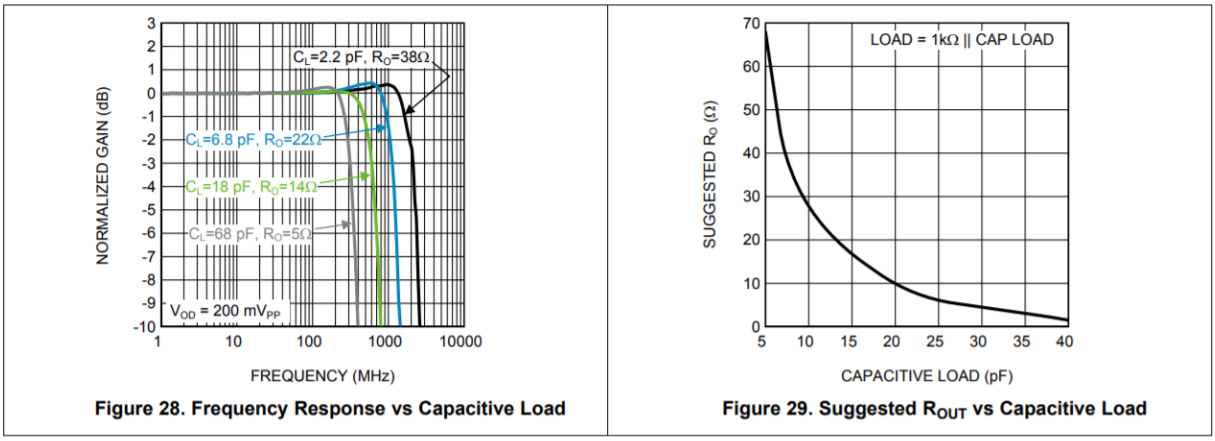

Figure 28. Frequency Response vs Capacitive Load

Figure 29. Suggested R_{OUT} vs Capacitive Load

Figure 3. Response shapes and recommended external Ro vs capacitive loads.

These are at a gain of 1 with 200Ω resistors where the responses to the output pins and load are shown using the TINA simulation model in Figure 4 for the 18pF case. The lack of peaking at the output pin suggests quite a lot of phase margin with this initial setting. The higher than necessary R_o also gives the relatively low 286MHz F_{-3dB} to the load vs the 1.1GHz across the output pins. It does appear this loading has dropped the simple 200Ω load SSBW of 2.8GHz quite a lot.

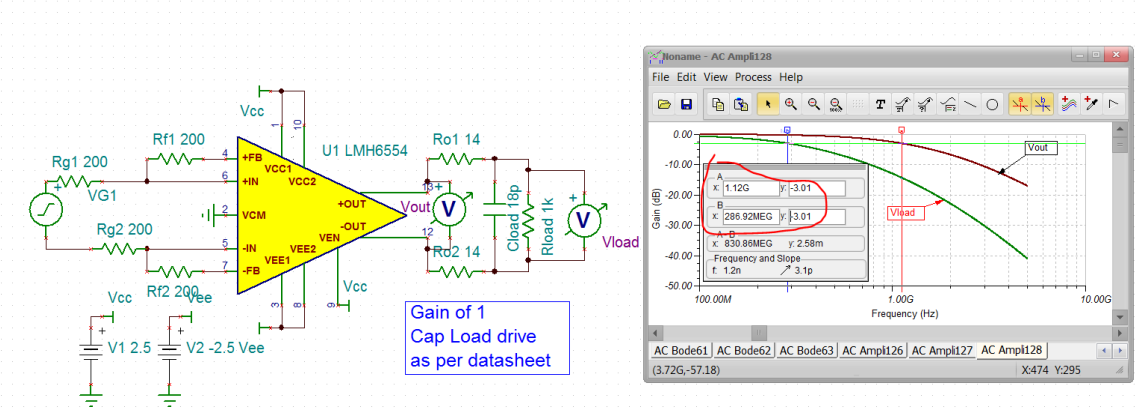

Figure 4. Recommended Ro case with 18pF load capacitance

Repeating the fig. 2 Loop Gain (LG) test with this new load gives the 52deg phase margin of Figure 5. Also, this crossover frequency far exceeds the closed loop bandwidth indicating some other factor is coming in to bandlimit the closed loop result. The open loop output impedance also showed an inductive characteristic above 1GHz and it is likely this is contributing to the bandlimiting.

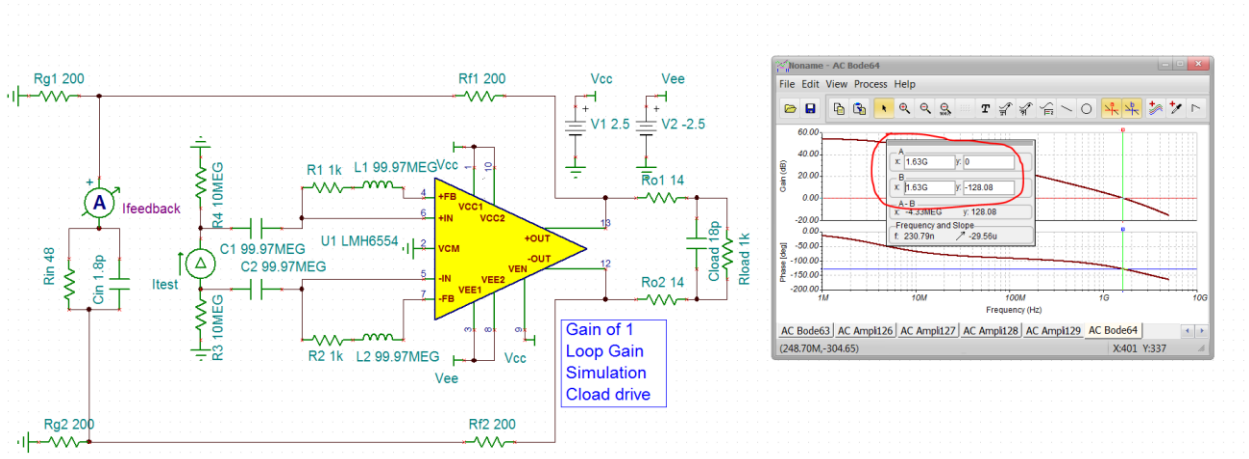

Figure 5. LG Phase Margin (PM) for the cap load test of fig. 4.

At least at the model level, this seems excessively conservative and lower R_o values should be possible extending the bandwidth to the C_{load} over what appears in fig. 4. It proved actually difficult to force peaking at the output pins with value changes. Reducing both the R_o and the feedback/gain resistors should both be moving in the direction of lower phase margin and bandwidth extension at the load. Figure 6 shows an example with only 3Ω R_o and the R's reduced to 150Ω where 43deg loop phase margin results.

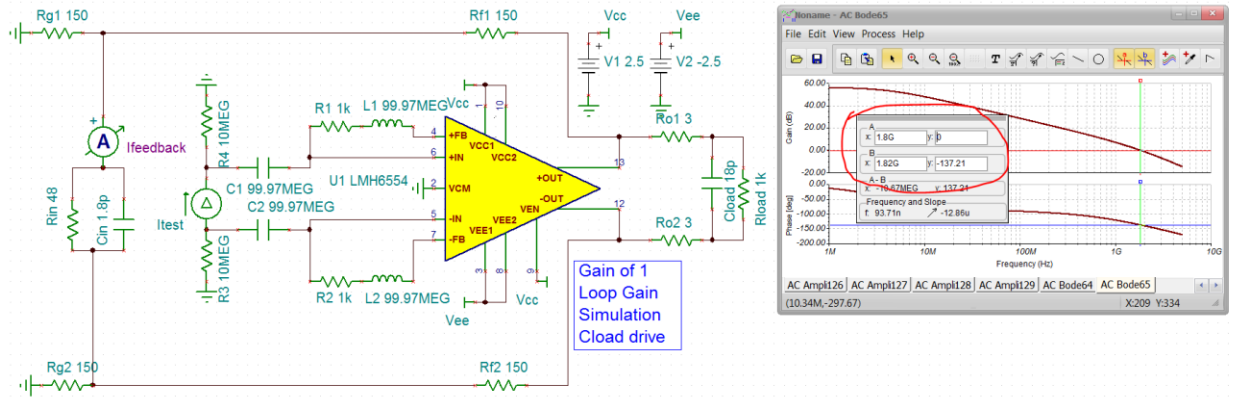

Figure 6. Reduced phase margin to extend bandwidth at the capacitive load.

Reducing the amplifier R's will also reduce the noise while the lower R_o will greatly extend the SSBW to the capacitive load as shown in the closed loop simulation in Figure 7.

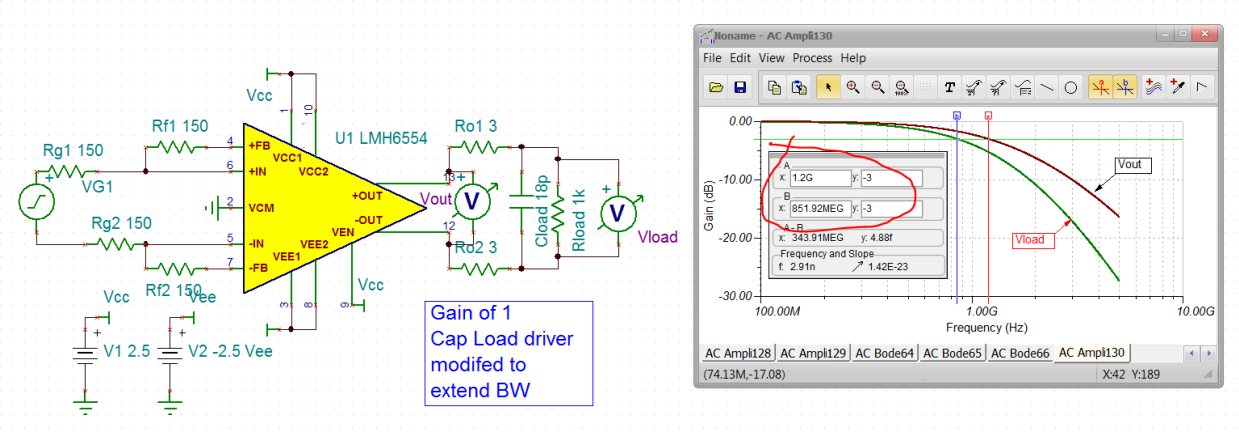

Figure 7. Bandwidth extended cap load driver

Still no peaking at the output pins but the SSBW to the cap load is vastly extended to 850MHz from the datasheet condition of 286MHz. To the extent this model is accurate, this approach can offer considerably more frequency range than Figure 3 suggests. The same ideas presented in ref. 3 can be applied here to adapt what are normally VFA only application circuits to CFA based FDA's.

New phase margin issues using RRout high speed VFA FDA's.

Starting from a wide range of very high- speed FDA's (ref. 2) focused 1st on driving high speed pipeline ADC's, the more recent introductions have aimed at lower speed devices with much improved DC precision, lower power, rail to rail outputs, and negative rail inputs (ref. 7) to support single supply differential drivers to SAR and delta sigma ADC converters. Table 2 shows the single channel, precision, voltage feedback FDA's available in descending SSBW at gain of 1V/V.

Table 2. High Speed, Precision, RRoutput FDA's

		Total Operating Supply Voltage (Vs)		Descending SSBW											
Supplier	Device	Vs (min) (V)	Vs (max) (V)	SSBW @ Gmin (MHz)	Gmin (V/V)	Slew Rate (V/µsec)	Icc Max/Ch (mA)	Vn_flatband (nV/√Hz)	Vos Max (mV)	Ib Max (V+pin) nA	Io (mA) (≈min. linear)	R-R In	R-R Out	Output Headroom (V)	Part Description
TI	THS4541	2.7	5.4	620.0	1	1500	10.5	2.2	0.450	1.30E+04	35	-Vs	Yes	0.200	NRI, RRO Precision 850Mhz Fully Differential Amplifier
ADI	ADA4940-1	3.0	7.0	260.0	1	95	1.4	3.9	0.350	1.60E+03	46	-Vs	Yes	0.070	Ultralow Power, Low Distortion, Fully Differential ADC Driver
TI	THS4551	2.7	5.4	150.0	1	220	1.4	3.3	0.175	1.50E+03	45	-Vs	Yes	0.200	Low Noise, Precision, 150MHz Fully Differential Amplifier
MChip	MCP6D11	2.5	5.5	82.0	1	27	1.8	5.0	0.150	1.70E+03	25	-Vs	Yes	0.150	Low Noise, Precision, 90Mhz Differential I/O Amplifier
TI	THS4561	2.9	12.6	70.0	1	130	0.9	5.0	0.200	6.00E+02	27	-Vs	Yes	0.200	Low Power, High Supply Range, 70Mhz fully differential amplifier
TI	THS4531A	2.5	5.5	36.0	1	250	0.4	10.0	0.400	2.10E+02	25	-Vs	Yes	0.100	Ultra Low-Power, RRO, NRI, Fully Differential Amplifier with improved offset
LTC	LTC6363	2.8	11.0	35.0	1	75	1.9	2.9	0.100	1.00E+02	18	-Vs	Yes	0.150	Precision, Low Power Differential Amplifier
LTC	LTC6362	2.8	5.5	34.0	1	45	1.1	3.9	0.200	3.50E+02	10	Yes	Yes	0.080	Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver

There are two somewhat hidden issues in these newer parts contributing to lower phase margin conditions in certain kinds of applications –

1. Many are designed to nominal closed loop gain of 1 which is a Noise Gain (NG) of 2 with good phase margin. Adding a feedback capacitor as part of the design reduces the NG to 1 at higher frequencies - nominally giving lower phase margin.
2. The Rail to Rail output stages often have a complex and reactive open loop output impedance that interacts with both the load and feedback network. It is imperative to break the loop at the inputs so that this modelled Z_{ol} sees both the load and feedback network in the LG phase margin simulation (ref. 8). Some, but not all, of the listed devices in Table 2 include an accurate Z_{ol} model (fig. 2, ref. 8).

While there has been some earlier work on improving phase margins using FDA's with capacitive feedback capacitors (ref. 9), here a more detailed Multiple FeedBack (MFB) filter design example will show some added alternatives to improving the phase margin in those designs using the very well modelled THS4551 (ref. 10).

Starting from the 500kHz 2nd order filter used to drive the 24bit ADS127L01 in Fig. 78 ref. 10, two improvements can be made on the relatively low phase margin latent within this circuit. Figure 8 shows this design target with slightly improved RC solutions where a simulation of the spot noise across the output pins is a quick way to see if there might be a low phase margin at unity gain crossover for the Loop Gain (LG). This circuit has already added those small inside the loop 5Ω resistors which were found to help move the required external Riso to the load capacitor down. The two peaks in the noise at the output pins (before it is filtered by the post RC filter to the ADC) occur first at the noise gain peaking region that always occurs in these MFB filters and then a 2nd peak around 59MHz which is likely due to low phase margin at crossover.

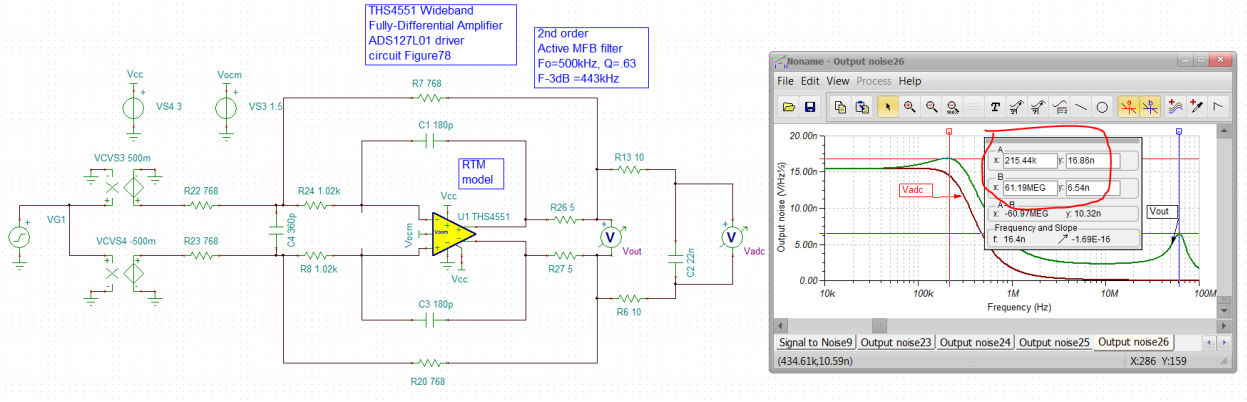

Figure 8. Closed loop THS4551 MFB simulation for differential output spot noise.

Using the LG phase margin set up of ref. 8, Figure 9 shows a low 21deg phase margin for this simple starting point design. Here, +/-2.5V supplies have been used with a centered Vcom voltage at ground for the LG phase margin simulation. The differential summing point sense voltage polarity reports phase margin directly where the THS4551 differential input impedance is pulled outside the inductive break points and placed across the input sensing points.

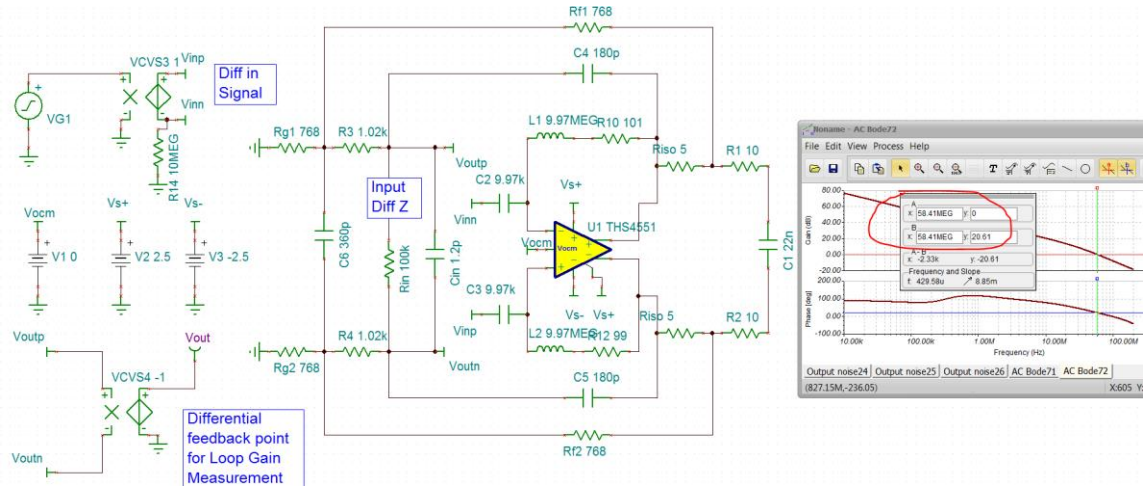

Figure 9. Initial phase margin for 500kHz MFB filter using the THS4551

A common approach (ref. 11) to improving phase margin for inverting designs (like this MFB filter) is to shape the Noise Gain (NG) up over frequency using a feedback capacitor and a capacitor to ground (for an op amp design). This MFB filter already has feedback capacitors as part of the filter design where placing that same value differentially across the FDA summing junctions is nominally shaping the NG up from 1V/V at higher frequencies (due to just the feedback capacitors) to 1.5V/V splitting the differential capacitor into 2 elements to ground at 2X the value in a NG analysis. Making that slight modification to the original LG simulation circuit does indeed lower the crossover frequency raising the phase margin to 32deg. That capacitor is connected across the differential sense point connections where they are converted to single ended with is the same as putting it in parallel with the device differential input Z.

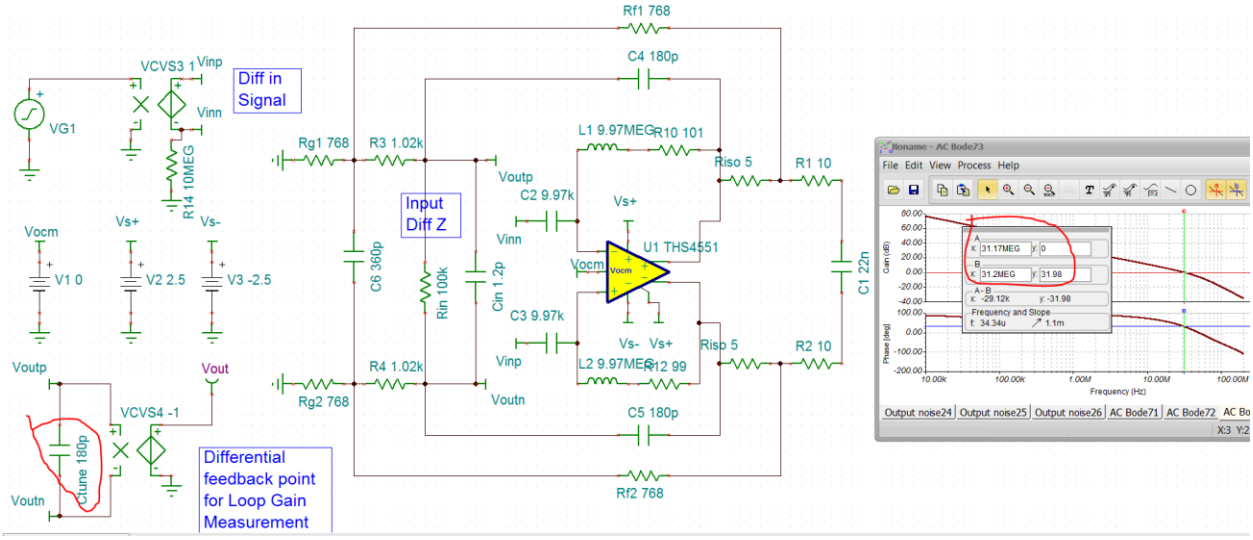

Figure 10. Improved phase margin using only a NG shaping capacitor across the FDA inputs.

This simple approach is not working as well as it does for low output impedance, non-RRout, high speed op amps. The very reactive open loop output impedance is still adding excessive loop phase shift at the output pins due to the feedback capacitive load. One simple change to try is to move the MFB feedback

capacitor connection from the output pins to be outside the isolating 5Ω resistors. Doing that in Figure 11 indeed works very well to increase the phase margin to 52deg.

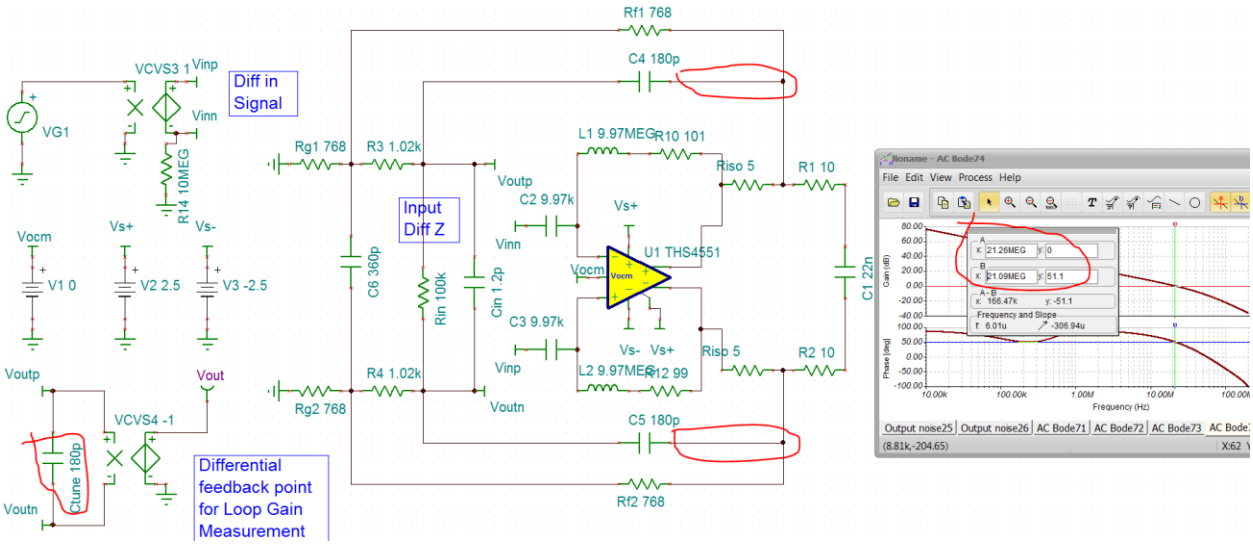

Figure 11. Phase margin with an added NG shaping input capacitor and connecting the MFB feedback caps outside the 5Ω isolating resistors.

Going back to the closed loop spot output noise simulation of fig. 8 with these two small changes shows a much reduced higher frequency noise peaking in Fig. 12.

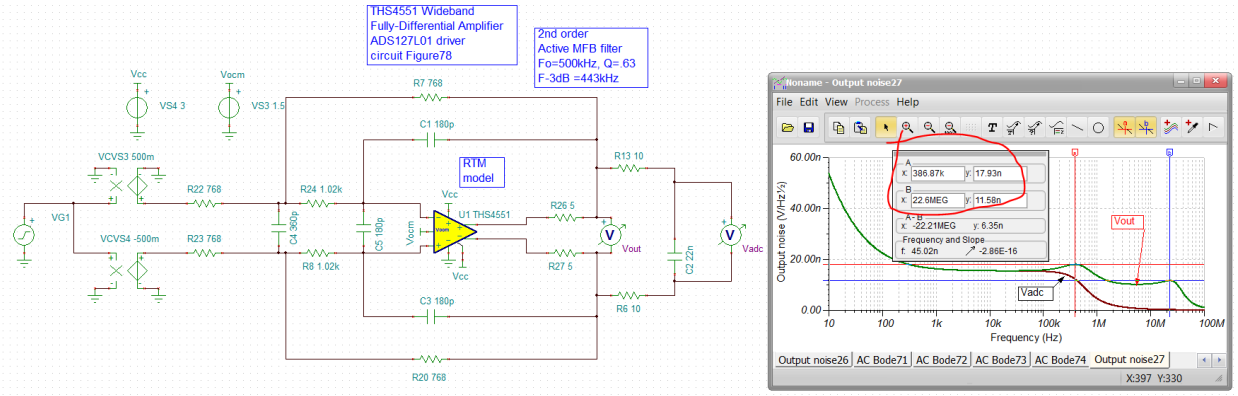

Figure 12. Output differential spot noise with improved phase margin design changes.

Making these two modifications has also improved the fit to target as shown in the two response curves to the differential FDA output pins shown in Fig. 13.

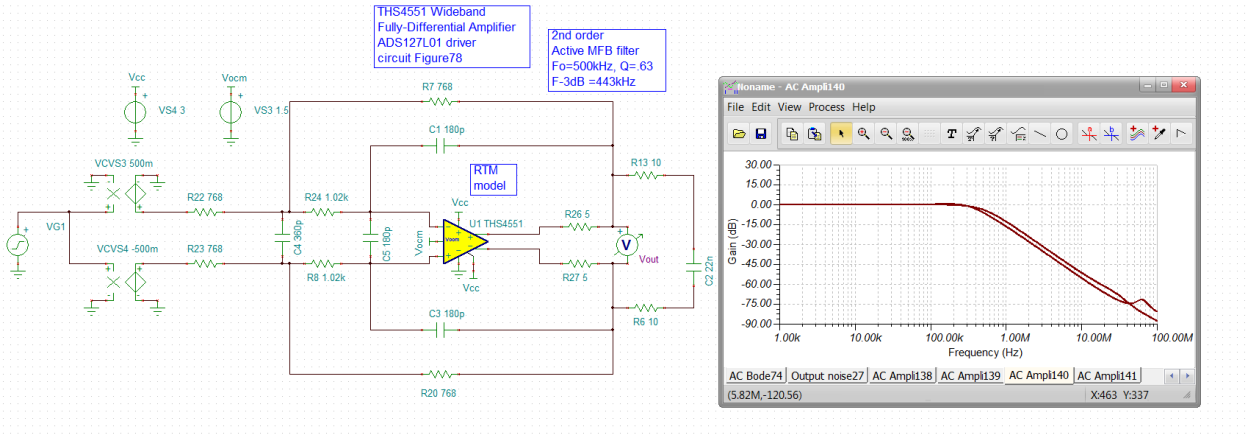

Figure 13. Filter responses curves with original vs improved phase margin designs.

The original circuit of Fig. 8 gives that slight response peak at 59MHz and actually missed the ideal 440kHz target F_{-3dB} with only 385kHz. The improved phase margin design of Fig. 13 removes that resonance and hits the target very closely with 443kHz F_{-3B}. Since the RC values are the same in each case, the shift in target shape can probably be attributed to the open loop output impedance seeing the feedback capacitors directly instead of isolated through 5Ω's.

The methods described here to extract the phase margin for a voltage feedback FDA can be applied to any application circuit. In the specific case of circuits having direct feedback capacitors, consider adding small inside the loop isolating resistors then connecting those feedback capacitors outside those R's. Also, consider adding (at least a placeholder on the PCB) a differential input capacitor to shape the noise gain up at higher frequencies. Many older non-RRout designs respond very well to this noise gain tuning by itself. For RRout designs, it might be necessary to also include the isolating resistor and connect the feedback C outside that element to isolate the reactive open loop output impedance. It is not always the case that the model captures that effect – even if it is almost certainly in the physical device for RRout devices. Next up, extracting parasitic input capacitance for the different high speed amplifiers, what to do if it doesn't match the datasheets, and how that element gets into the response for different circuits.

References for FDA Stability considerations

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