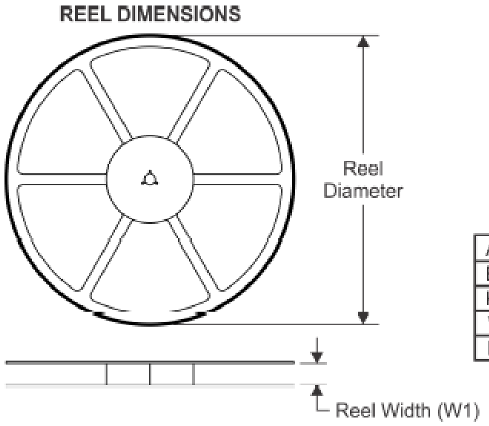
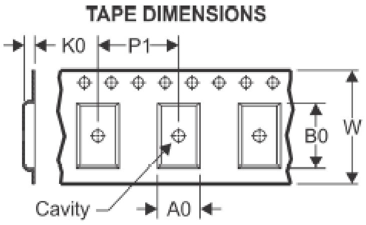
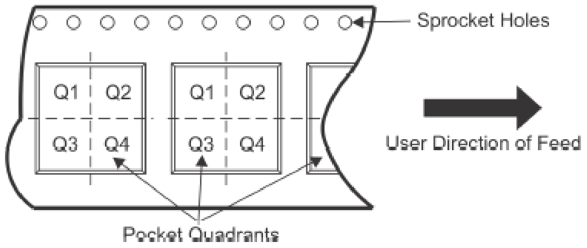
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

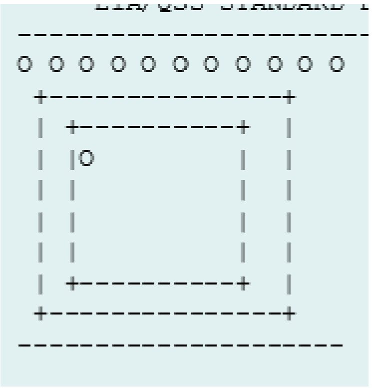
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27Z561YPHR-R1	DSBGA	YPH	12	3000	180.0	8.4	1.83	2.2	0.53	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27Z561YPHR-R1	DSBGA	YPH	12	3000	182.0	182.0	20.0



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Marking picture	vendor Name	Part No.	Marking Rule
Q27Z561R1	TI	BQ27Z561YPHR-R1	the marking " Q27Z561R1" represents the device name, by identifying units marking Q27Z561R1 correctly to determine device

TI Part	Component	Homogeneous Material Name.	Substance Name	*CAS No.	Substance Mass. (mg)	Content Rate(%)
BQ27Z561YPHR-R1	Solder Bump	Copper and Its Alloys	Copper	7440-50-8	0.002245	0.599961
		Other Nonferrous Metals and Alloys	Tin	7440-31-5	0.357353	95.500159
		Precious Metals	Silver	7440-22-4	0.014593	3.89988
	Semiconductor Device	Ceramics / Glass	Doped Silicon	7440-21-3	1.485935	100

Basic Information	**Result**
Device Part Number	BQ27Z561YPHR-R1
Wafer fab information, process type and node	foundry
Wafer process was qualified and released to production or not.	Mature
Products have been applied with this wafer process?	Yes
Is there any part from the same wafer process family have been used in customer?	YES
Wafer Process Capability(SPC)	Meet SPC Spec
Is there any wafer process CPK<1.33? If yes, please list it and provide the improvement plan.	NO
Chip ID:Do you have chip ID or die ID for this device?	NO
Assembly Factory, Package type	TI Clark WCSP
Package Size (Length*Width*Height)	2.05x1.67x0.4mm
Ball/Lead pitch	0.5MM

Is there any part from the same package family have been used in customer? If yes, please list the part number.		YES
Wire Bonding (Only for Wire Bonding Package)	Wire composition	NA
	Wire diameter	NA
Assembly Process Capability(SPC)		Meet spc spec
Is there any assembly process CPK<1.33? If yes, please list it and provide the improvement plan.		NO
Range of Operation Temperature （Ta, Tj or Tc）		-40~85C
Storage Temperature range		-65 ~ 150C
Storage limit		1years at customer side
Max.Junctioin Temperature		125C
IFR, Intrinsic Failure Rate, FIT		1.5FIT@60%CL
MSL, Moisture Sensitive Level		MSL 1
Theta ja, jc and jb	Θja	64.1°C/W
	Θjc	59.8 °C/W
	Θjb	52.7°C/W
ESD (HBM、CDM, for all pin)	HBM	1500
	CDM	500
Latch-Up (At max. Ambient Temperature)		Meet qual test requirement
Test Factory		TI Clark
If the chip is new process or new design, And some Lifetime limit test(Test to fail or beyond JEDEC standard) had been down. Please specify the test condition and result details.		NO
Wafer reliability Qualification Report, including: TDDB, HCI, NBTI, PBTI, EM, SM .etc		YES
Package Qualification Report, including: PC, THB, HAST, UHAST, HTSL, TC, BLTC, DT, Bend, PDT, PVT .etc		See TI.com qual report
Device Qualification Report, including: ELFR, HTOL, LTOL, ASER, SSER, ESD-HBM, ESD-CDM, LU .etc		See TI.com qual report
The device should be done reliability monitoring. Please provide the latest Reliability Monitoring Report, including: PC, THB, HAST, UHAST, TC, HTSL, HTOL .etc		ORT test based on package
Characterization report, follow JESD86		Refer to datasheet

Component information		Investigation Result
Ball Compositions and ratio		SAC396
Ball Diameter(μm) before ball attachment		0.25MM
Back side laminate		Yes
Is there RDL layer in WLCSP?		Yes
Package standard		JEDEC
Weight of component (g)		1.90mg
Weight/ available P&P area≤0.06g/mm2		Yes
Is there polarity point on the top side of component?		Yes
Is the polarity point sole?		Yes
Is there any specific location number of terminals in component specification?		Yes
Component orientation can be identified by AOI?		Yes
Are matters RoHS compliant and lead free?		Yes
Are matters are Halogen-free		Yes
Storage Condition	Relative humidity (%)	≥20%&≤70%
	Temperature (℃)	≥-10C&≤35C
	Maximum storage time (month)	12Month at customer side
Packaging type		Tape and real
Position of component pin 1 in packing		Q1
Packaging height(K0)		0.53mm
Packaging width(W)		8mm
component pitch:P1		4mm
ESD packaging		Yes
Rollover rate ≤0.05% in packing		Yes
tray packing Baking conditions: 125℃@24h		Yes

reel tape packing Baking conditions: 40℃@192h	Yes
Can reel tape packing meet EIA-481 standard?	EIA
MSL	1
MSL>=2,moisture sensitive protection must include: moisture sensitive indicator card, desiccant, moisture sensitive grade logo	Yes
Baking requirement meet J-STD-033b if moisture	Yes
Maximum soldering times ≥3	Yes
Can heat resistance of SMT components meet JSTD020D. (should focus on the classification of temperature and reflow profiles, that is table 4-1, 4-2 and 5-2, please refer to sheet6 J-STD-020D in this file)	Yes
Maximum pick-and-place pressure (N)	Meet SMT pick-and-place pressure request
Whether the welding process and design requirements of component have all written to the component specifications	Yes
Whether Pad & stencil design as Mandatory requirements in component spec?	recommended
Whether the device has special requirements for the reflow temperature ramp-up rata and ramp-down rata? Customer follow J-STD-002 standard	No
Are there other mandatory requirements in component spec?	No
Solder ability shall be tested per J-STD-002D and the report must be offered,	Yes