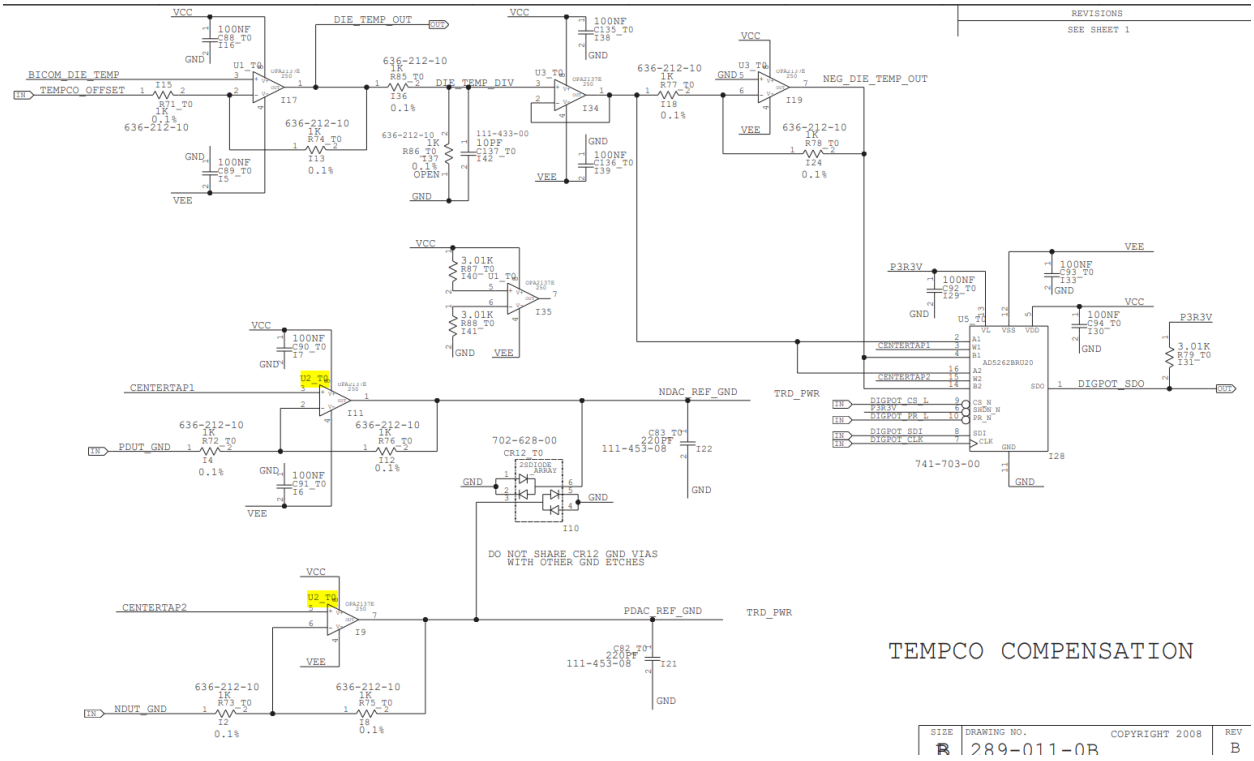
Contents

Description of the problem

The Operational Amplifier OPA2137E is being reported by the Tester. The References Designators are U1_Tx, U2_Tx U3_Tx.

The same circuit for figure below is valid for all reference designators.

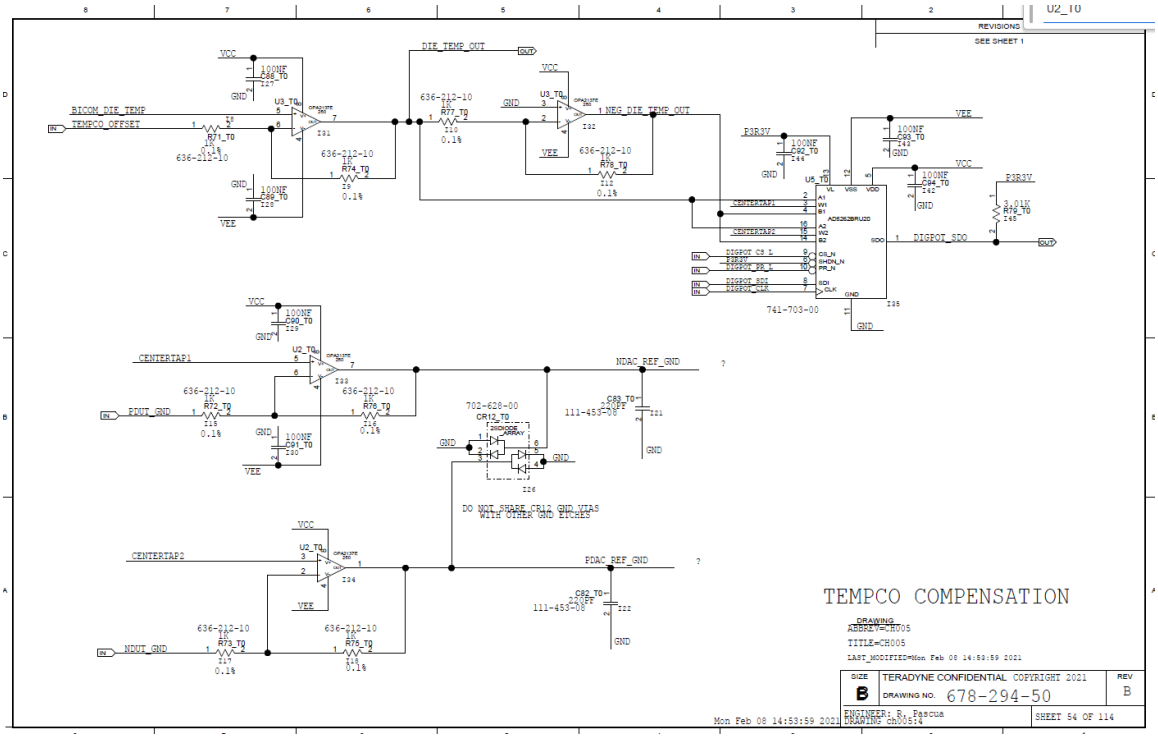


Comparing 289-011-0B & 678-294-50

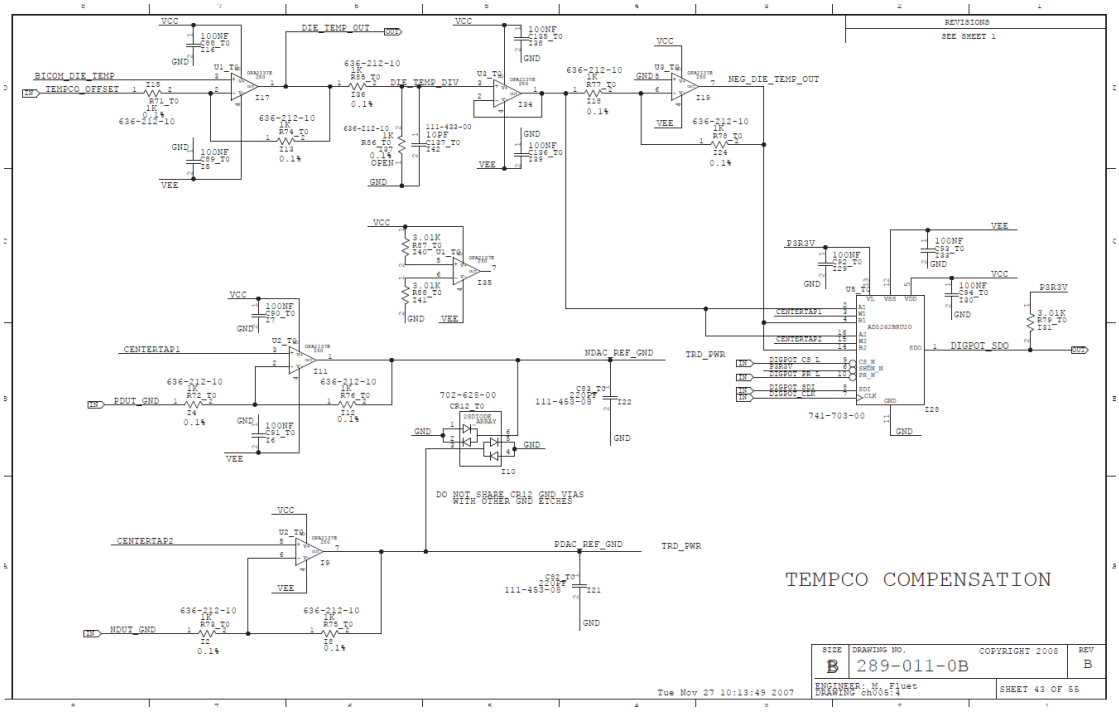
U2_T0

The circuit is the same in both PCBAs

278-294-50



289-011-0B



Test Step

The test comes from different libraries

278-294-50 (Library: \libraries\teradyne.htl)

U2_T0_P: {

/***

DUT: U2_T0

Type: OPA2137

Model: OPA2137

Library: \libraries\teradyne.htl

Pin count: 9

Pin	Signal	Type	Node
1	OUT1	ANALOG OUTPUT	U2_T0_1
2	IN1M	ANALOG INPUT	U2_T0_2
3	IN1P	ANALOG INPUT	U2_T0_3
4	VM	POWER	VCC5
5	IN2P	ANALOG INPUT	U2_T0_5
6	IN2M	ANALOG INPUT	U2_T0_6
7	OUT2	ANALOG OUTPUT	U2_T0_7
8	VP	POWER	VCC
9	CGND	GROUND	GND

Flagspecs:

MSG = PN=73107200002 X:7.975 Y:1.600 SIDE=B

***/

289-011-0B(Library sy:BT011B.htl)

U2_T0_P: {

/***

DUT: U2_T0

Type: OPA2137

Model: OPA2137

Library: sy:BT011B.htl

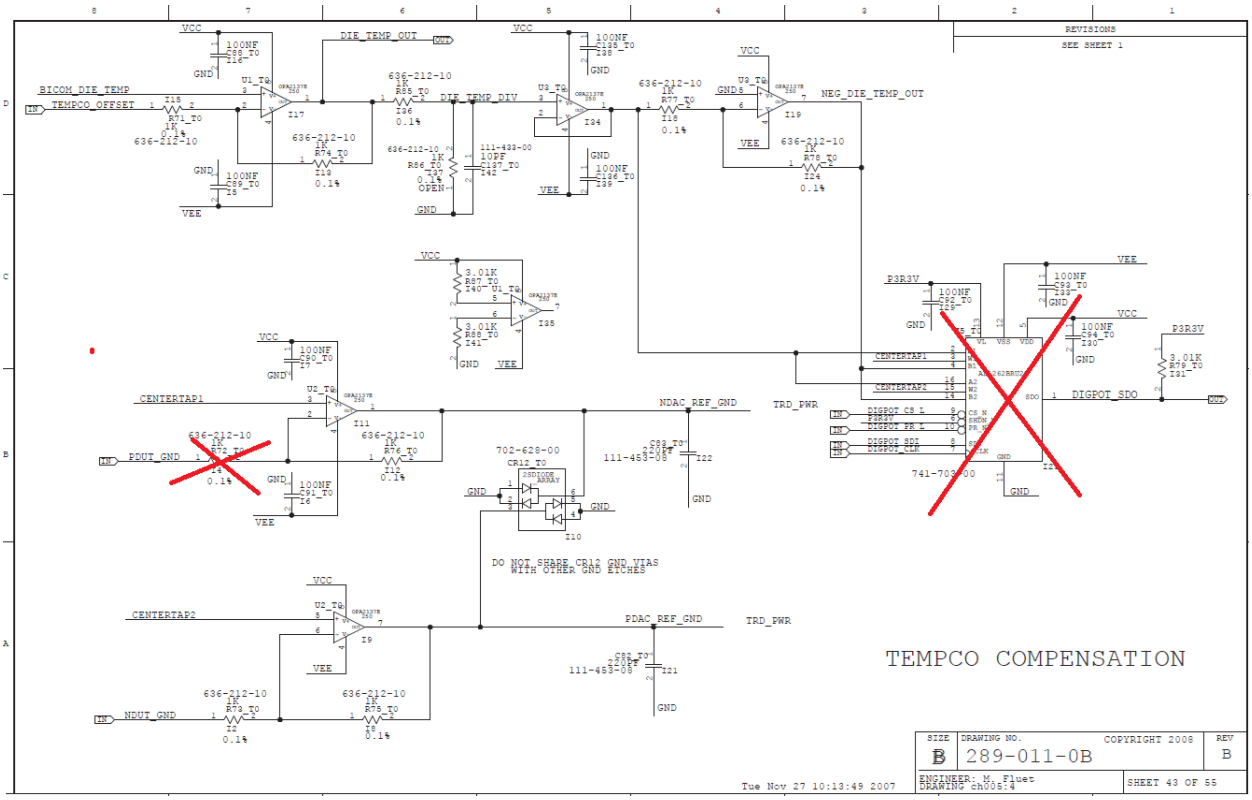
Pin count: 9

Debugging

1. To Isolate U2_T0

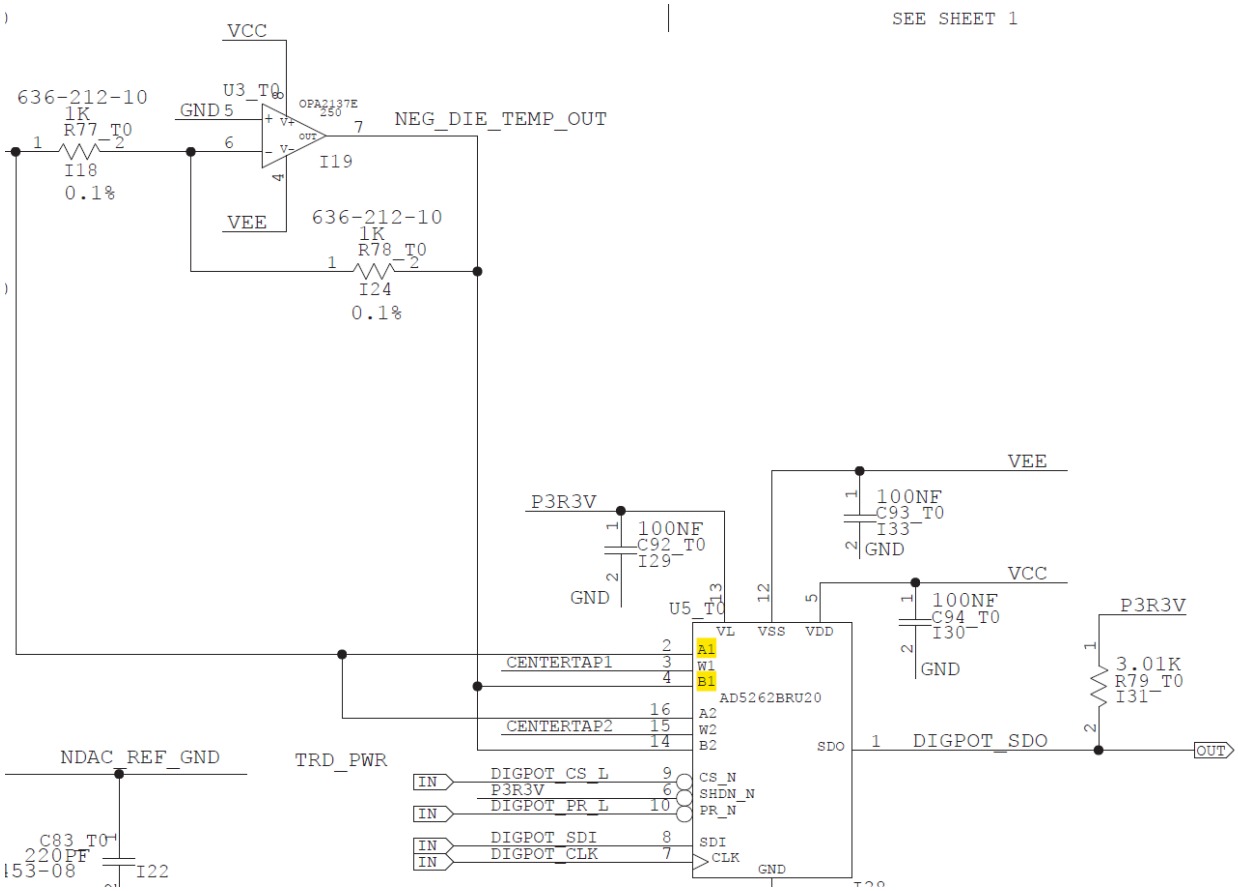
The components U5_T0 & R72_T0 were removed but the test is still measuring 0.92V (the valid range is between 0.4V and 0.9V).

The input voltage of the step was reduced from -0.2V to -0.043V, and it passed



2. Resistance Test on U5_T0

This step is failing, resistance between pins U5_T0.2 & U5_T0.4 is greater than 15Ohms

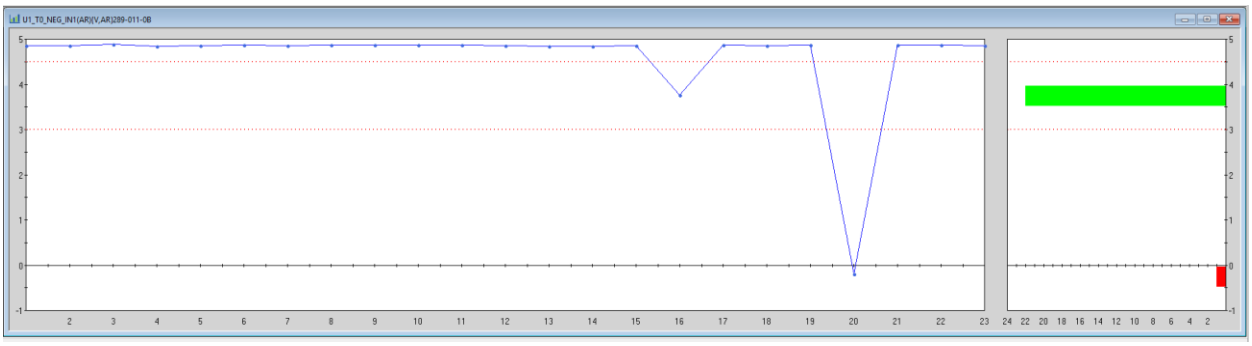


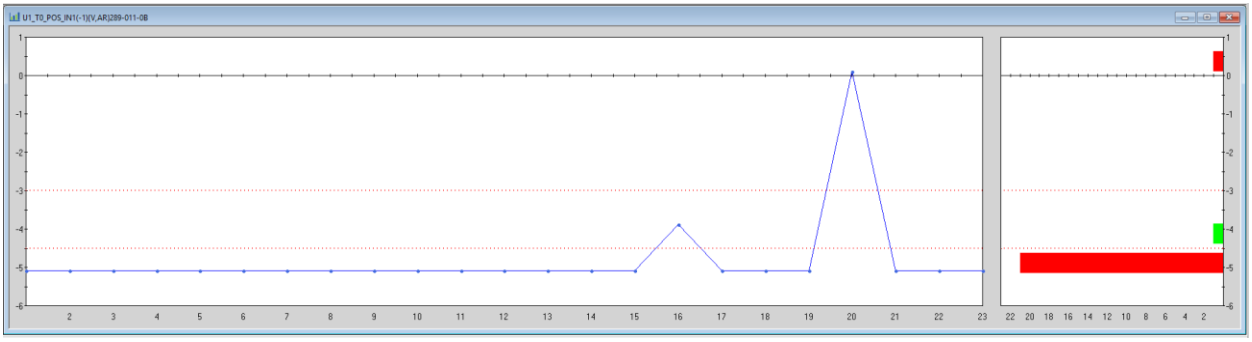
With Ohmmeter outside the fixture the measurement is 2K-Ohm on the golden board and production board,

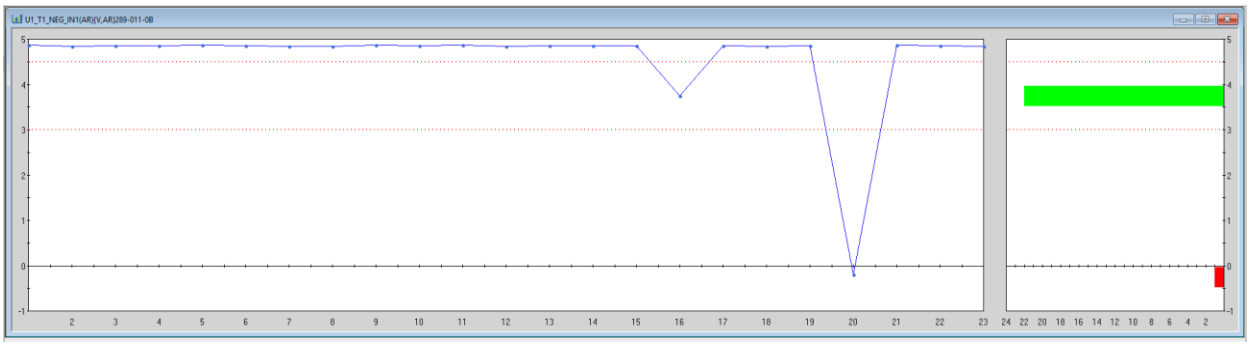
Results of Current Production

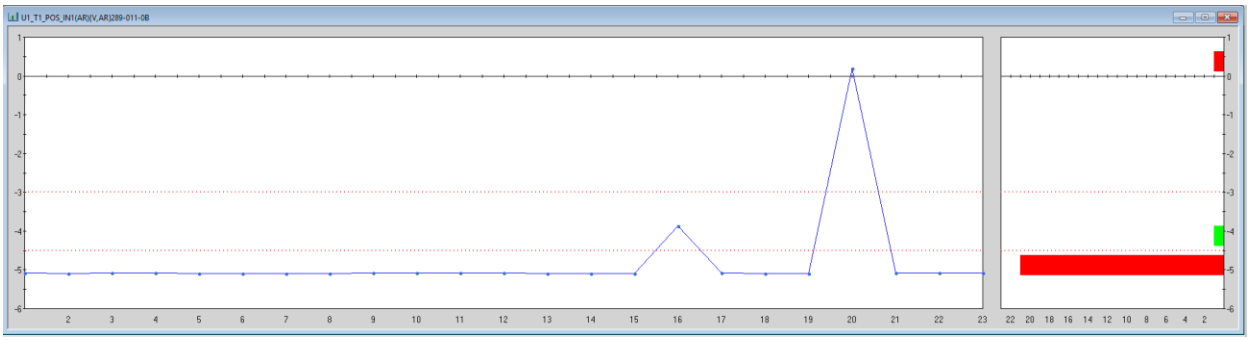
Operational Amplifier OPA2137E

U1_Tx





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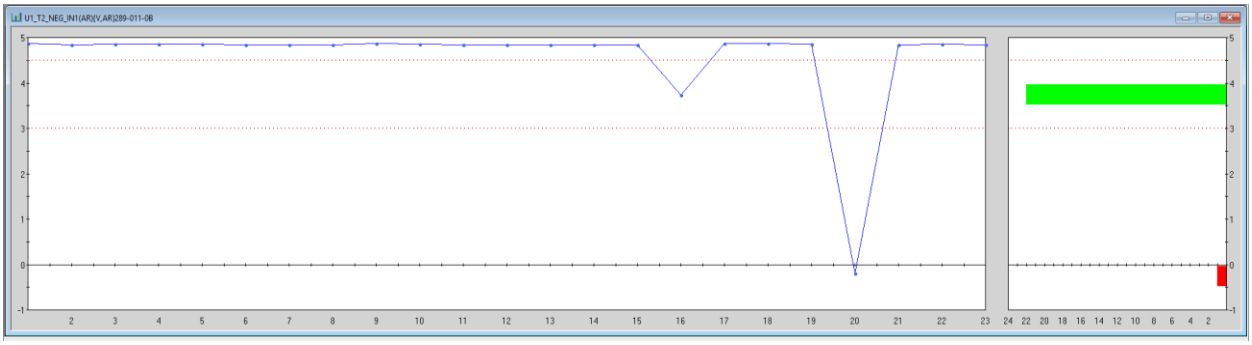
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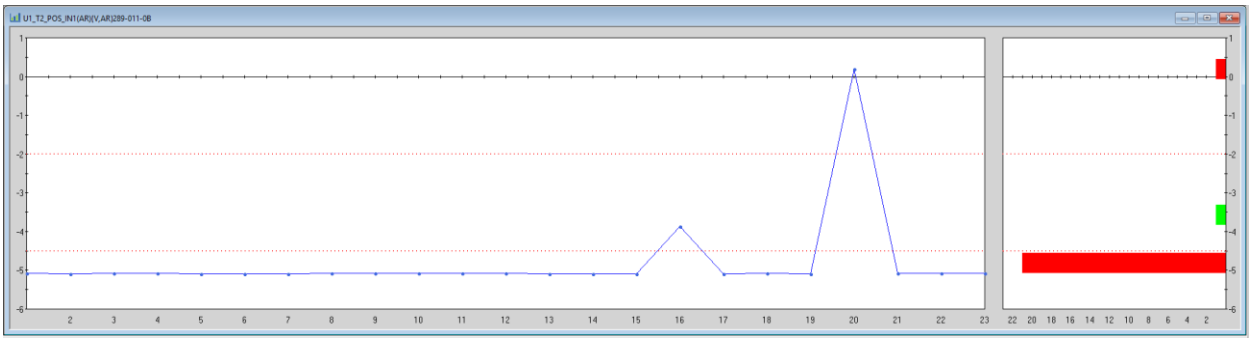
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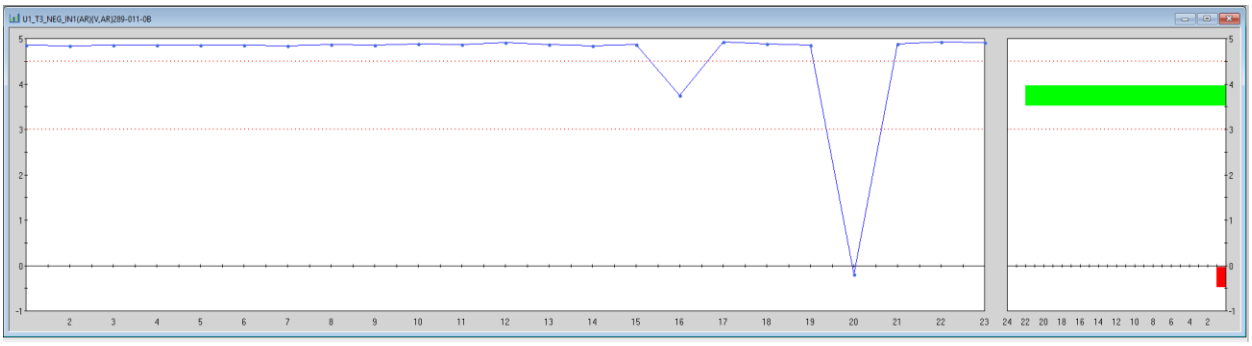
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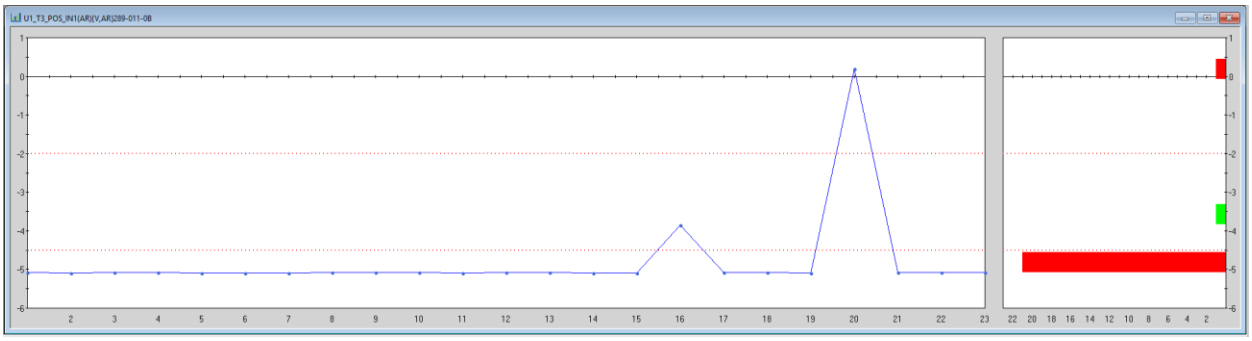
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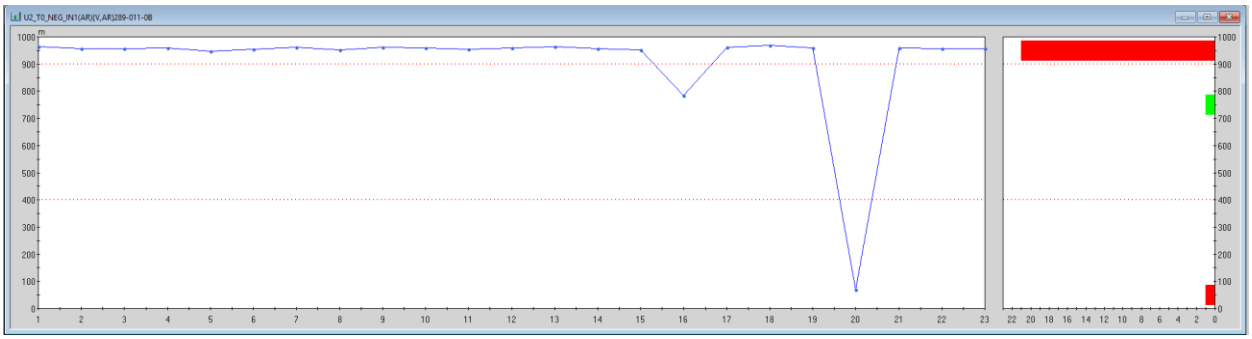
U2_Tx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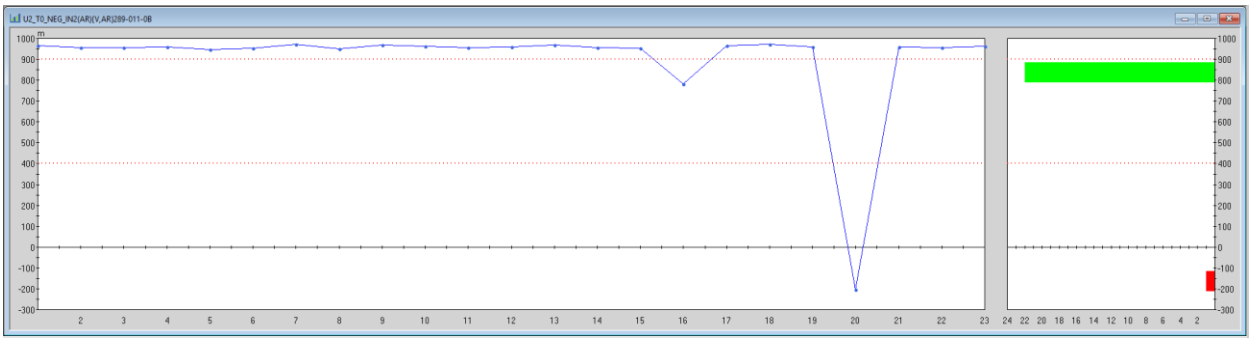
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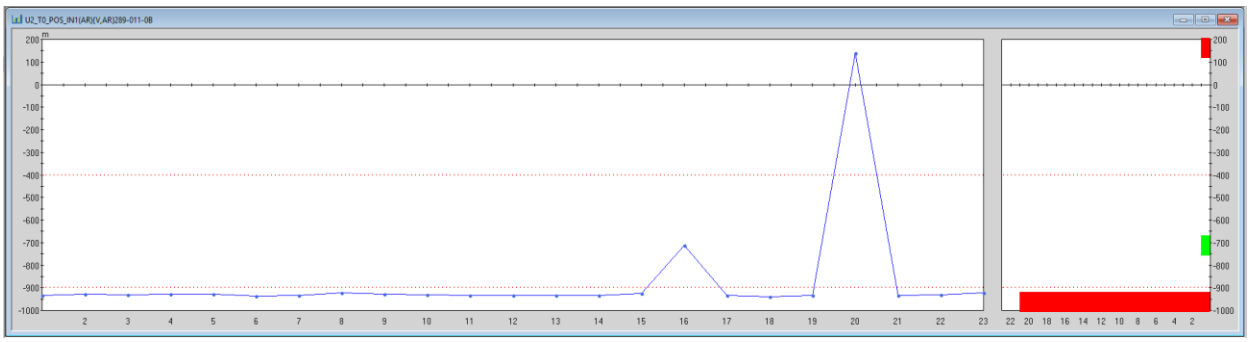
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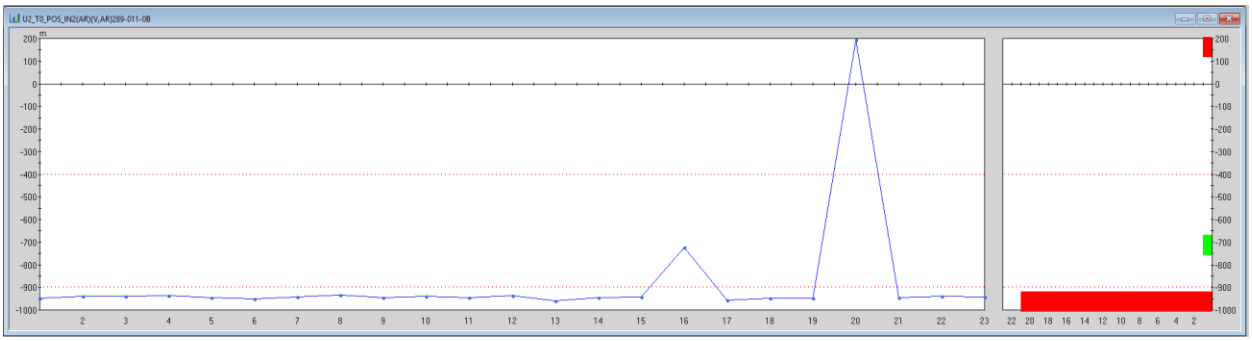
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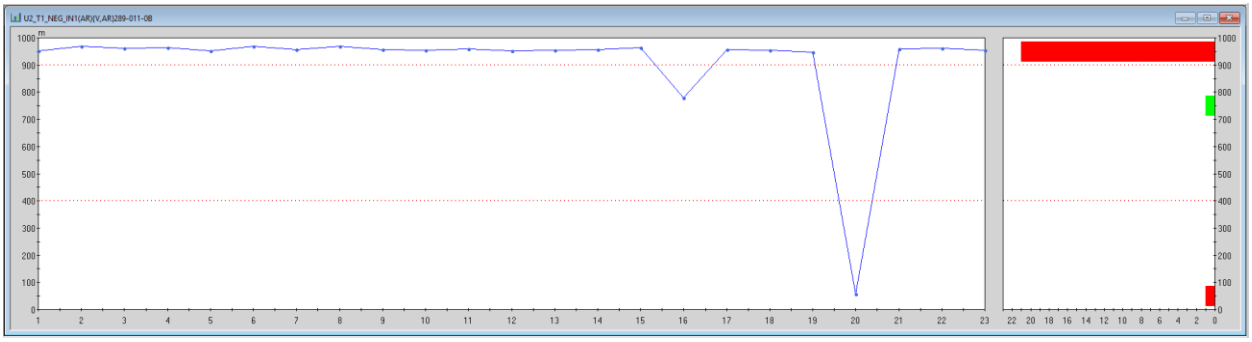
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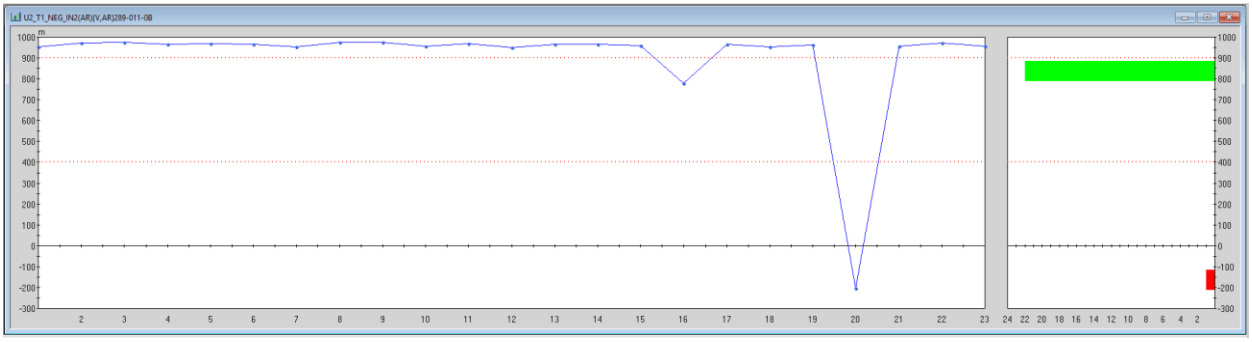
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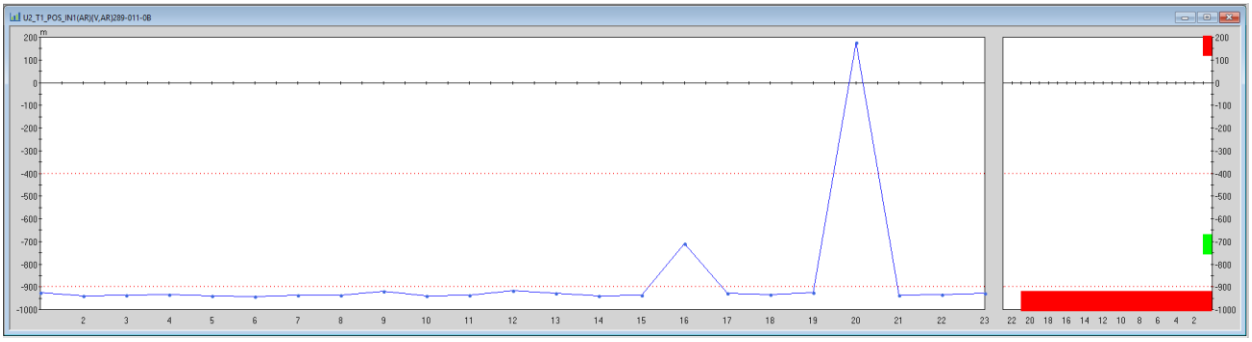
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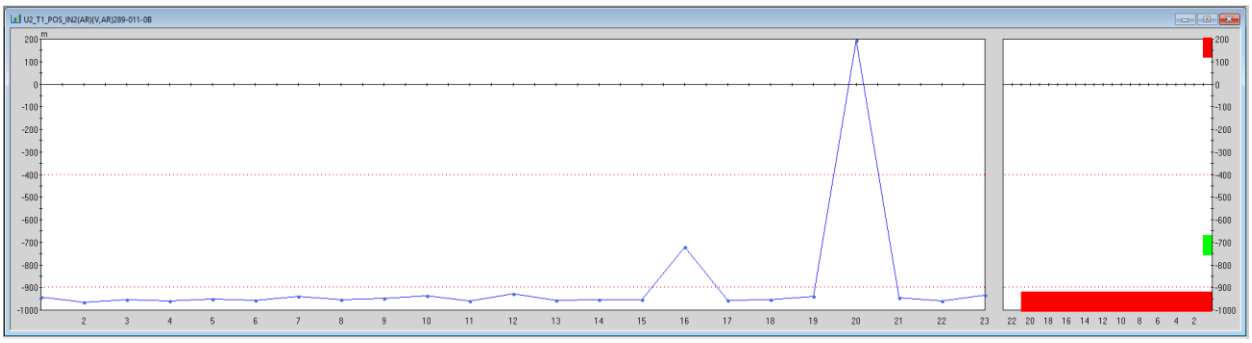
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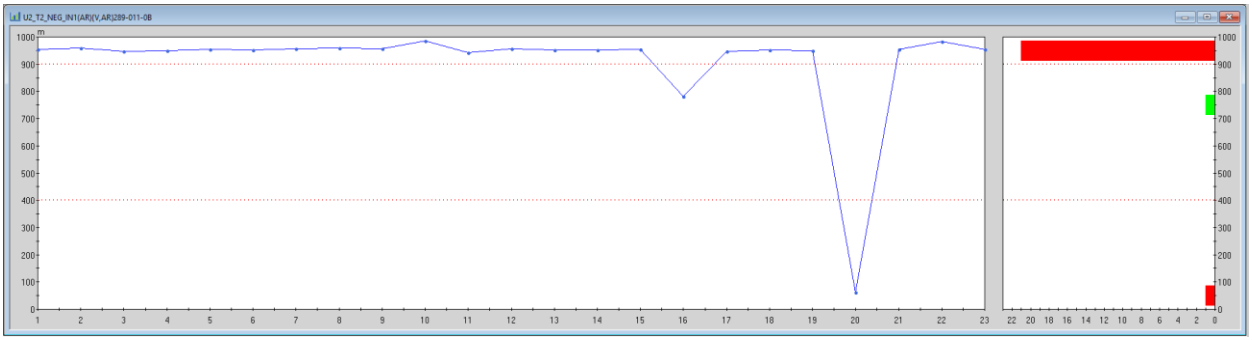
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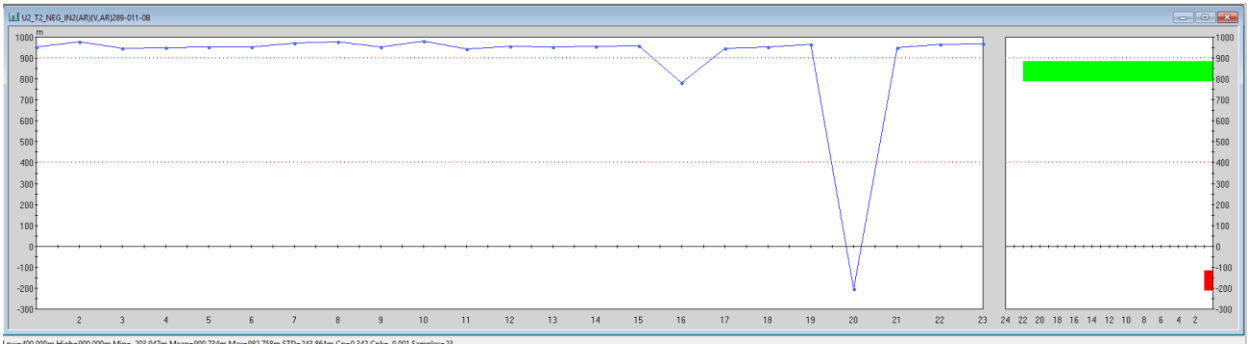
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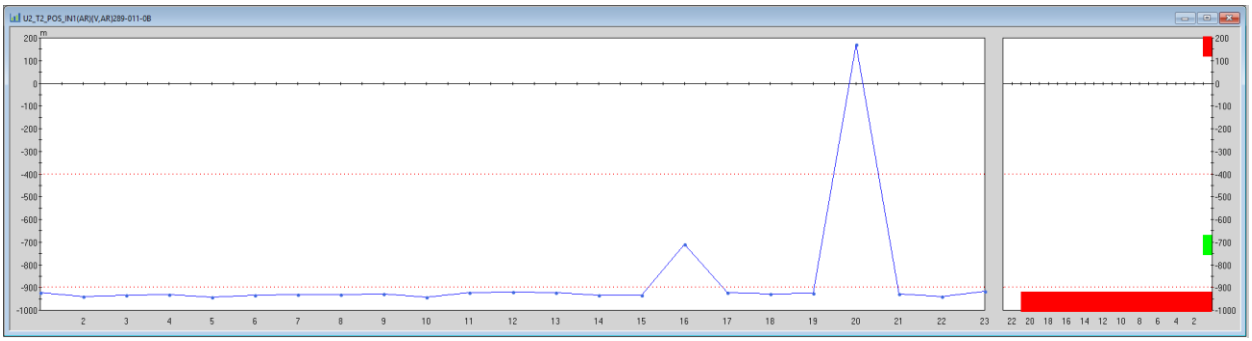
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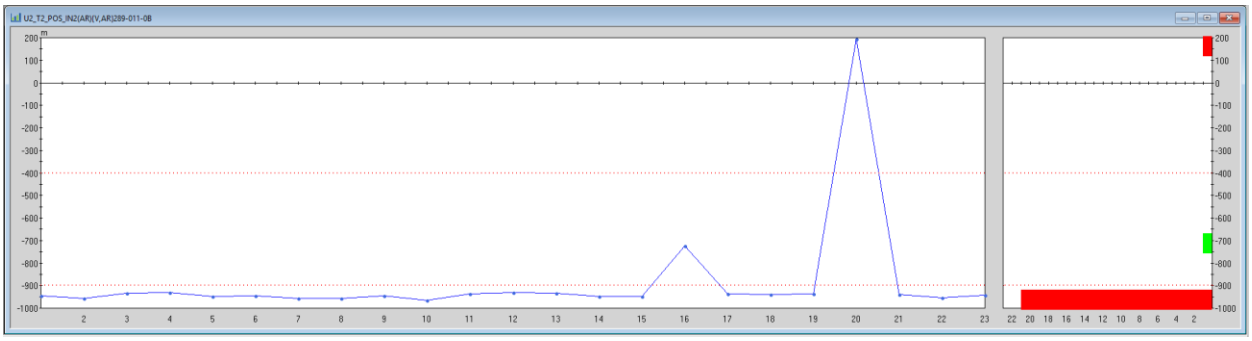
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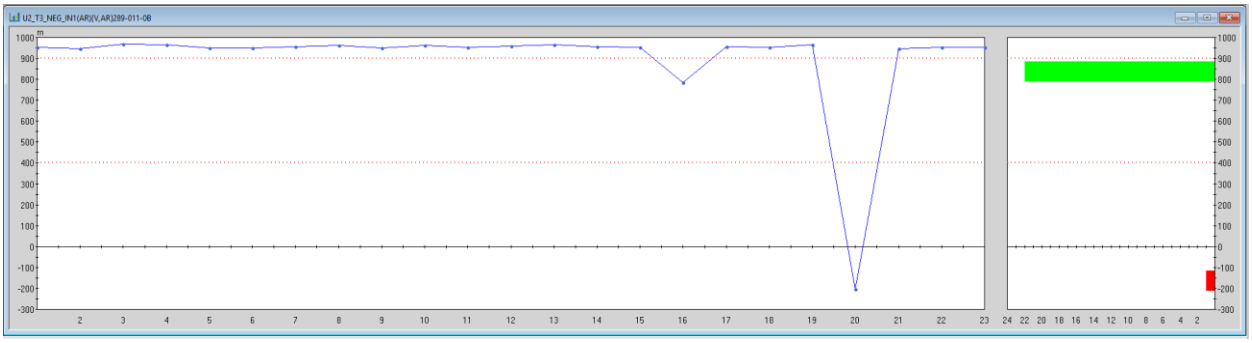
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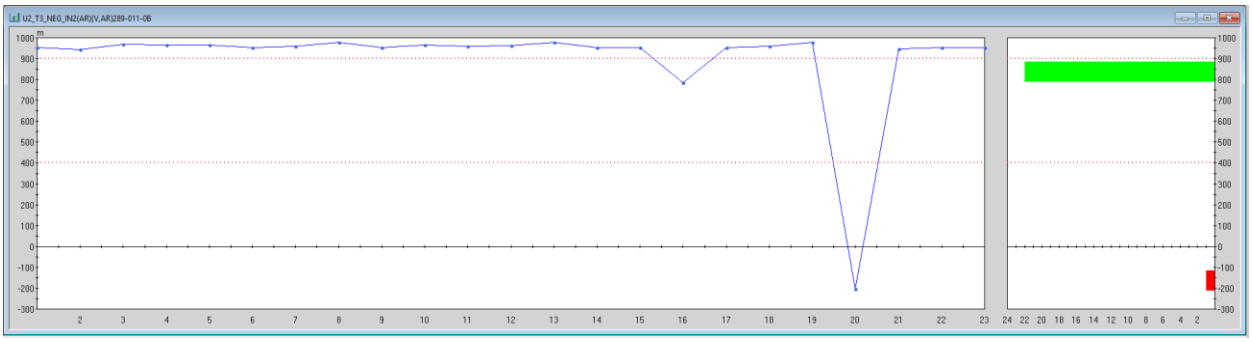
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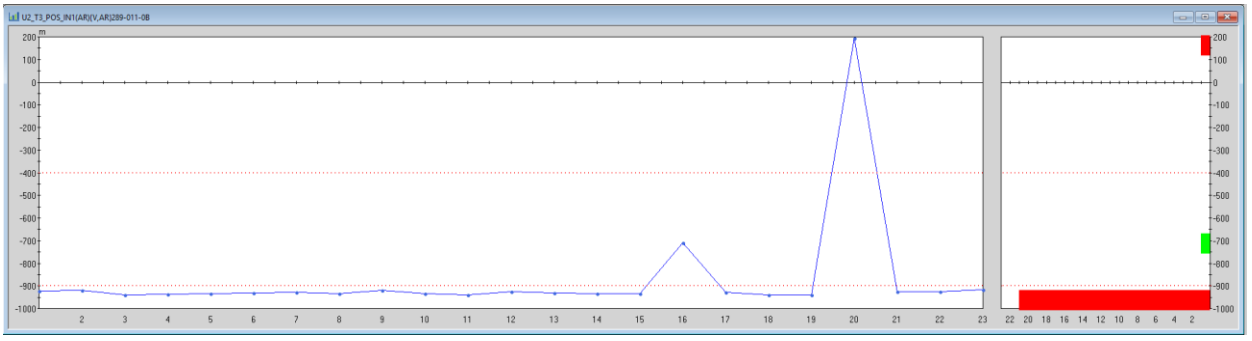
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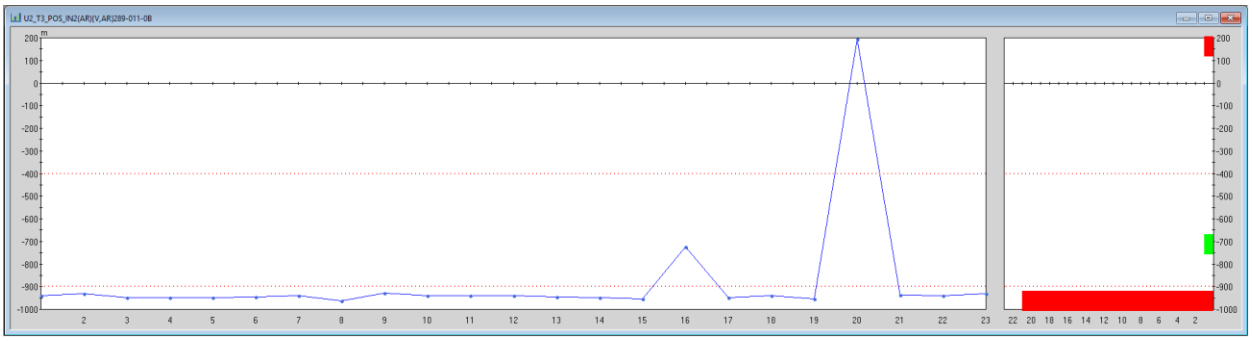
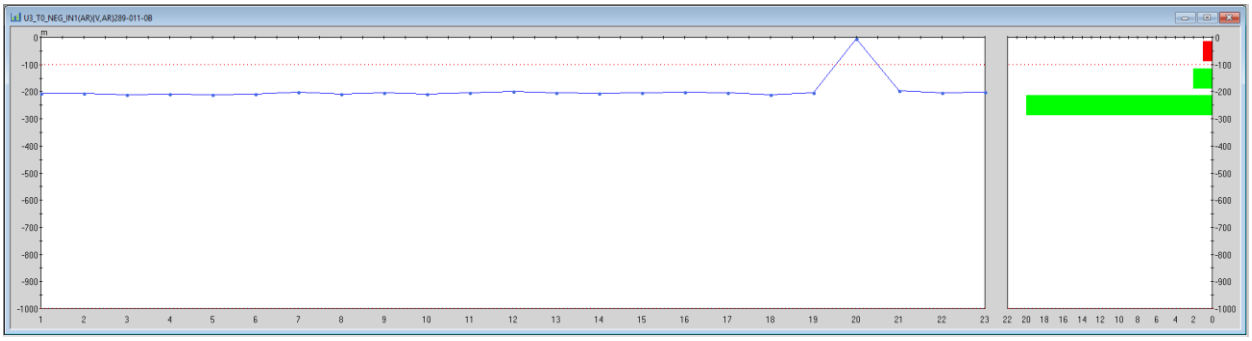
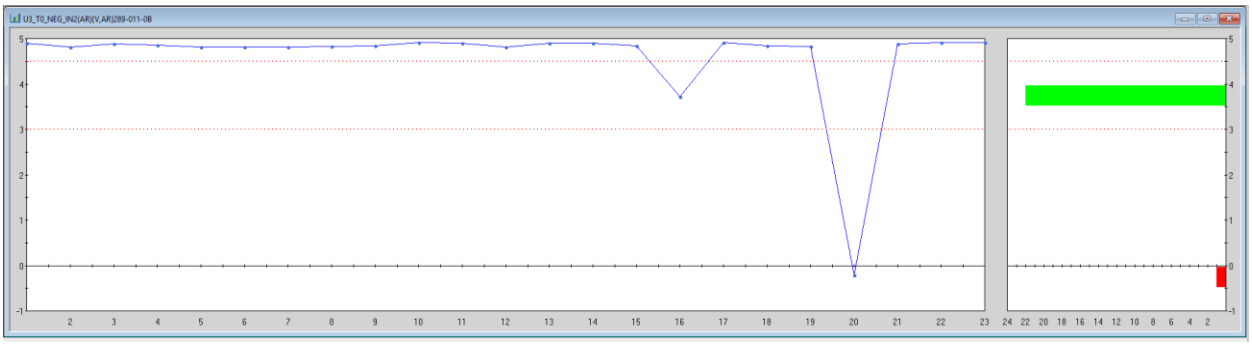
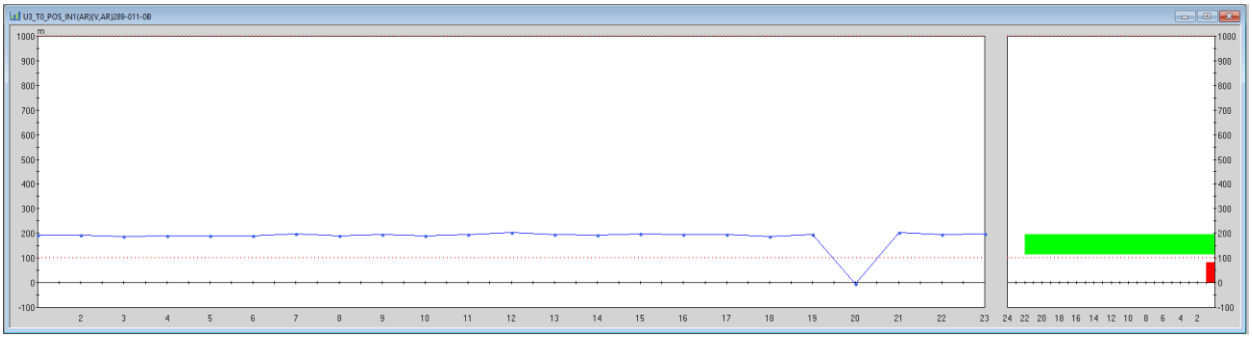
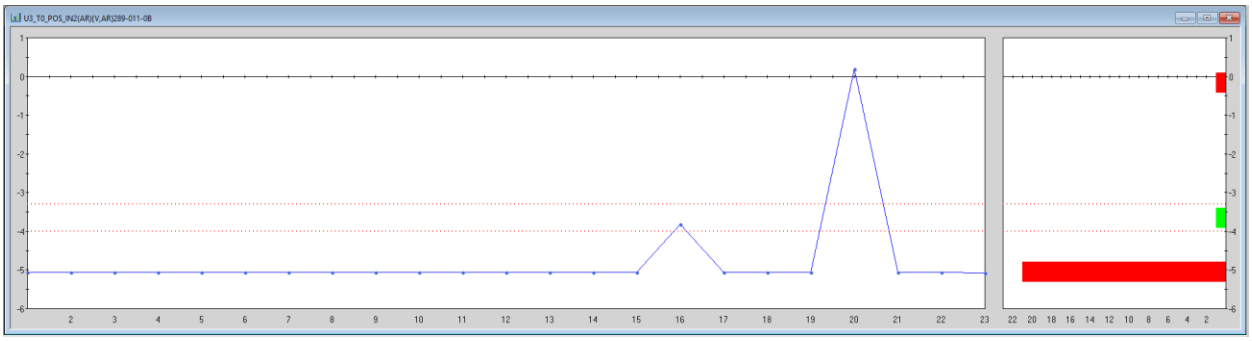


U3_Tx





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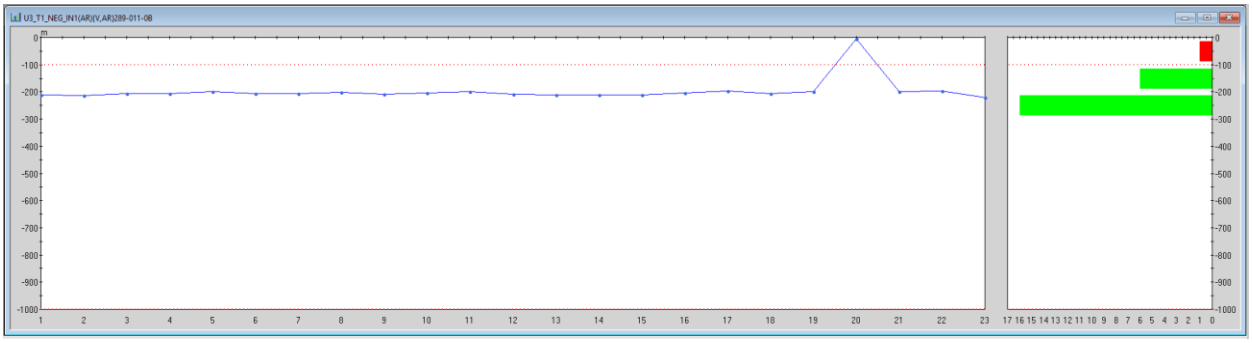
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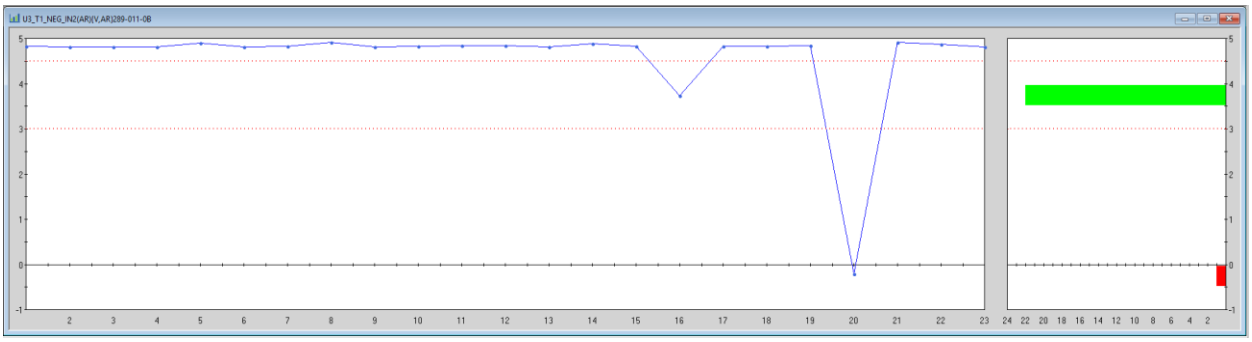
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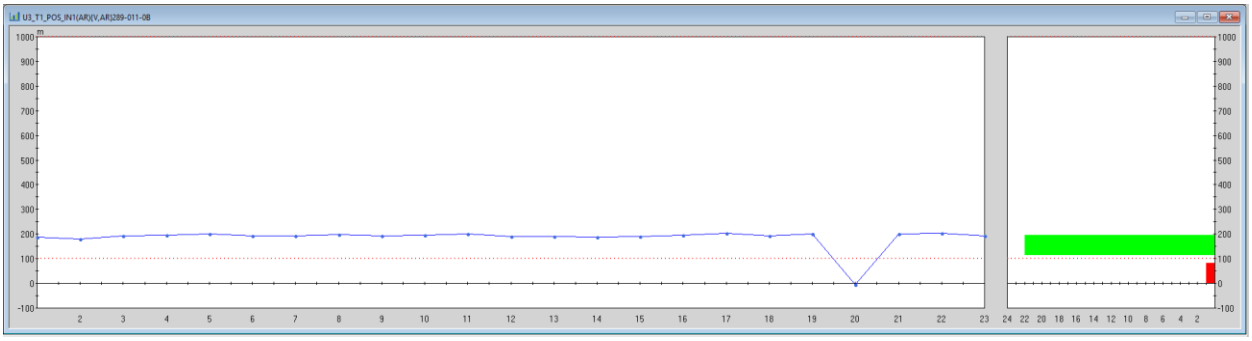
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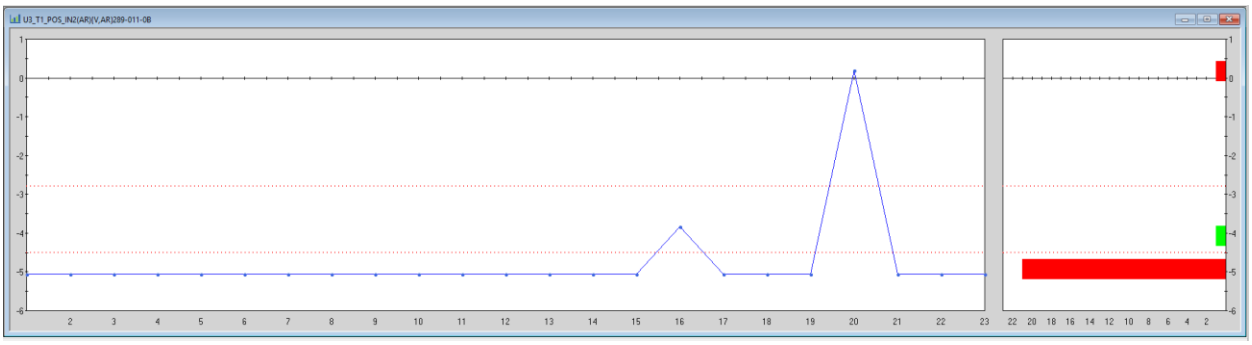
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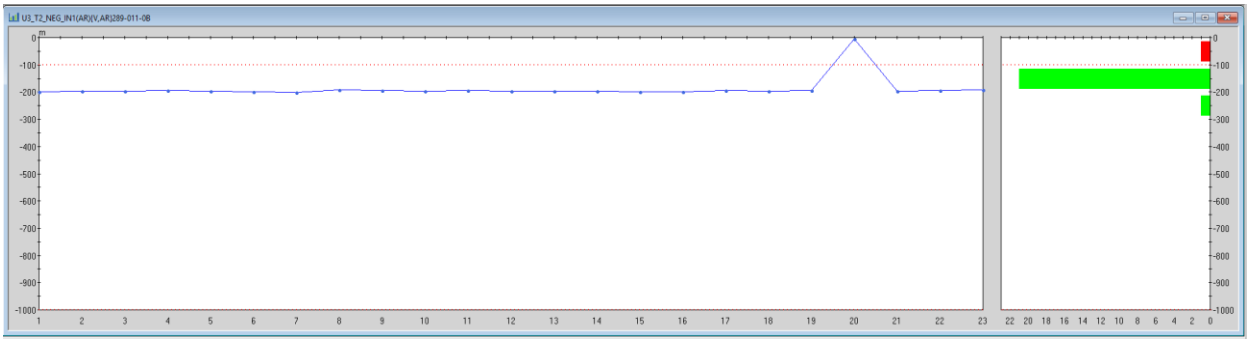
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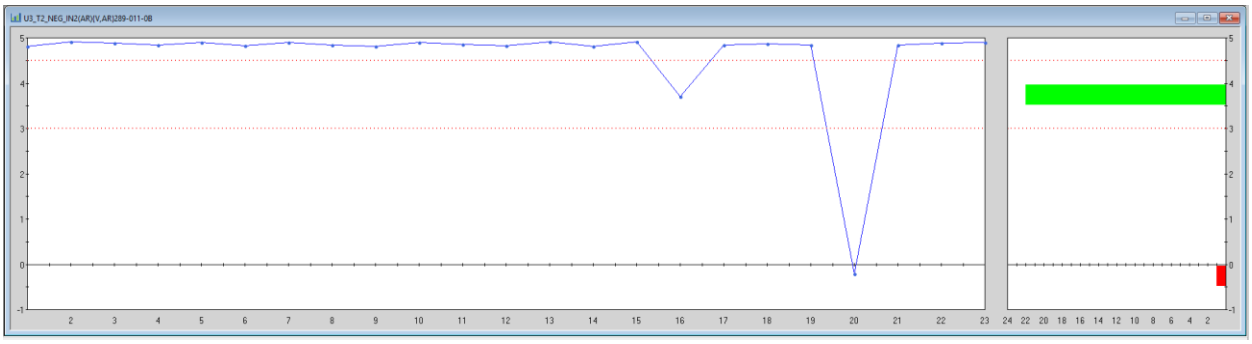
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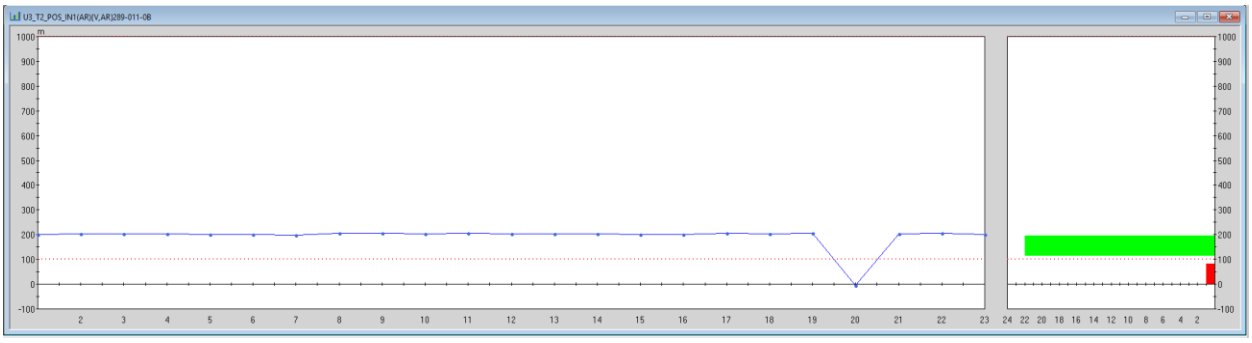
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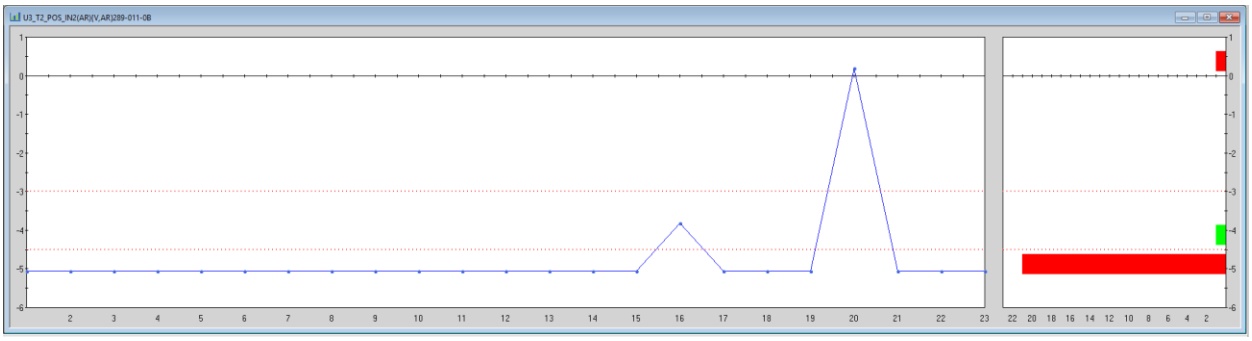
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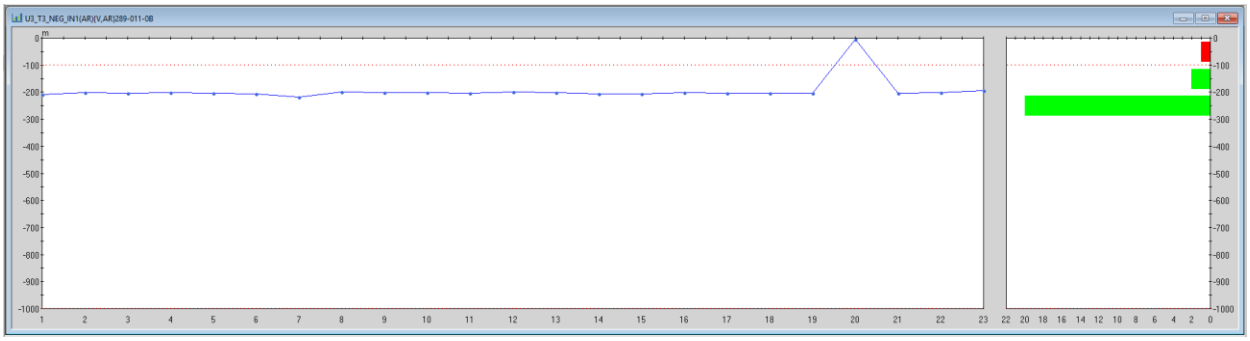
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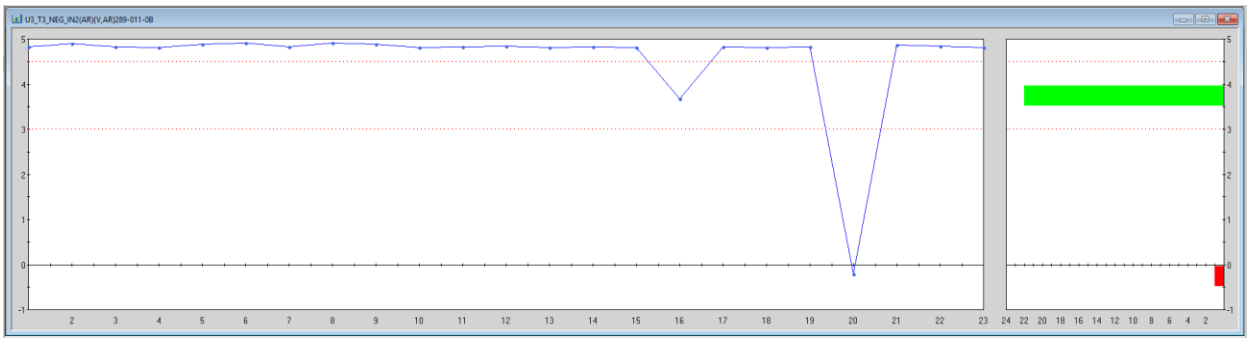
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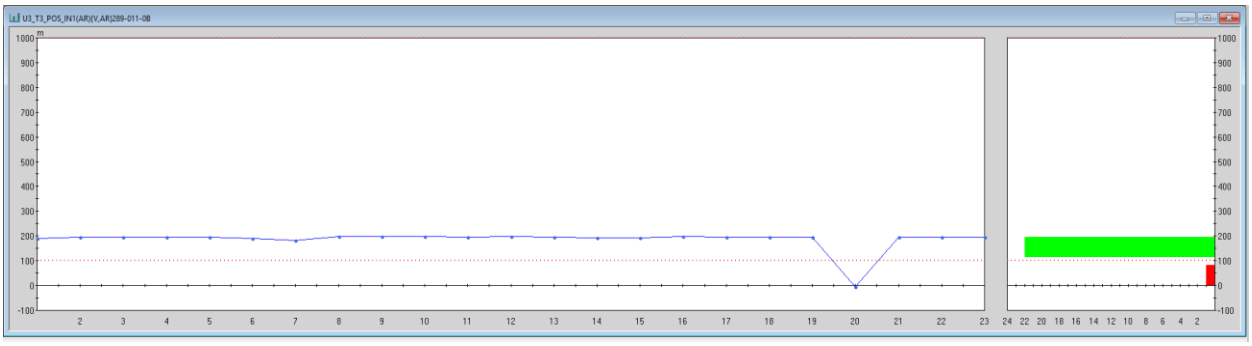
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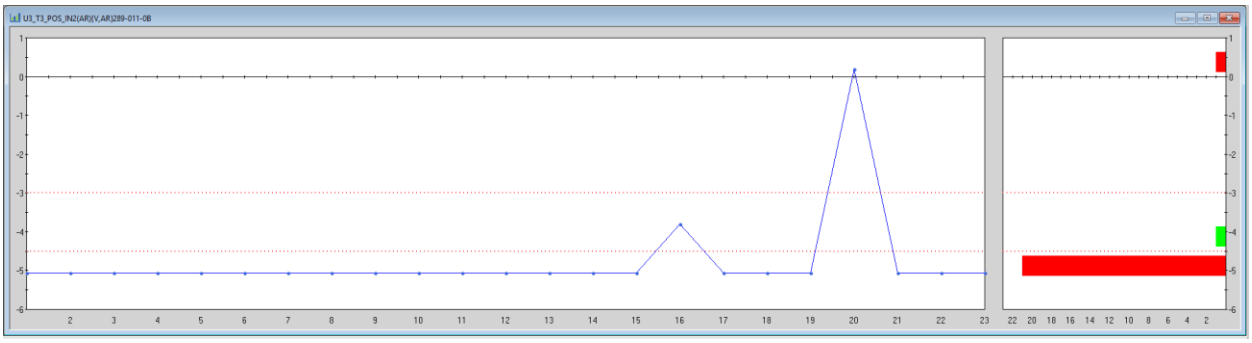
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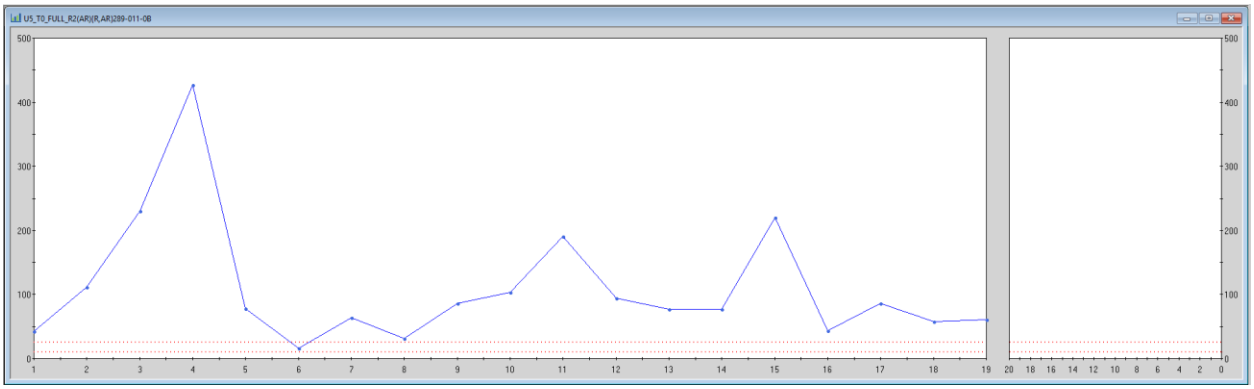
1
0
-1
-2
-3
-4
-5
-6
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
22 20 18 16 14 12 10 8 6 4 2

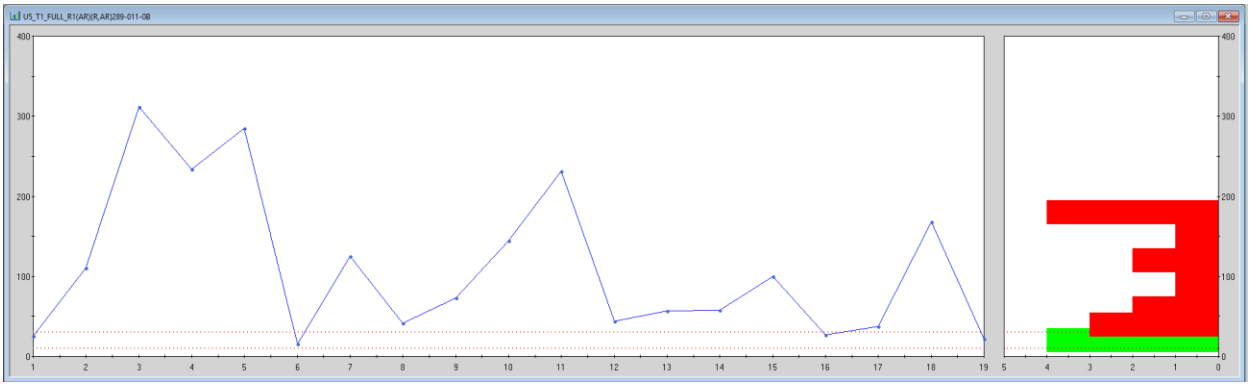
Digital Potentiometer AD5262BRU20

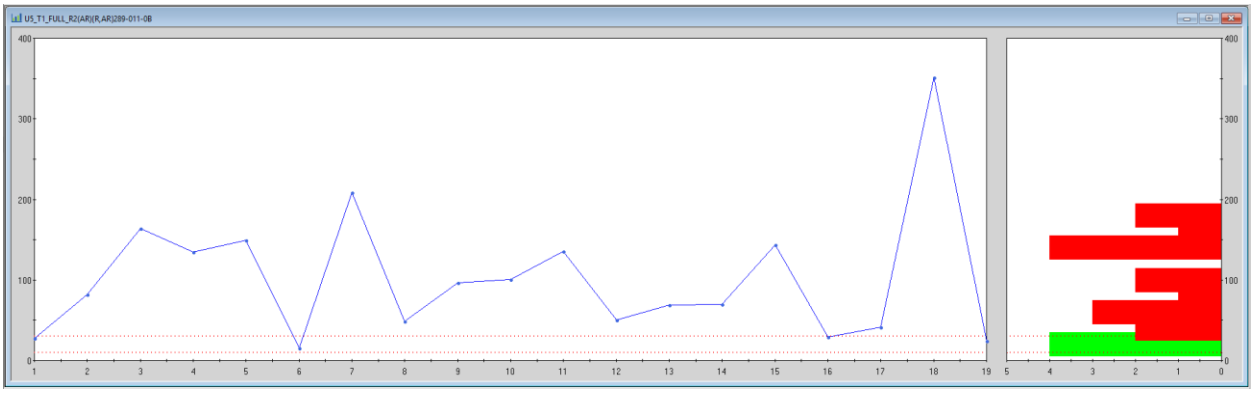
U5_Tx

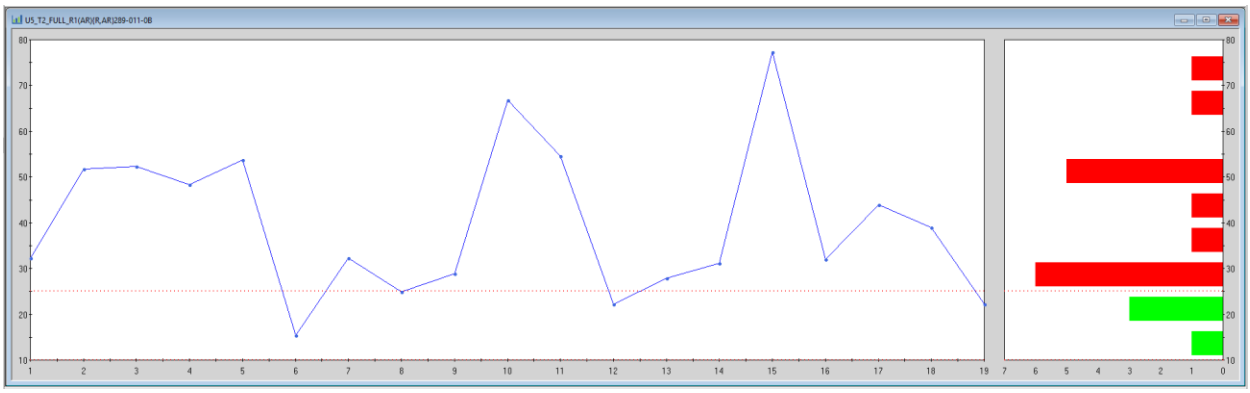
In this graphics S/N 990D5AA was removed.

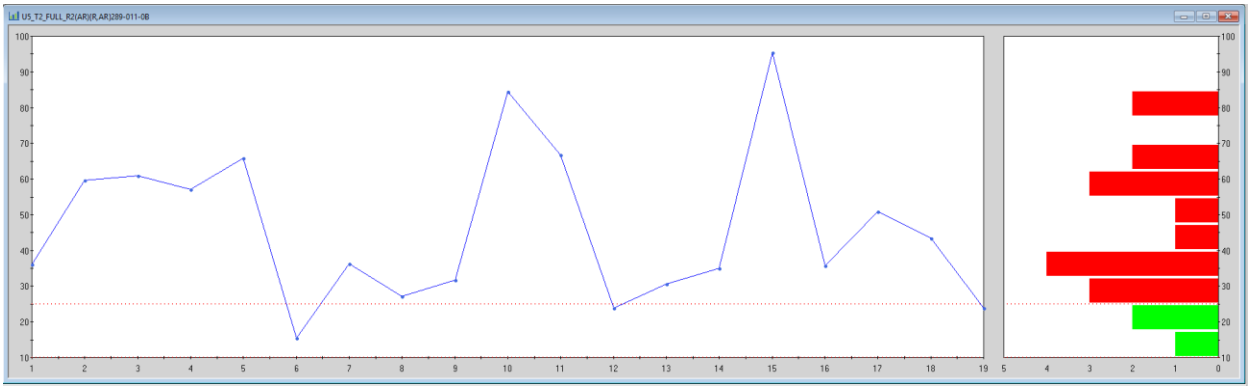
This problem was fixed, voltage level was increased from 200mv to 250mV








U5_T2_FULL_R1(AR)(R,AR)289-011-0B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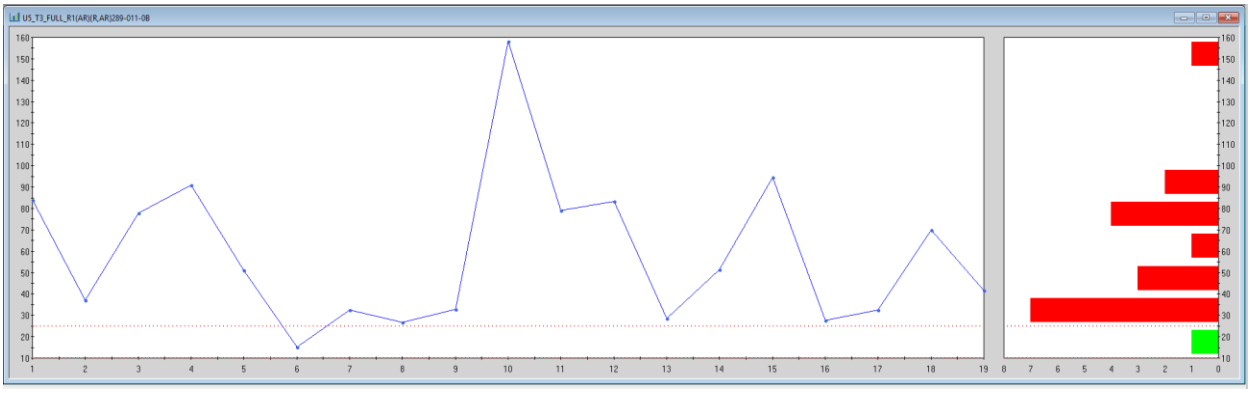
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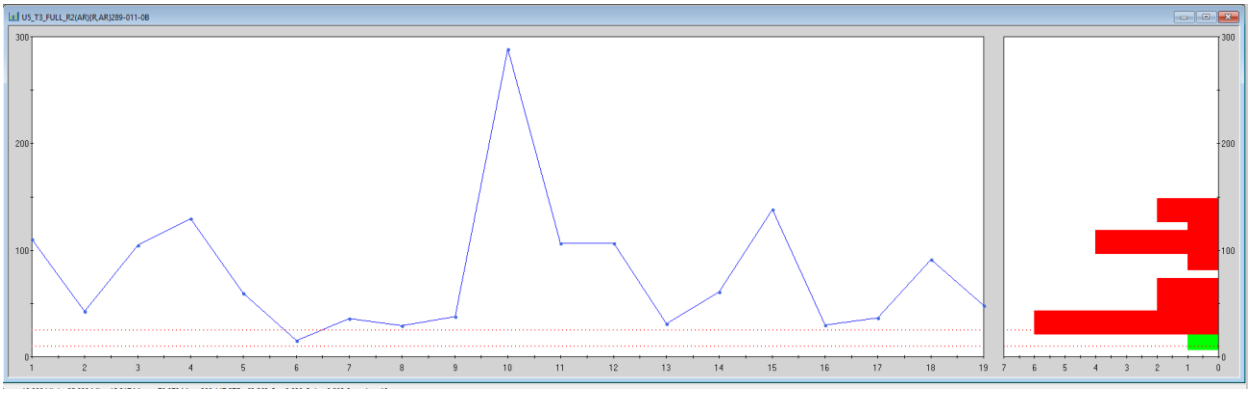
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Cpk of Previous Running with 16 Good PCBAs

In terms of Cpk, the previous production batch, show cpk values higher than 1.33

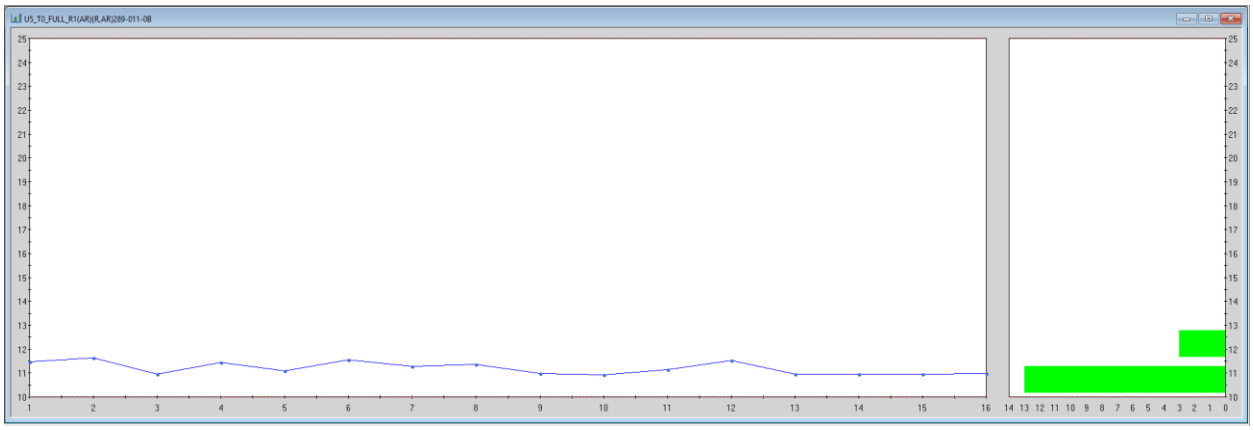
U1_Tx, U2_Tx & U3_Tx

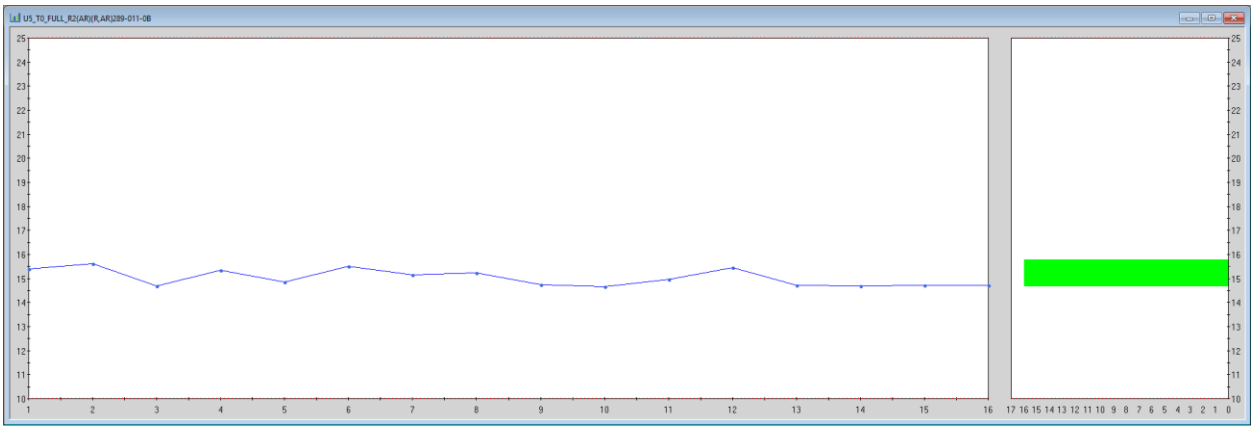
Part	Low	High	Min	Mean	Max	STD	Cp	Cpk	Samples
U1_T0_POS_IN1(AR){V,AR}	-4.500	-3.000	-3.933	-3.912	-3.880	0.017	14.612	11.457	16
U1_T1_POS_IN1(AR){V,AR}	-4.500	-3.000	-3.942	-3.918	-3.891	0.015	16.669	12.934	16
U1_T1_NEG_IN1(AR){V,AR}	3.000	4.500	3.750	3.784	3.802	0.017	14.526	13.867	16
U1_T2_POS_IN1(AR){V,AR}	-4.500	-2.000	-3.941	-3.927	-3.893	0.014	30.774	14.095	16
U1_T3_NEG_IN1(AR){V,AR}	3.000	4.500	3.755	3.791	3.823	0.016	15.415	14.577	16
U1_T0_NEG_IN1(AR){V,AR}	3.000	4.500	3.757	3.780	3.807	0.016	15.348	14.726	16
U1_T2_NEG_IN1(AR){V,AR}	3.000	4.500	3.768	3.792	3.808	0.012	21.468	20.258	16
U1_T3_POS_IN1(AR){V,AR}	-4.500	-2.000	-3.936	-3.925	-3.909	0.009	46.750	21.522	16
U2_T0_POS_IN1(AR){V,AR}	-900.000m	-400.000m	-749.642m	-734.419m	-720.146m	10.106m	8.246	5.462	16
U2_T3_POS_IN1(AR){V,AR}	-900.000m	-400.000m	-751.564m	-732.284m	-722.388m	8.106m	10.280	6.896	16
U2_T2_POS_IN1(AR){V,AR}	-900.000m	-400.000m	-745.158m	-732.172m	-720.050m	7.197m	11.579	7.773	16
U2_T1_NEG_IN2(AR){V,AR}	400.000m	900.000m	765.399m	773.175m	782.373m	5.309m	15.697	7.963	16
U2_T1_NEG_IN1(AR){V,AR}	400.000m	900.000m	765.911m	773.534m	782.853m	5.199m	16.028	8.108	16
U2_T3_NEG_IN1(AR){V,AR}	400.000m	900.000m	766.776m	772.433m	781.508m	4.625m	18.017	9.194	16
U2_T3_NEG_IN2(AR){V,AR}	400.000m	900.000m	766.808m	772.233m	780.868m	4.516m	18.455	9.432	16
U2_T1_POS_IN1(AR){V,AR}	-900.000m	-400.000m	-746.888m	-731.955m	-721.907m	5.930m	14.053	9.446	16
U2_T2_NEG_IN2(AR){V,AR}	400.000m	900.000m	765.623m	773.646m	781.797m	3.971m	20.987	10.607	16
U2_T1_POS_IN2(AR){V,AR}	-900.000m	-400.000m	-751.532m	-743.041m	-734.974m	4.763m	17.494	10.984	16
U2_T2_NEG_IN1(AR){V,AR}	400.000m	900.000m	766.168m	773.710m	781.925m	3.803m	21.912	11.069	16
U2_T2_POS_IN2(AR){V,AR}	-900.000m	-400.000m	-751.500m	-744.292m	-736.639m	4.663m	17.870	11.130	16
U2_T3_POS_IN2(AR){V,AR}	-900.000m	-400.000m	-751.788m	-743.007m	-734.590m	4.637m	17.971	11.285	16
U2_T0_NEG_IN1(AR){V,AR}	400.000m	900.000m	768.826m	774.420m	784.038m	3.489m	23.882	11.996	16
U2_T0_NEG_IN2(AR){V,AR}	400.000m	900.000m	768.474m	773.902m	783.046m	3.417m	24.387	12.301	16
U2_T0_POS_IN2(AR){V,AR}	-900.000m	-400.000m	-749.514m	-744.258m	-734.526m	4.211m	19.791	12.329	16
U3_T0_POS_IN2(AR){V,AR}	-4.000	-3.300	-3.904	-3.882	-3.843	0.019	5.995	2.029	16
U3_T0_POS_IN1(AR){V,AR}	100.000m	1.000	187.258m	193.233m	198.852m	3.562m	42.115	8.726	16
U3_T0_NEG_IN1(AR){V,AR}	-1.000	-100.000m	-211.630m	-205.930m	-200.389m	3.541m	42.366	9.973	16
U3_T1_POS_IN1(AR){V,AR}	100.000m	1.000	190.653m	194.150m	199.845m	2.381m	62.998	13.181	16
U3_T1_NEG_IN1(AR){V,AR}	-1.000	-100.000m	-208.908m	-205.315m	-199.364m	2.566m	58.449	13.679	16
U3_T0_NEG_IN2(AR){V,AR}	3.000	4.500	3.710	3.750	3.771	0.018	13.933	13.923	16
U3_T3_POS_IN2(AR){V,AR}	-4.500	-3.000	-3.874	-3.859	-3.822	0.015	16.839	14.384	16
U3_T3_POS_IN1(AR){V,AR}	100.000m	1.000	190.717m	193.946m	197.219m	2.128m	70.473	14.712	16
U3_T1_POS_IN2(AR){V,AR}	-4.500	-2.800	-3.902	-3.884	-3.856	0.013	21.166	15.329	16
U3_T2_POS_IN1(AR){V,AR}	100.000m	1.000	192.767m	196.356m	199.300m	2.028m	73.950	15.834	16
U3_T3_NEG_IN1(AR){V,AR}	-1.000	-100.000m	-208.588m	-205.149m	-201.638m	2.202m	68.128	15.919	16
U3_T2_NEG_IN1(AR){V,AR}	-1.000	-100.000m	-206.570m	-203.005m	-199.973m	2.050m	73.174	16.750	16
U3_T3_NEG_IN2(AR){V,AR}	3.000	4.500	3.688	3.714	3.727	0.014	18.410	17.530	16
U3_T1_NEG_IN2(AR){V,AR}	3.000	4.500	3.722	3.752	3.772	0.014	17.976	17.940	16
U3_T2_NEG_IN2(AR){V,AR}	3.000	4.500	3.734	3.753	3.770	0.010	24.510	24.397	16
U3_T2_POS_IN2(AR){V,AR}	-4.500	-3.000	-3.898	-3.886	-3.875	0.007	36.077	29.517	16

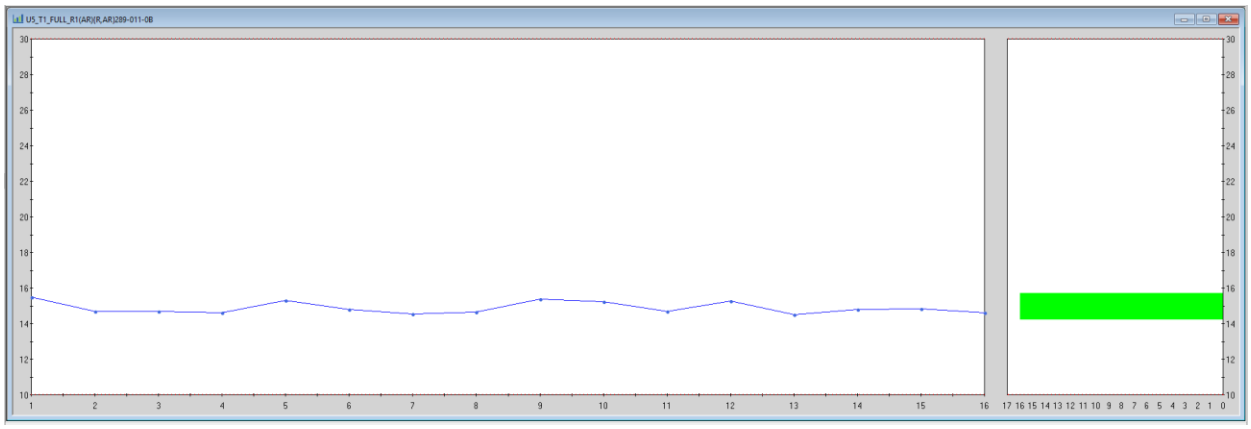
U5_Tx

Part	Low	High	Min	Mean	Max	STD	Cp	Cpk	Samples
U5_T0_FULL_R1(AR){R,AR}	10.000	25.000	10.932	11.204	11.647	0.261	9.593	1.539	16
U5_T0_FULL_R2(AR){R,AR}	10.000	25.000	14.663	15.030	15.625	0.347	7.194	4.825	16
U5_T1_FULL_R1(AR){R,AR}	10.000	30.000	14.518	14.885	15.493	0.331	10.061	4.915	16
U5_T1_FULL_R2(AR){R,AR}	10.000	30.000	14.582	14.939	15.548	0.328	10.164	5.019	16
U5_T3_FULL_R1(AR){R,AR}	10.000	25.000	14.496	14.930	15.511	0.292	8.566	5.631	16
U5_T3_FULL_R2(AR){R,AR}	10.000	25.000	14.556	14.983	15.566	0.289	8.642	5.741	16
U5_T2_FULL_R1(AR){R,AR}	10.000	25.000	14.614	14.873	15.370	0.188	13.287	8.633	16
U5_T2_FULL_R2(AR){R,AR}	10.000	25.000	14.686	14.932	15.410	0.182	13.751	9.044	16

Resistance Measurements of Previous Running with 16 Good PCBAs in U5_Tx



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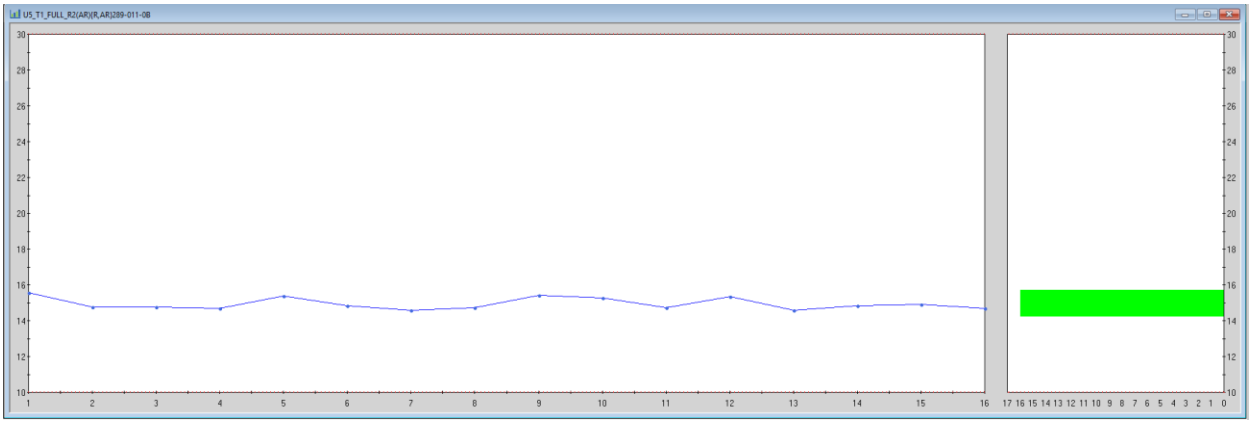
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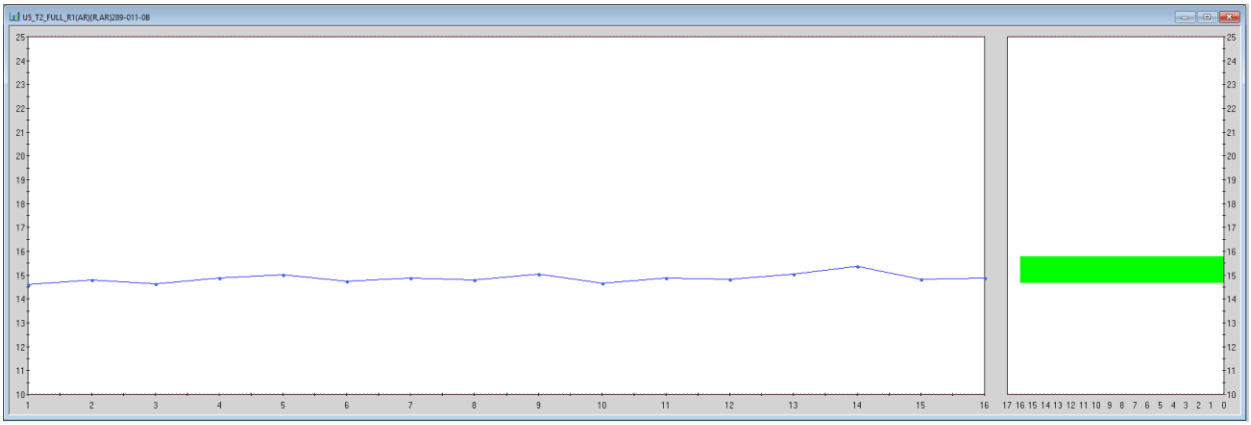
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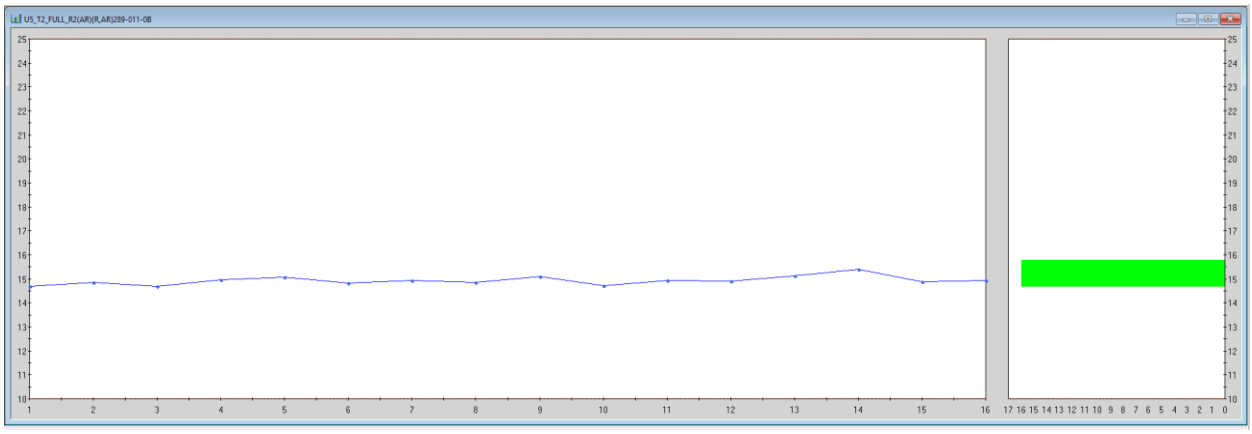
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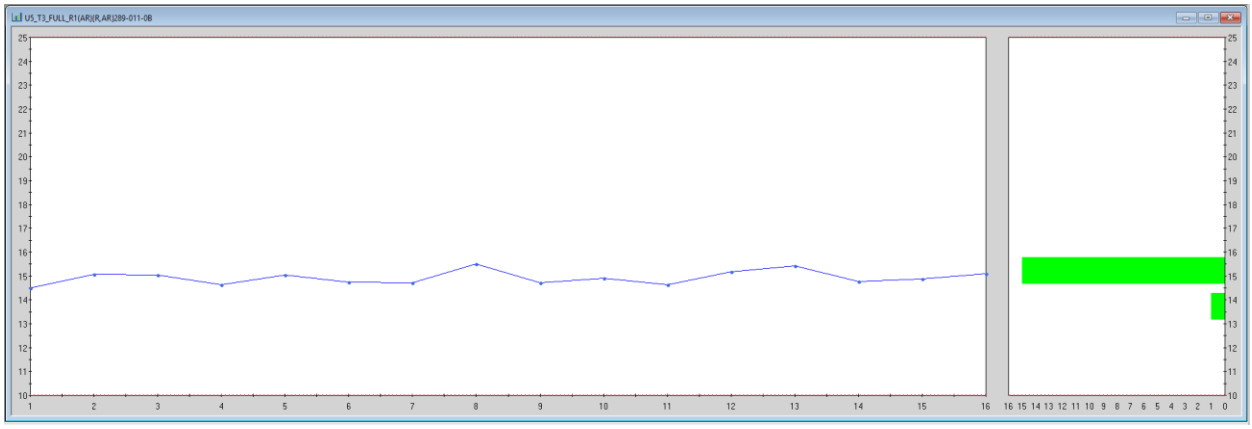
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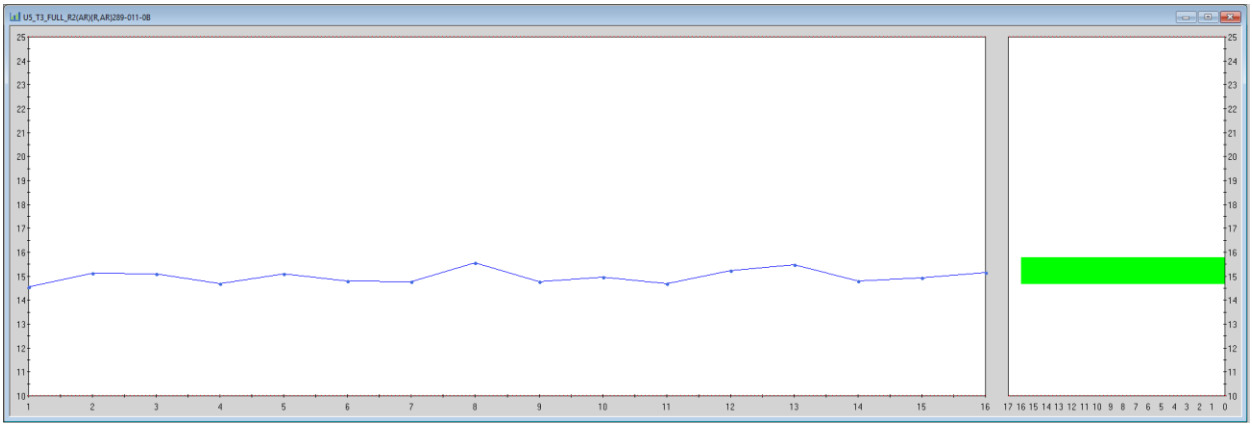
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