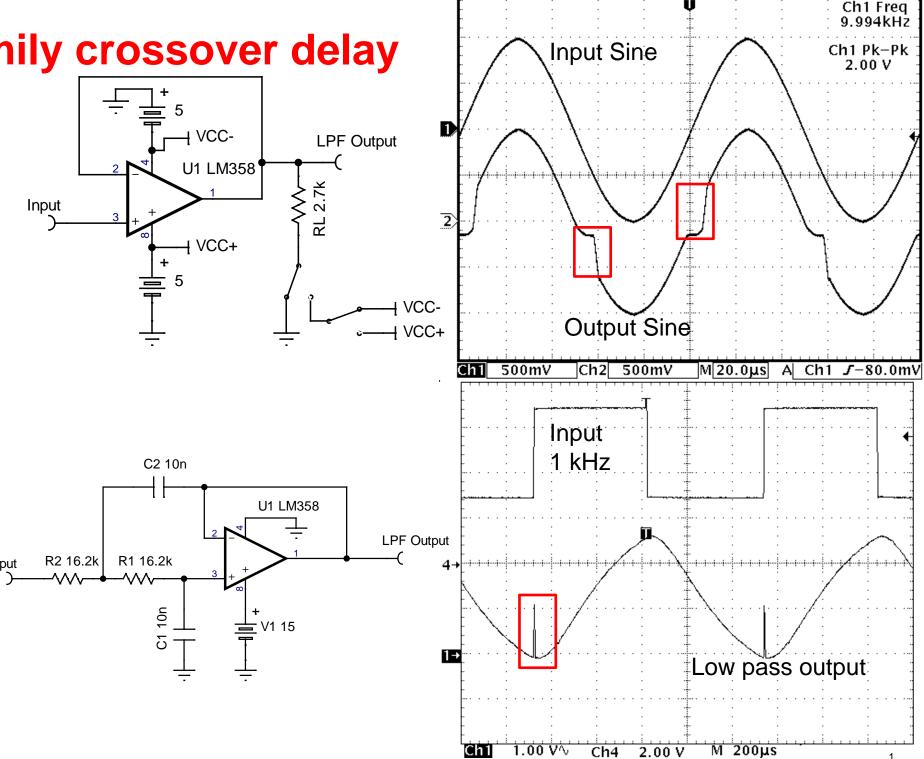
TS321, LM358, LM324 Family crossover delay

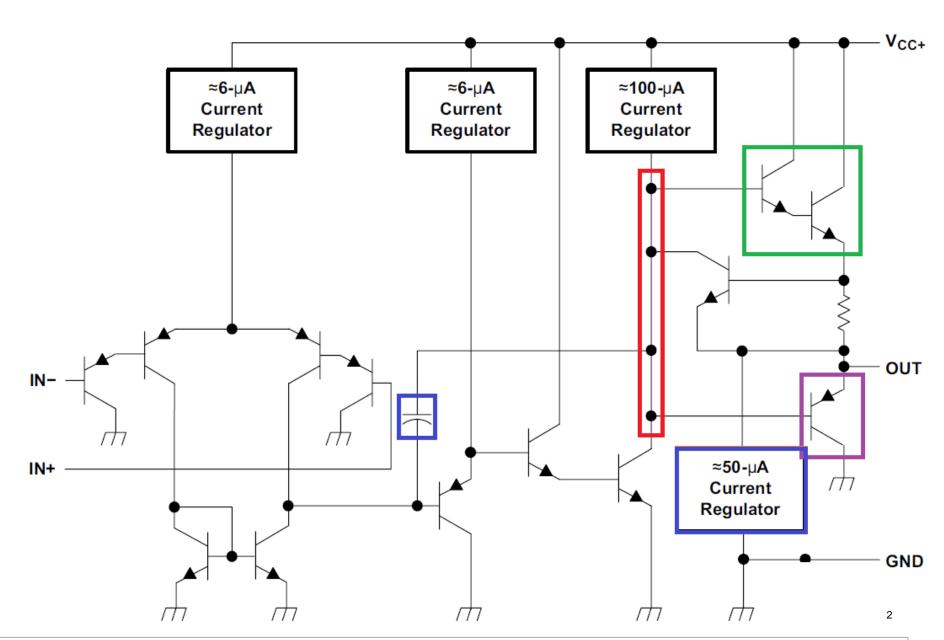
- Signal artifacts can occur internally as seen in unity gain amp (top) when load is terminated to mid-supply-rail.
- Signal artifacts can occur externally as seen in low pass filter amp (bottom) when input step current is capacitively coupled to output.
- In both cases, the root cause is the same. The output becomes high impedance (not open) while output stage switches between high current sink and high current source drivers.
- In both cases the solution is to ensure unidirectional output current. In top schematic terminate load to VCC+ or VCC-. In bottom schematic add pullup or pull down resistor.
- Next slide covers reason for the delay.





TS321, LM358, LM324 Family crossover delay

- The crossover delay is a side effect of the unique output structure.
- There is a low impedance Darlington NPN source current driver (green) with a 1.5V to 2V headroom requirement. This limits VOH level.
- There is emitter follower sink current driver (purple) with a 0.7V headroom requirement. So it cant' provide sink current when OUT is near GND.
- There is a 2nd weaker constant current sink driver (blue) that has a high impedance, and low VOL at light load.
- The red node controls the main source and sink drivers and has a 3-diodedrop dead-band between source and sink drive. The slew rate capacitor limits the slew rate of the red node.

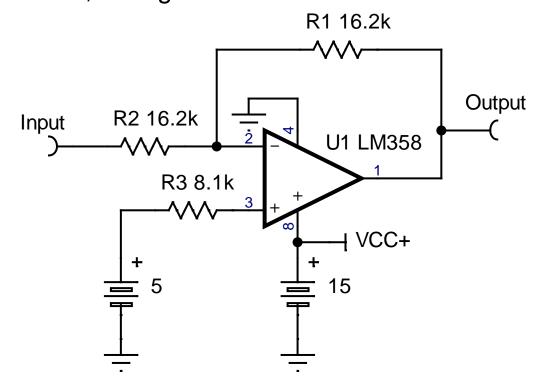




TS321, LM358, LM324 Family dual sink driver

- This inverting amplifier can't produce a VOL near zero because the current needed by the feedback resistor is >0.2mA.
- The load line intercepts the output curves between 0.43V and 0.77V depending on the device temperature.

If R1 and R2 are increased to 300k, then the load line intercepts well under 100mV at all temperatures. To cancel input bias current, change R3 set to 150k



Data sheet minimum current at 200mV is 12uA DS maximum voltage at 10k to ground is 20mV

