Modifying Configurations and Tolerances for Improved Convergence in PSpice for TI

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PSPICE Convergence FAQ

- What is convergence?
  - Convergence is when an electrical simulator is able to find a solution to a circuit. Many different factors influence convergence.
- What can cause a failure to converge?
  - Improper connections, faulty spice models, tight tolerances, and oscillations
- How can I make my simulation converge?
  - Fix glaring circuit issues (PWR and GND connections, current directions)
  - Simplify circuit
  - Check 3rd party models first, then TI models (isolate and simulate)
  - Modify
    - Auto-Converge
    - Tolerances
    - Simulation Conditions
  - The parameters above will be discussed in the following slides

Tolerances Overview

- What are tolerances in PSpice for TI?
  - Tolerances are how much error/iterations will be accepted when finding a circuit's solution
  - Loosening tolerances can help the simulation converge and also speed up simulations
  - Larger tolerances mean the simulation is less accurate

(Recommended vs Default)

Name	Value	Default Value
SPEED_LEVEL	3	3
RELTOL	2m	0.001
VNTOL	1m	1.0u
ABSTOL	1n	1.0p
CHGTOL	0.01p	0.01p
GMIN	1.0E-12	1.0E-12
ITL1	150	150
ITL2	20	20
ITL4	10	10

Tolerances Definitions

- **RELTOL** – Relative accuracy of voltages and currents [%] – *Universal accuracy*
- **VNTOL** – Best accuracy of voltages [V] – *Smaller values are ignored*
- **ABSTOL** – Best accuracy of currents [A] – *Smaller values are ignored*
- **CHGTOL** – Best accuracy of charges [C] – *Smaller values are ignored*
- **GMIN** – Minimum conductance for any branch [1/Ω] – *Added to nonlinear devices*
- **ITL1** – DC and bias “blind” iteration limit – *Maximum iterations*
- **ITL2** – DC and bias “best guess” iteration limit – *Maximum step iterations*
- **ITL4** – Transient time point iteration limit – *Maximum transient step iterations*
- **TSTOP** – Run to time [s]
- **TMAX** – Maximum step size [s]

PSpice for TI vs TINA-TI – Default Tolerances

Tolerance	PSpice for TI	TINA-TI
RELTOL	1m	10m
VNTOL	1u	10u
ABSTOL	1p	10u
CHGTOL	1p	10f
GMIN	1p	-
ITL1	150	1000
ITL2	20	40
ITL4	10	20

Recommended Steps to Fix Convergence Issues

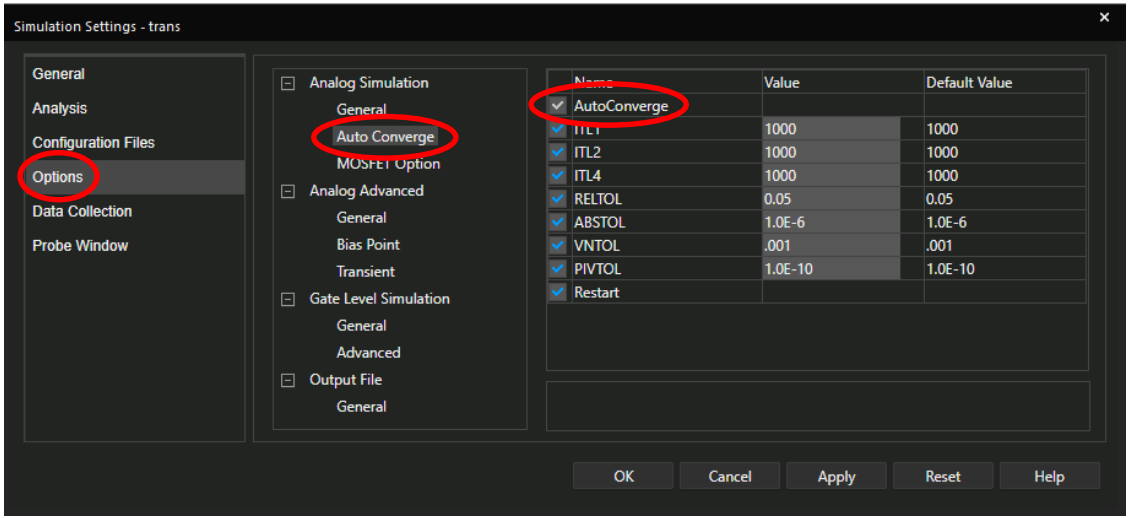
1. Enable AutoConverge and run simulation
2. Modify simulation tolerances
   a. Change ABSTOL to 100p
   b. Change VNTOL to 1m
   c. Change RELTOL to 2m
3. Modify pseudotransient options
   1. Change PTRANABSTOL to 10u
   2. Change PTRANVNTOL to 100u
4. Set the initial conditions (IC) of capacitors to 0
5. If transient:
   a. Check the “Skip initial transient bias point calculation” (SKIPBP) checkbox
   b. Switch power supplies to pulse and start at 0

Note: Each step reduces simulation accuracy, especially RELTOL.

Try running your simulation with each step!

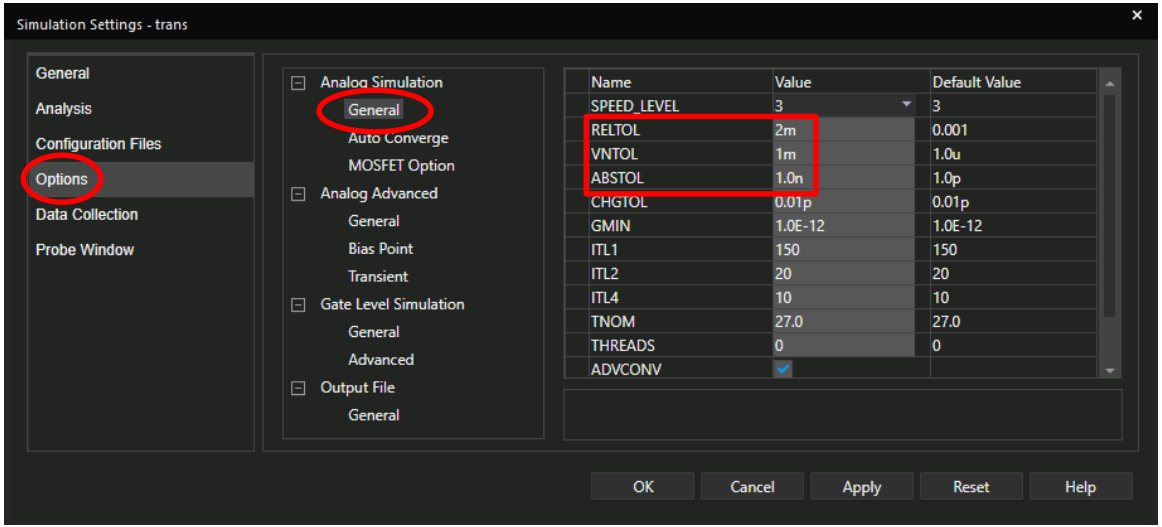
Step 1: Enabling AutoConverge

1. Go to Edit Simulation Profile
2. Go to Options > Analog Simulation > Auto Converge
3. Check AutoConverge
4. Click Apply and then OK



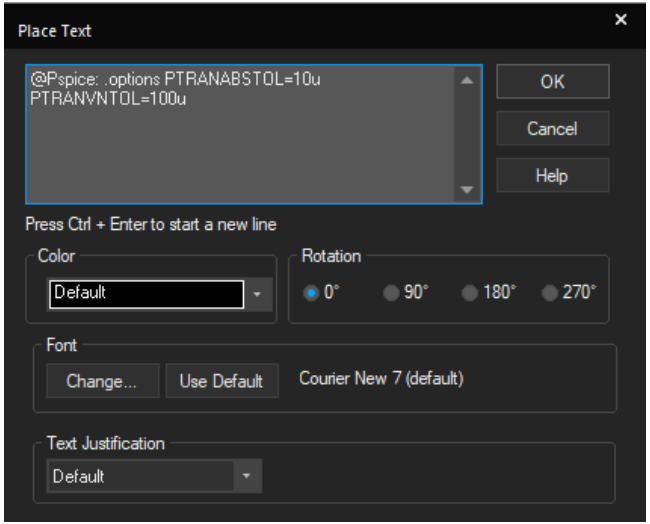
Step 2: Changing Tolerances

1. Go to Edit Simulation Profile
2. Go to Options > Analog Simulation > General
3. Change ABSTOL to 1n
4. Change VNTOL to 1m
5. Change RELTOL to 2m
6. Click Apply and then OK



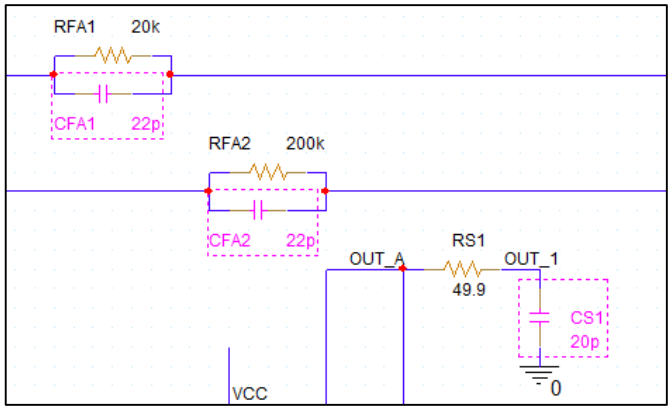
Step 3: Changing Pseudotransient Options

1. In your schematic, go to Place > Text (or use the hotkey “T”)
2. Type “@Pspice: .options PTRANABSTOL=10u PTRANVNTOL=100u”
3. Click OK and place text in schematic

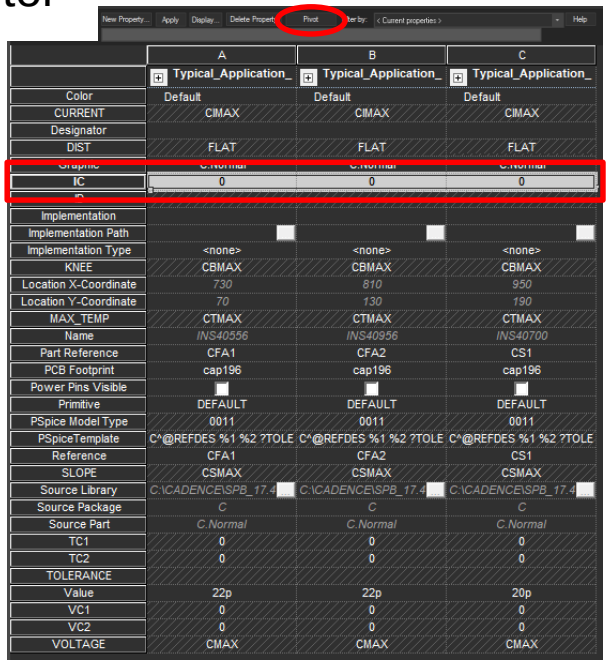


Step 4: Setting CAP Initial Conditions

1. CTRL+LeftClick to highlight multiple capacitors
2. LeftClick a capacitor twice to open Property Editor
3. Change all IC fields to 0
4. Click Apply and then close Property Editor

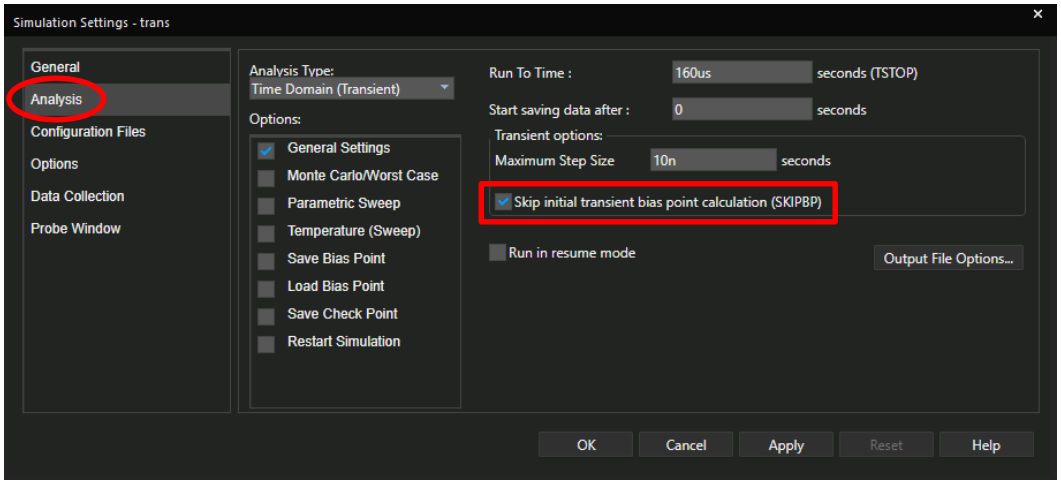


Click Pivot if properties are horizontal for easier viewing!



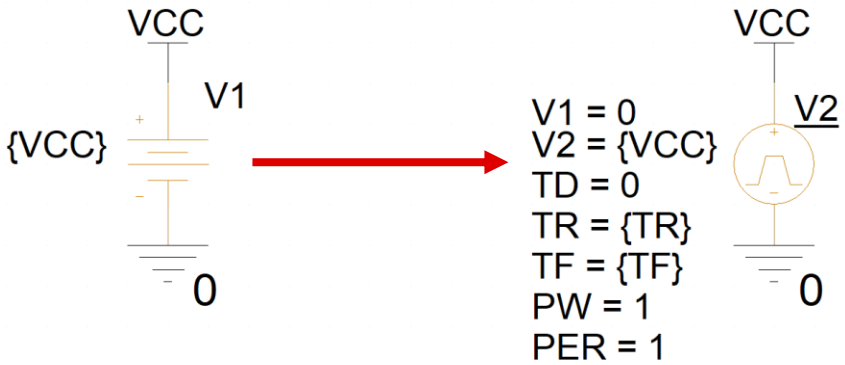
Step 5a (Transient) : Check SKIPBP

1. Go to Edit Simulation Profile
2. Go to Analysis
3. Check Skip initial transient bias point calculation (SKIPBP)
4. Click Apply and then OK

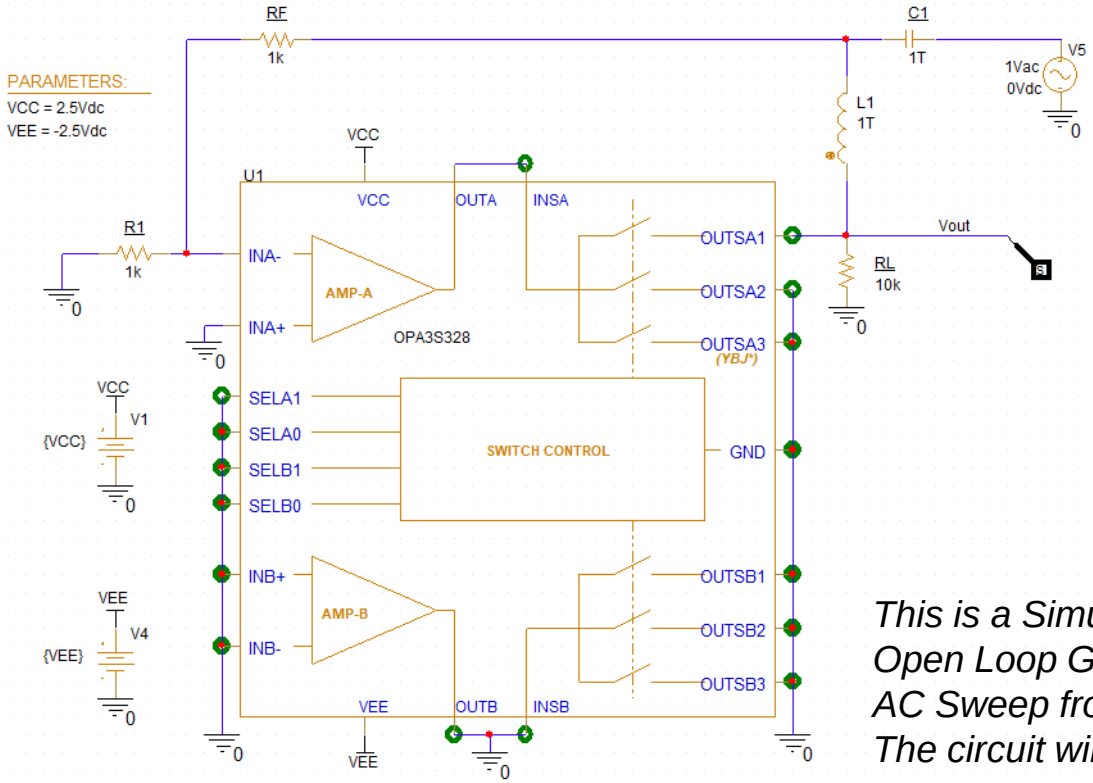


Step 5b (Transient): Use pulse power supplies

1. Go to Place > PSpice Component > Source > Voltage Sources > Pulse
2. Configure V1 as 0 and V2 as the desired VDD
3. Configure TD as 0
4. Calculate TR, TF as at least $(100ns * \frac{VCC}{5\ V})$
5. Configure PW and PER as longer than simulation time



Non-Convergence Example

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Convergence problem in bias point calculation

These voltages failed to converge:

V(VOUT)              = -540.38e-27V \    2.435V
V(X_U1.X_OPAx328_A.N3116503) =    52.44V \    54.28V
V(X_U1.X_OPAx328_A.N3116515) =   122.55mV \    1.076V
V(X_U1.X_OPAx328_A.VIMON) =   -1.436mV \   243.48mV
V(X_U1.X_OPAx328_A.N3117073) =    26.28V \   230.52V
ERROR(ORPSIM-15661): 5 of 5 errors shown. See output file for complete list

These supply currents failed to converge:

I(L_L1)              =   -5.408nA \   13.18fA
I(X_U1.X_OPA3S328_SWITCH.X_U22.L_L1) =   729.74pA \   243.48uA
I(X_U1.X_OPA3S328_SWITCH.X_U22.L_L2) =   729.86pA \   243.48uA
I(V_V1)              =   -13.60mA \   -13.84mA
I(V_V5)              =   -5.408nA \   63.18fA
ERROR(ORPSIM-15661): 5 of 34 errors shown. See output file for complete list
ERROR(ORPSIM-15660): These devices failed to converge
   X_U1.X_OPA3S328_SWITCH.X_U22.X_U1.E22
   X_U1.X_OPAx328_A.X_U26.G1
   X_U1.X_OPAx328_A.X_U27.G1
   X_U1.X_OPA3S328_SWITCH.X_U38.GD1
   X_U1.X_OPA3S328_SWITCH.X_U41.GD1
ERROR(ORPSIM-15661): 5 of 5 errors shown. See output file for complete list
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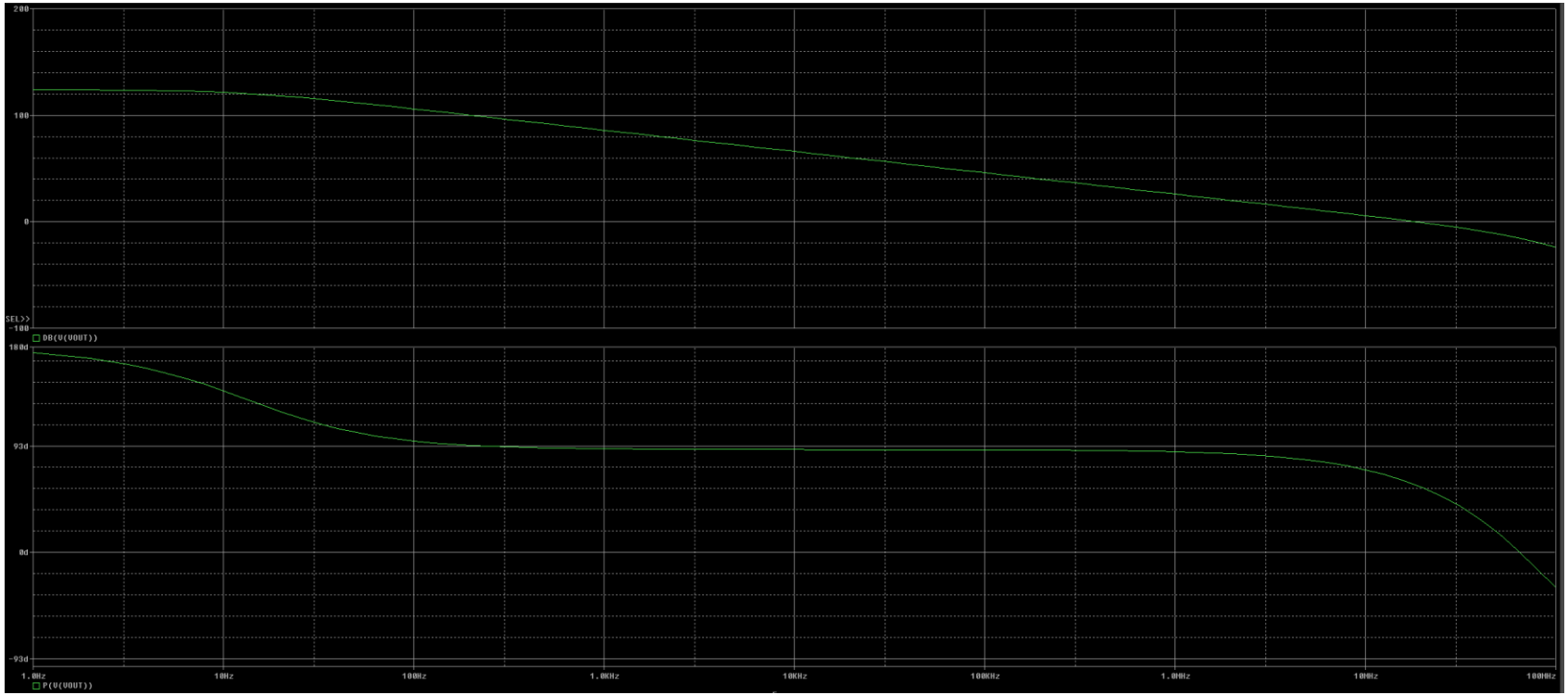
This is a Simulation Configuration for the Open Loop Gain (A_{OL}) of the OPA3S328
AC Sweep from 1 Hz – 100 MHz
The circuit will not converge with default settings

Non-Convergence Example - Results



After enabling AutoConverge (Step 1), the simulation converges.
After modifying the tolerances (Step 2), the simulation converges 300% faster.