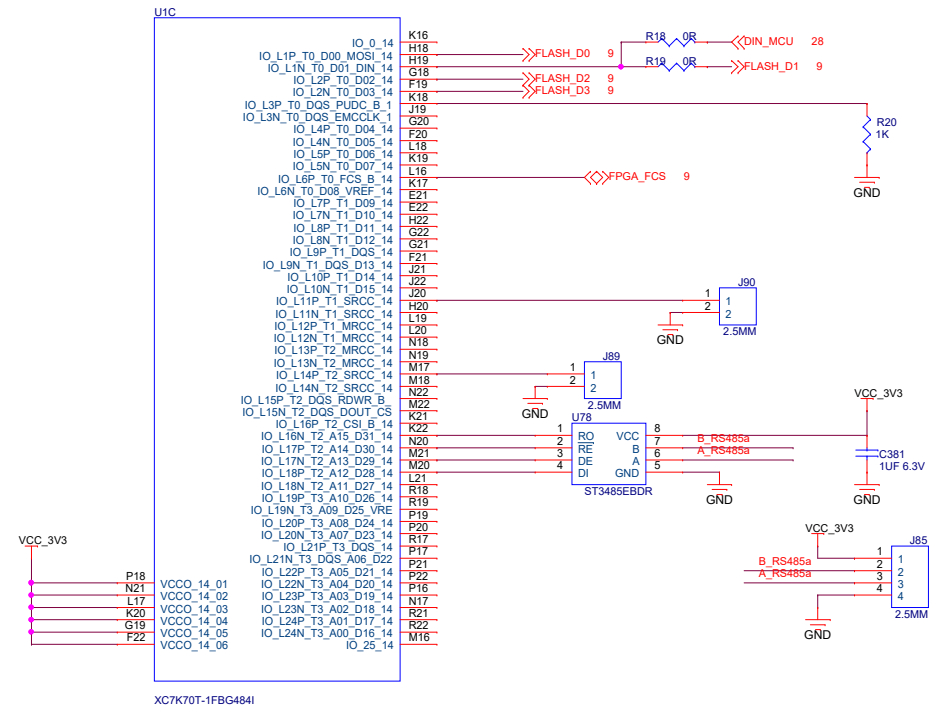
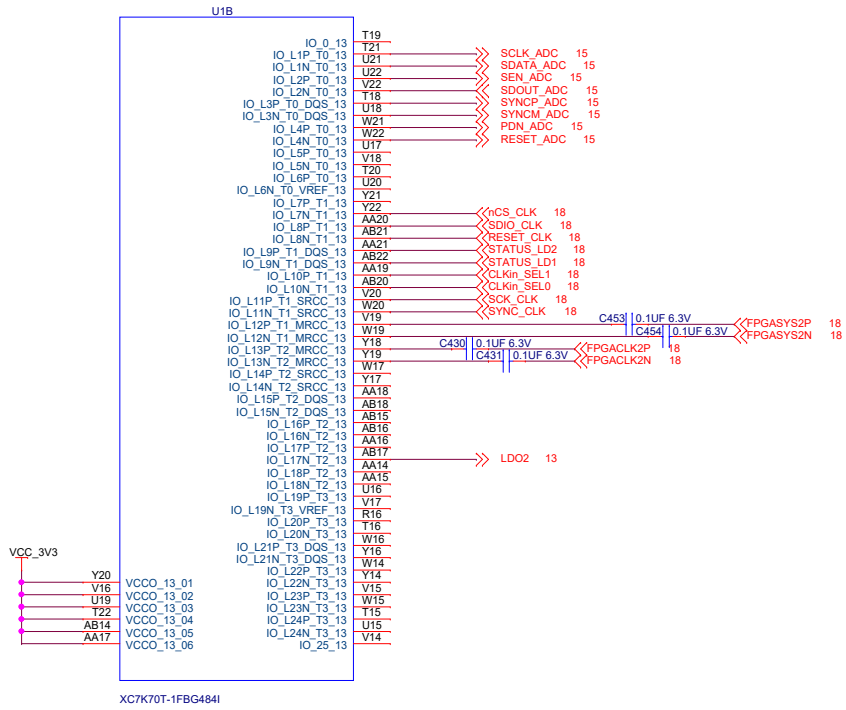
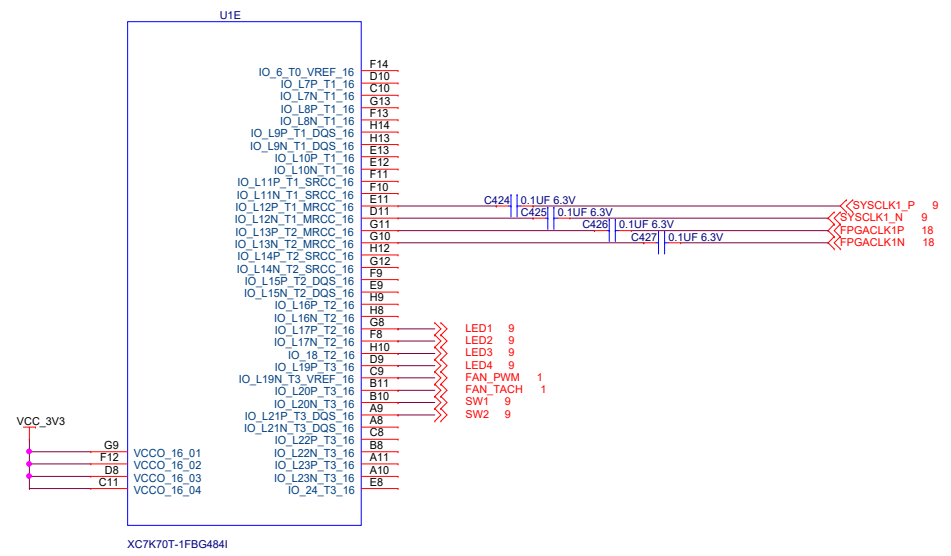
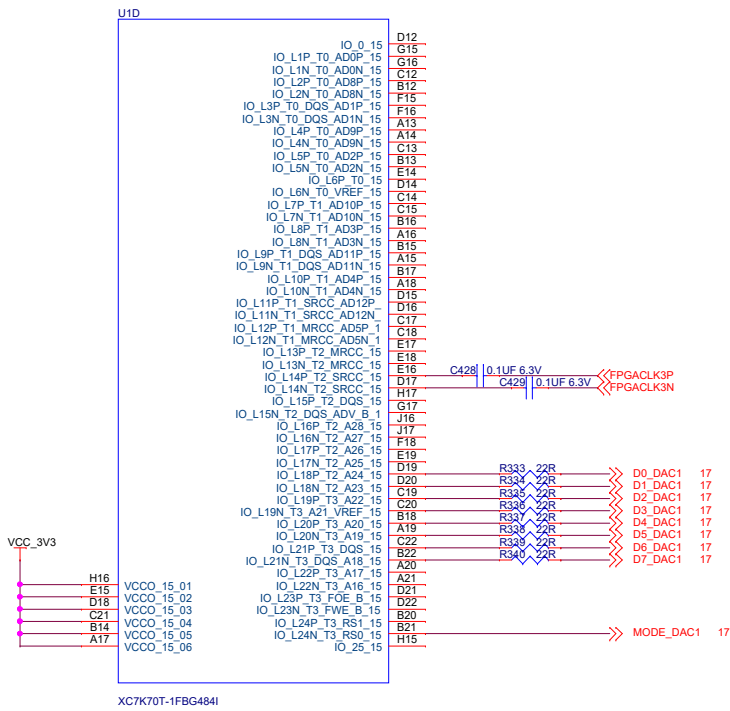


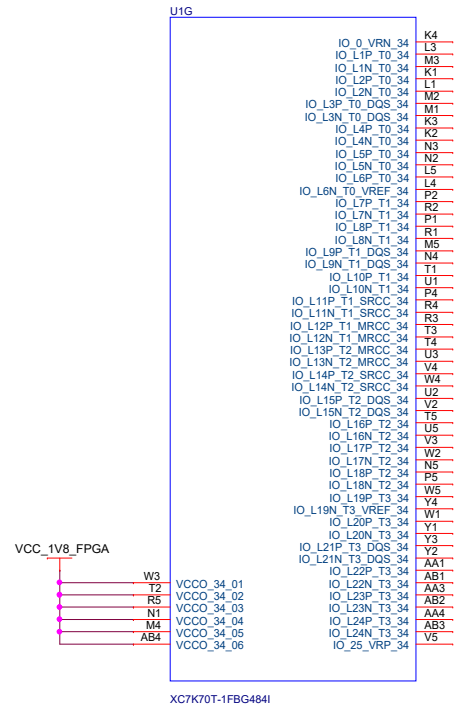
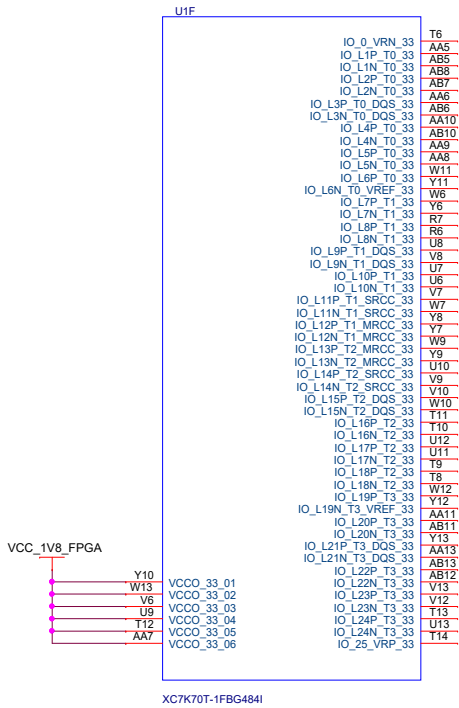
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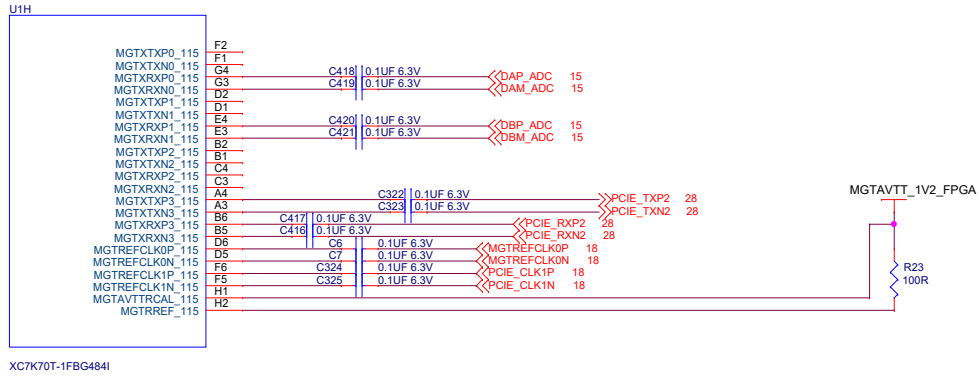
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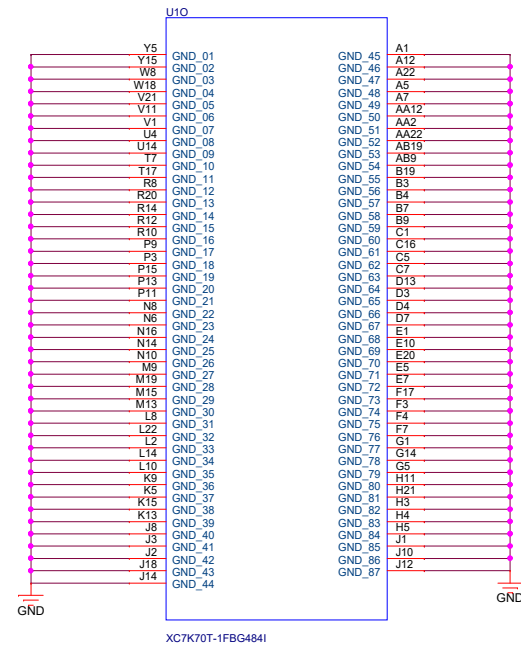
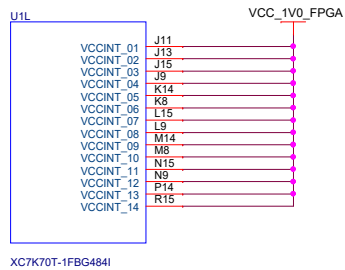
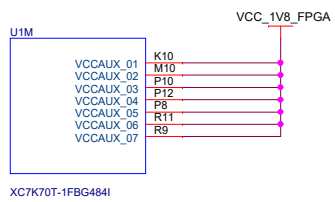
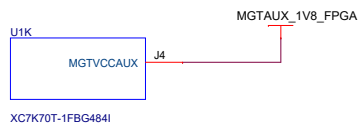
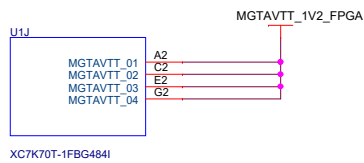
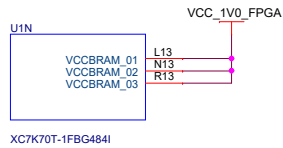
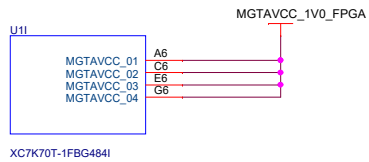
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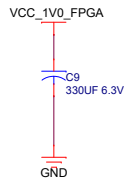
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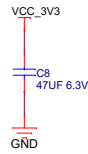
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# BYPASS CAPACITORS

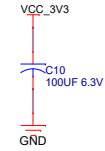
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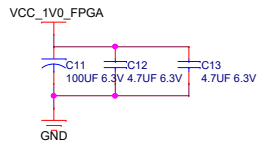
## Bank 0 1.5V VCCO



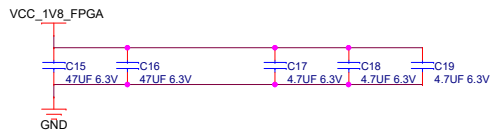
## Bank 13/14/15 1.5V VCCO



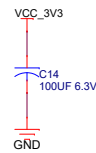
## VCCBRAM 100uF (1), 4.7uF (3) 0402



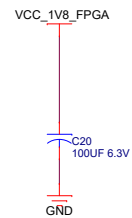
## VCCAUX 47uF



## Banks 16 3.3V VCCO



## Banks 33, 34 1.5V VCCO

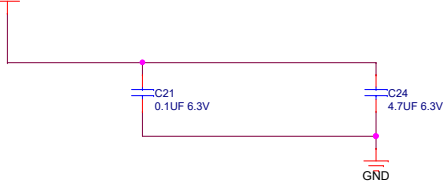


## FPGA Bypass Capacitors

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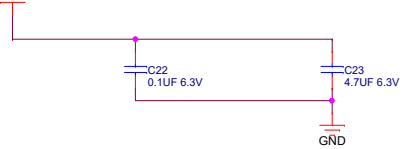
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MGTAVCC\_1V0\_FPGA



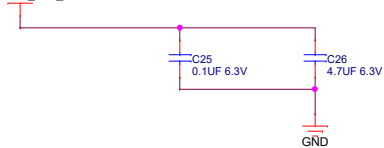
### MGTAVTT

MGTAVTT\_1V2\_FPGA



### MGTAUX

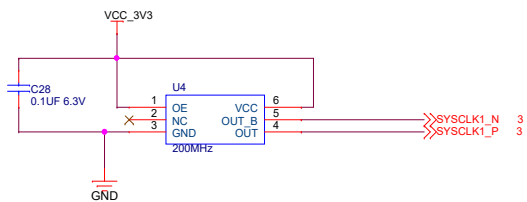
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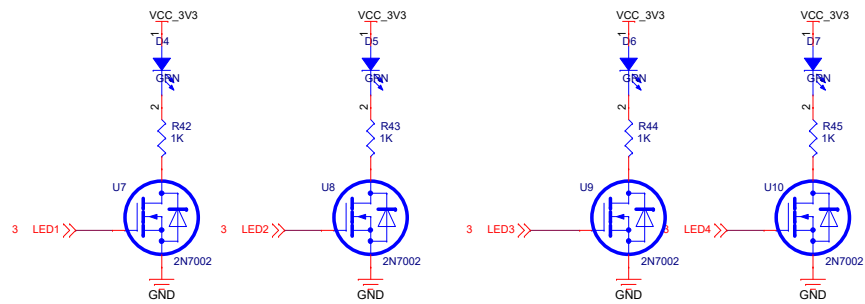
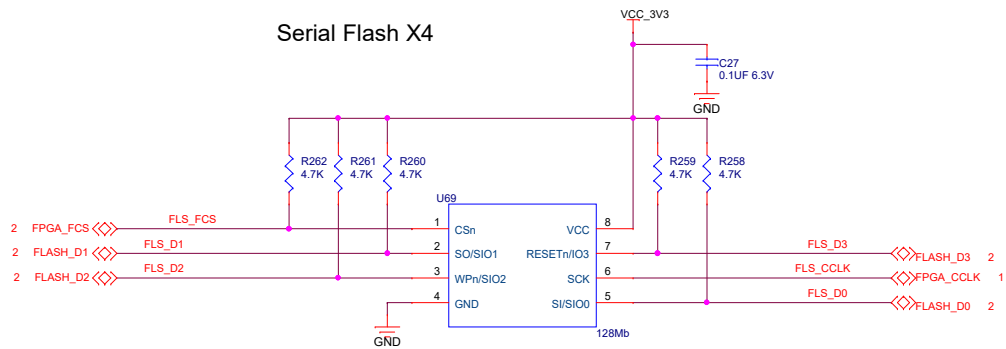
### FPGA MGT Bypass Capacitors

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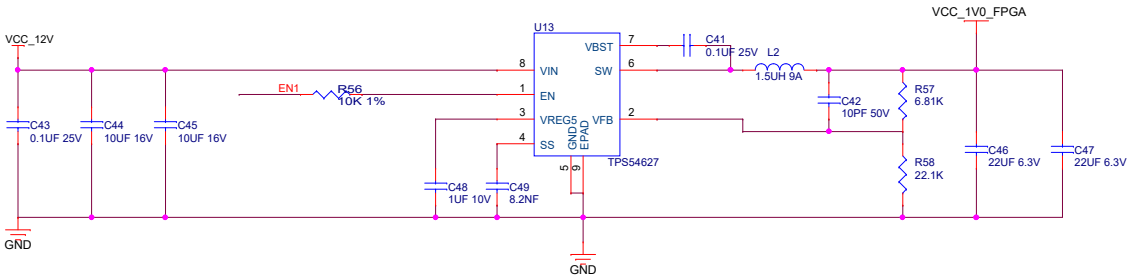
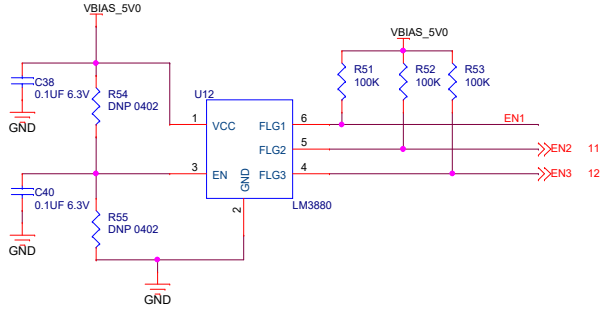
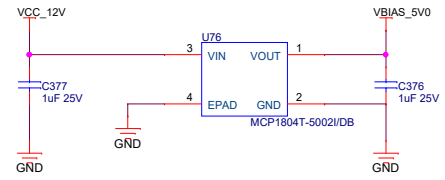
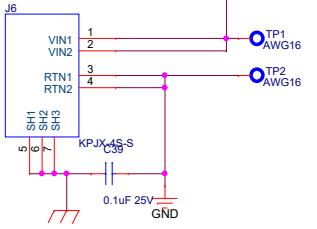
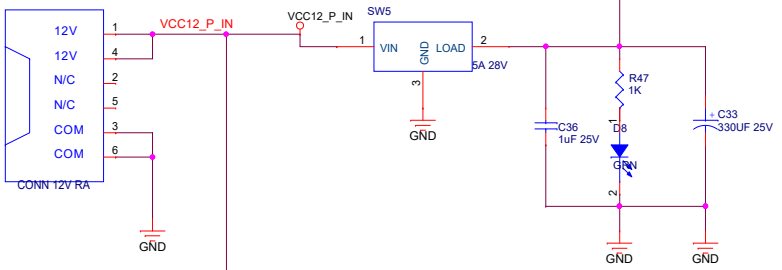
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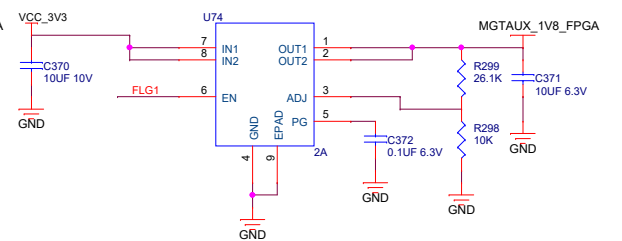
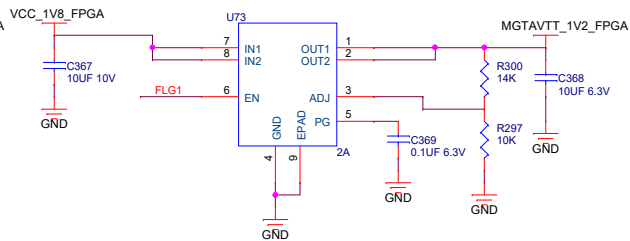
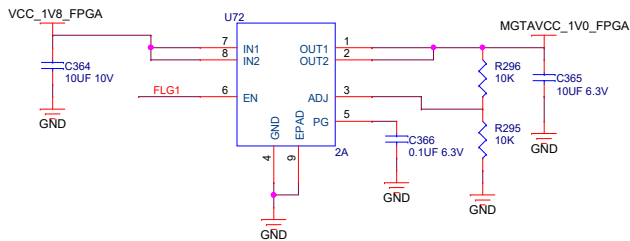
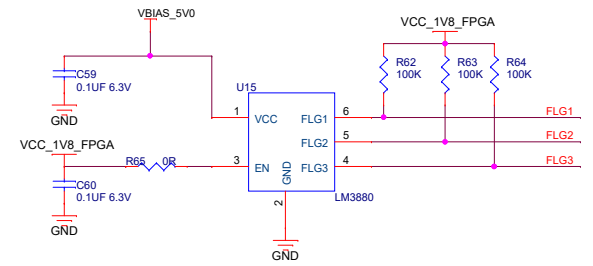
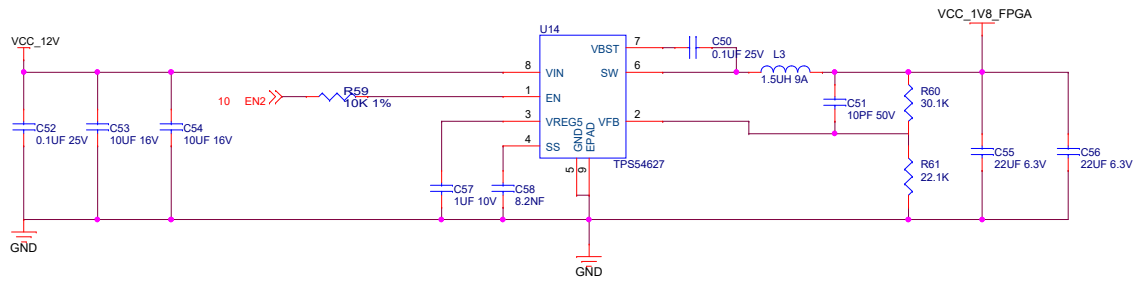
### FPGA JTAG, Clock, Flash, Buttons

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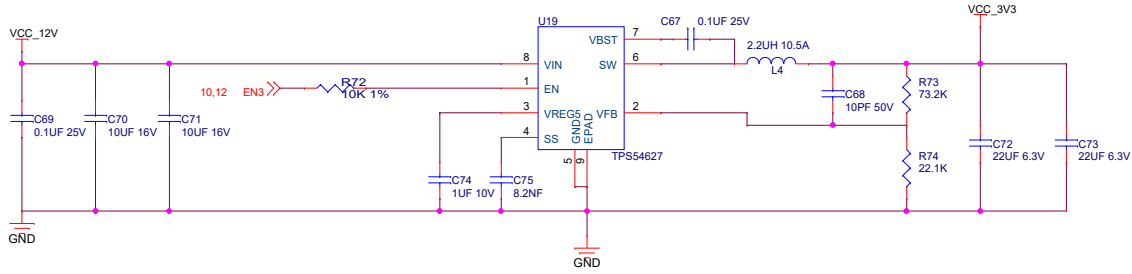
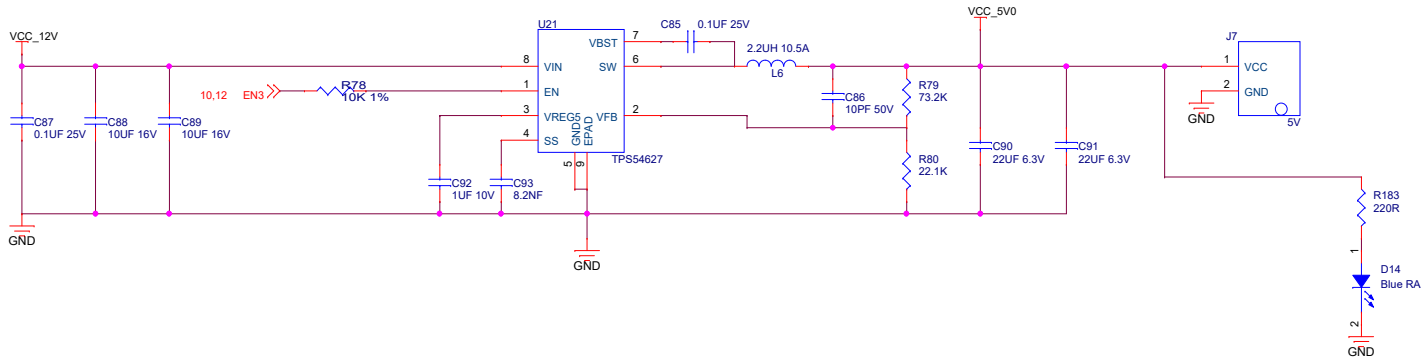
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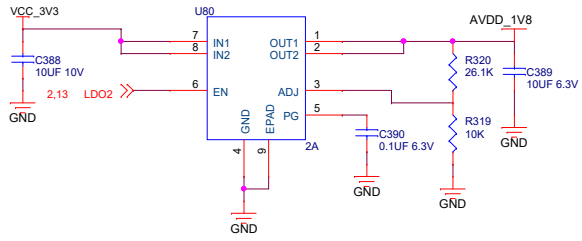
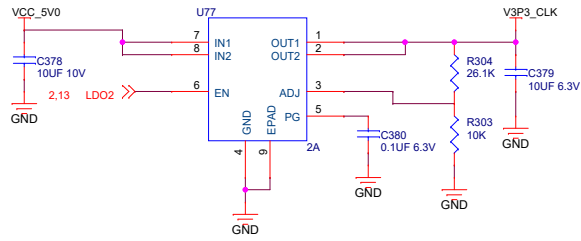
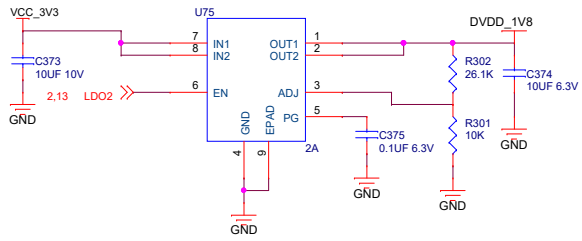
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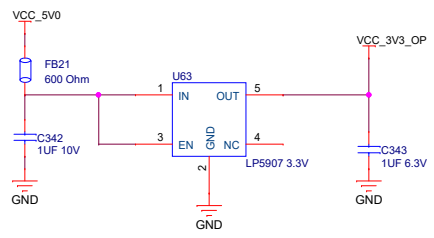
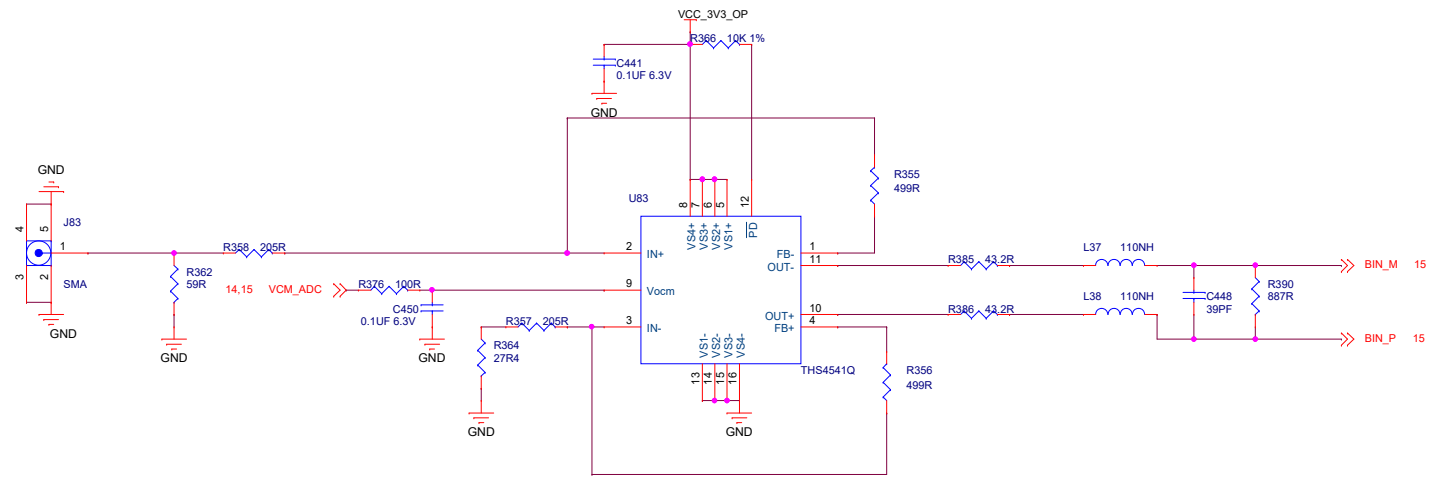
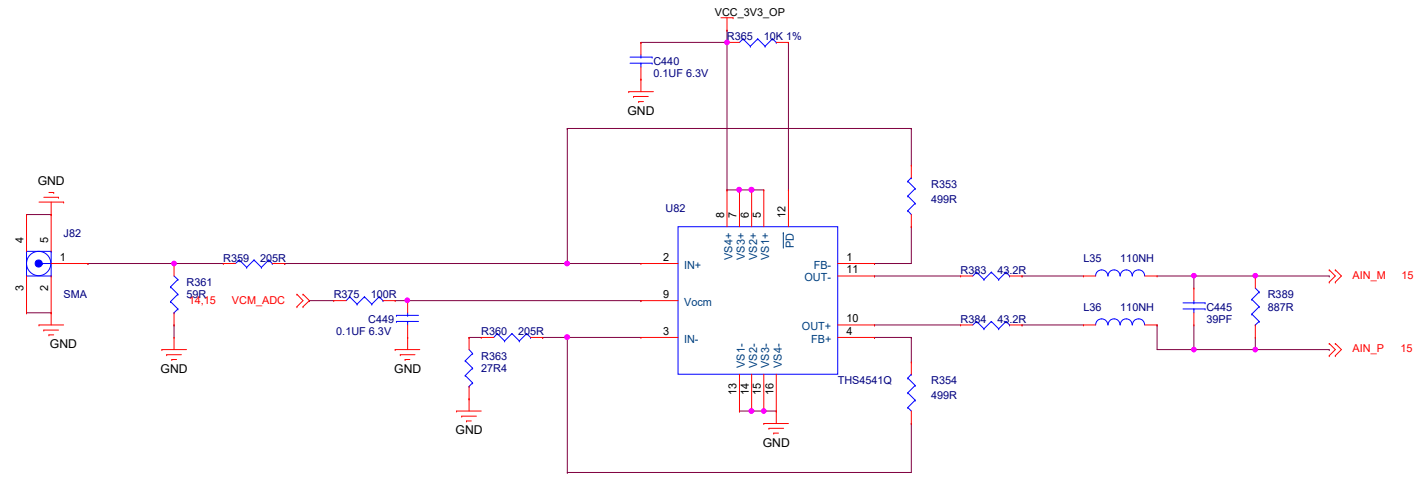
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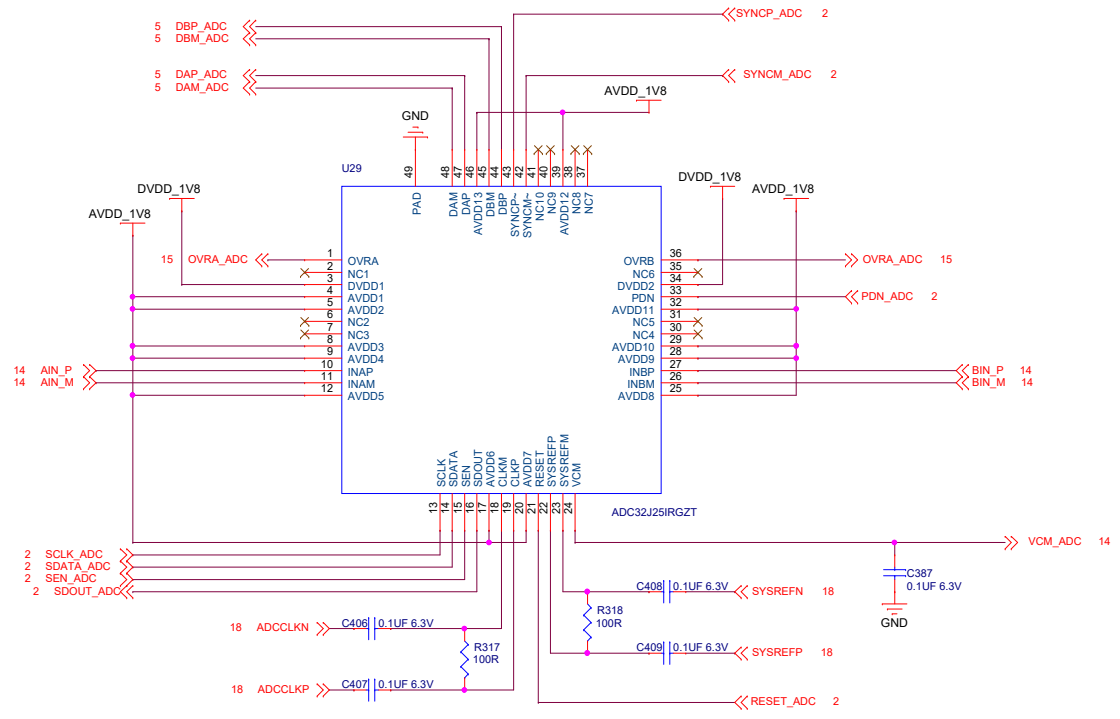
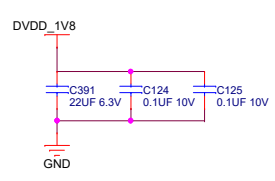
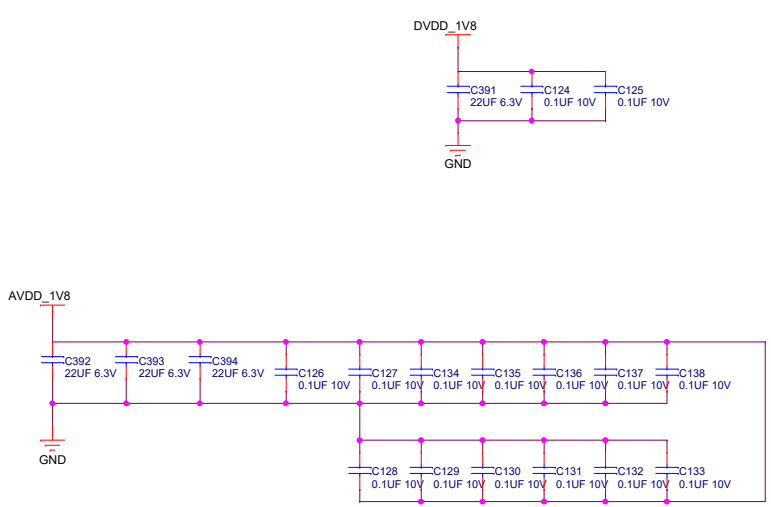
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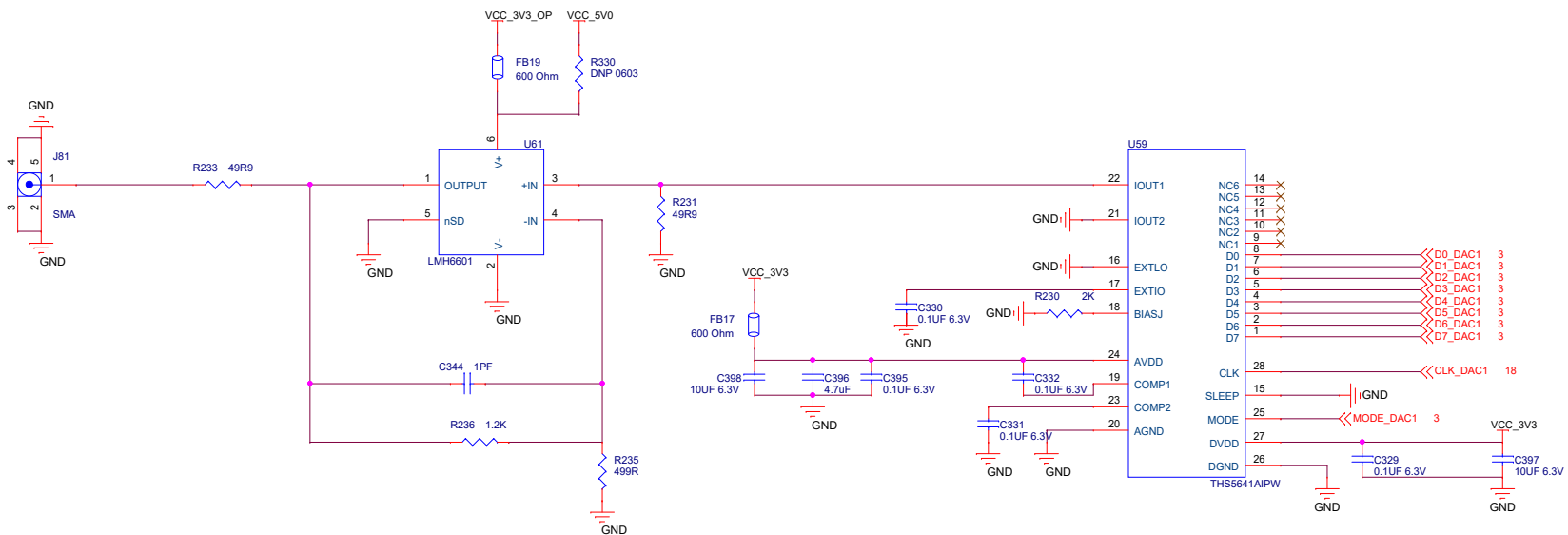
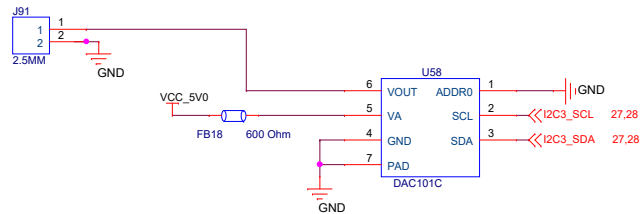
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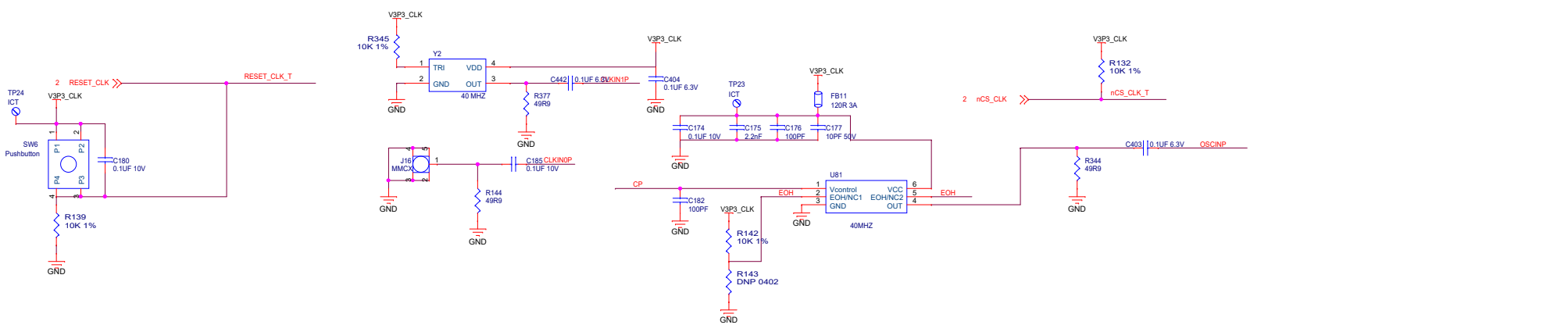
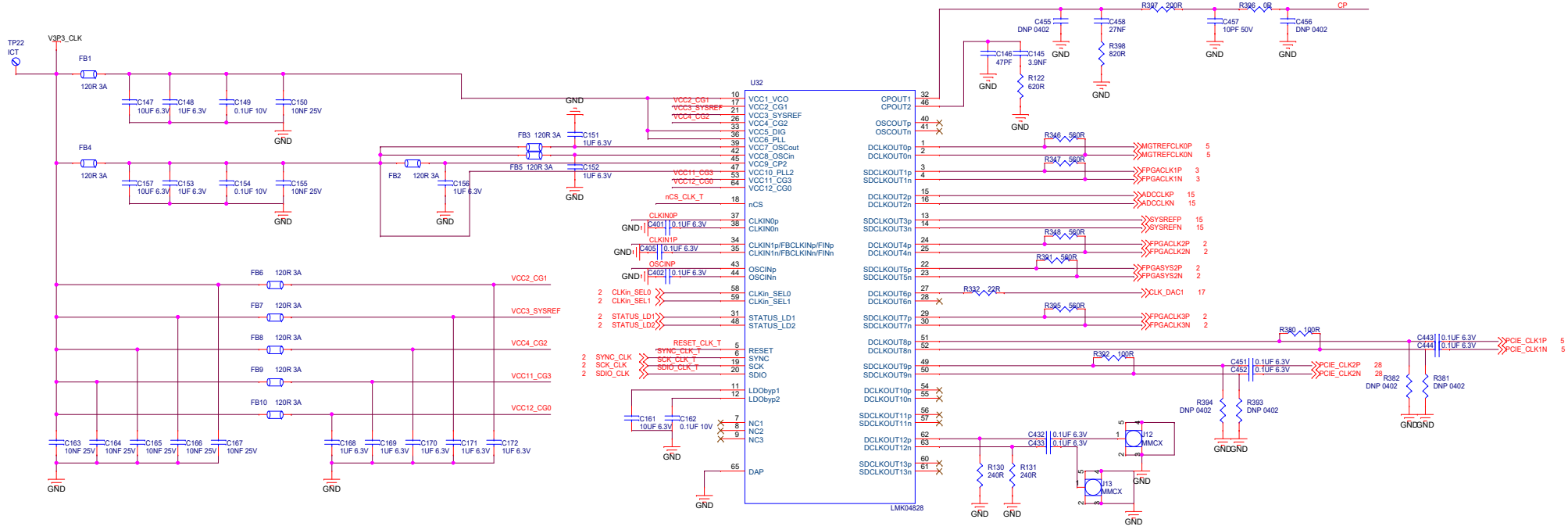
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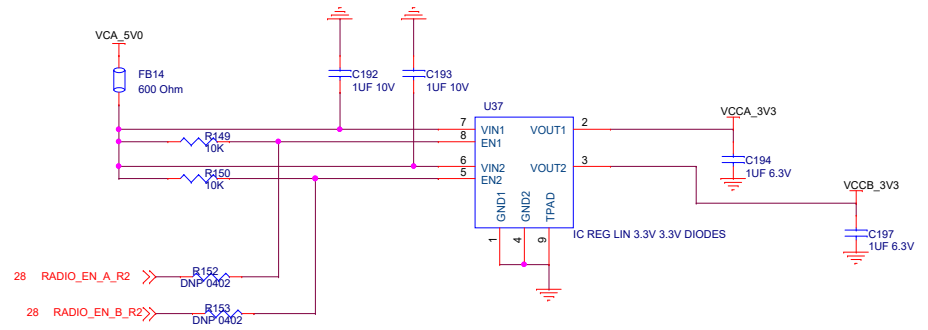
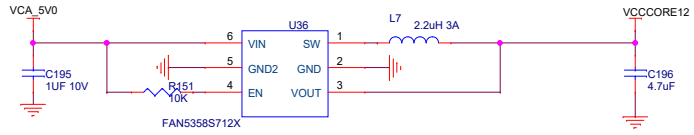
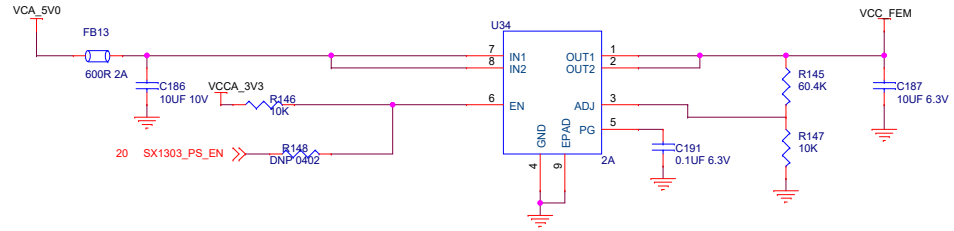
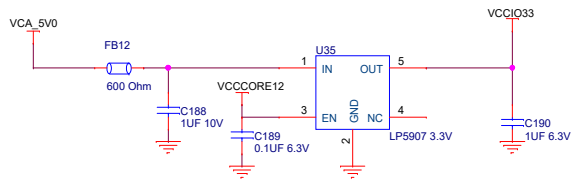




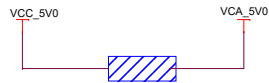
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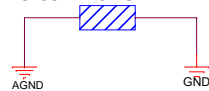
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**HOW TO CONNECT gnd TO AGND2?  
VIA STICING?  
CONNECT POWER PLANE?**

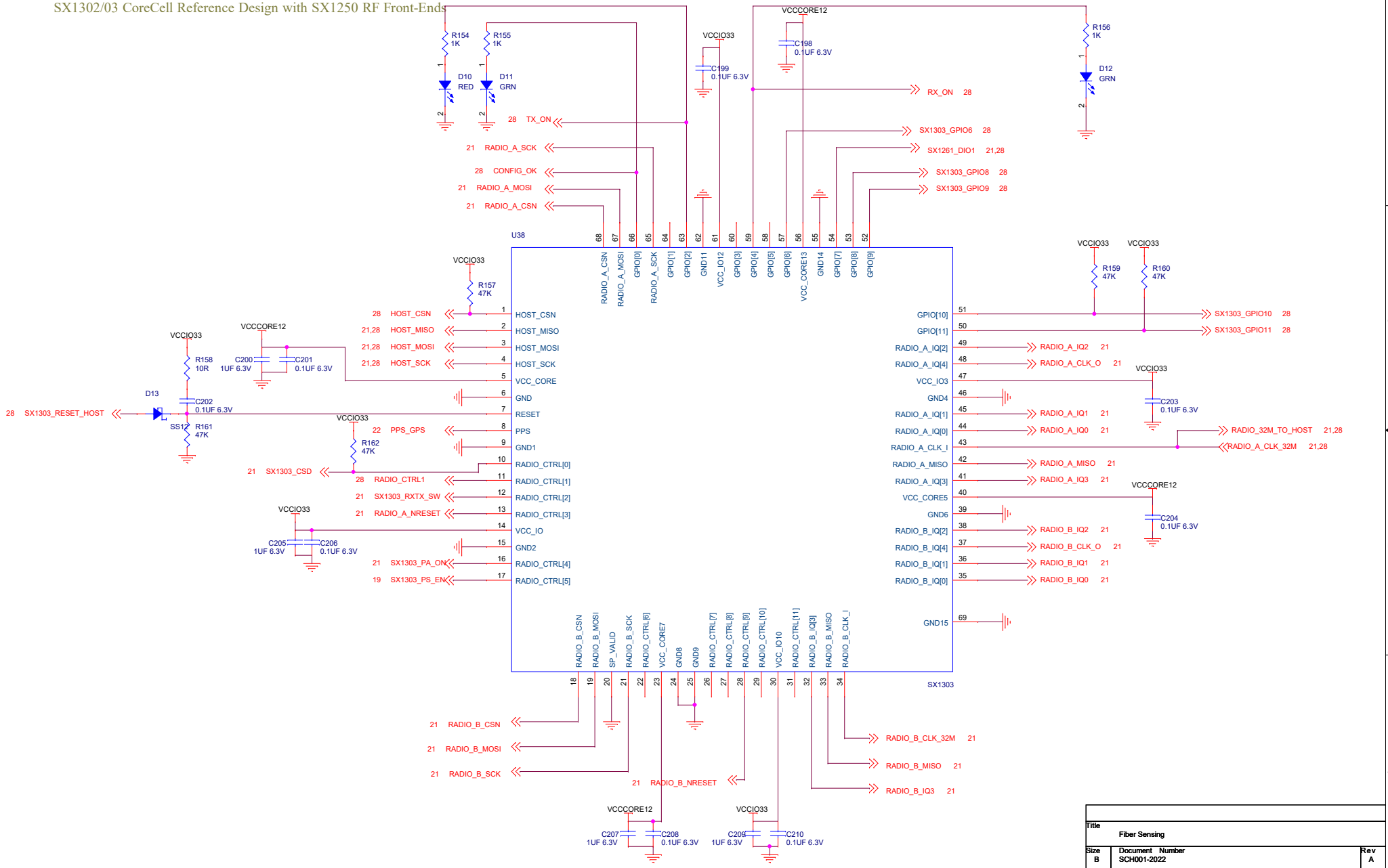


**FORCE TO CONNECT GND AND AGND2**



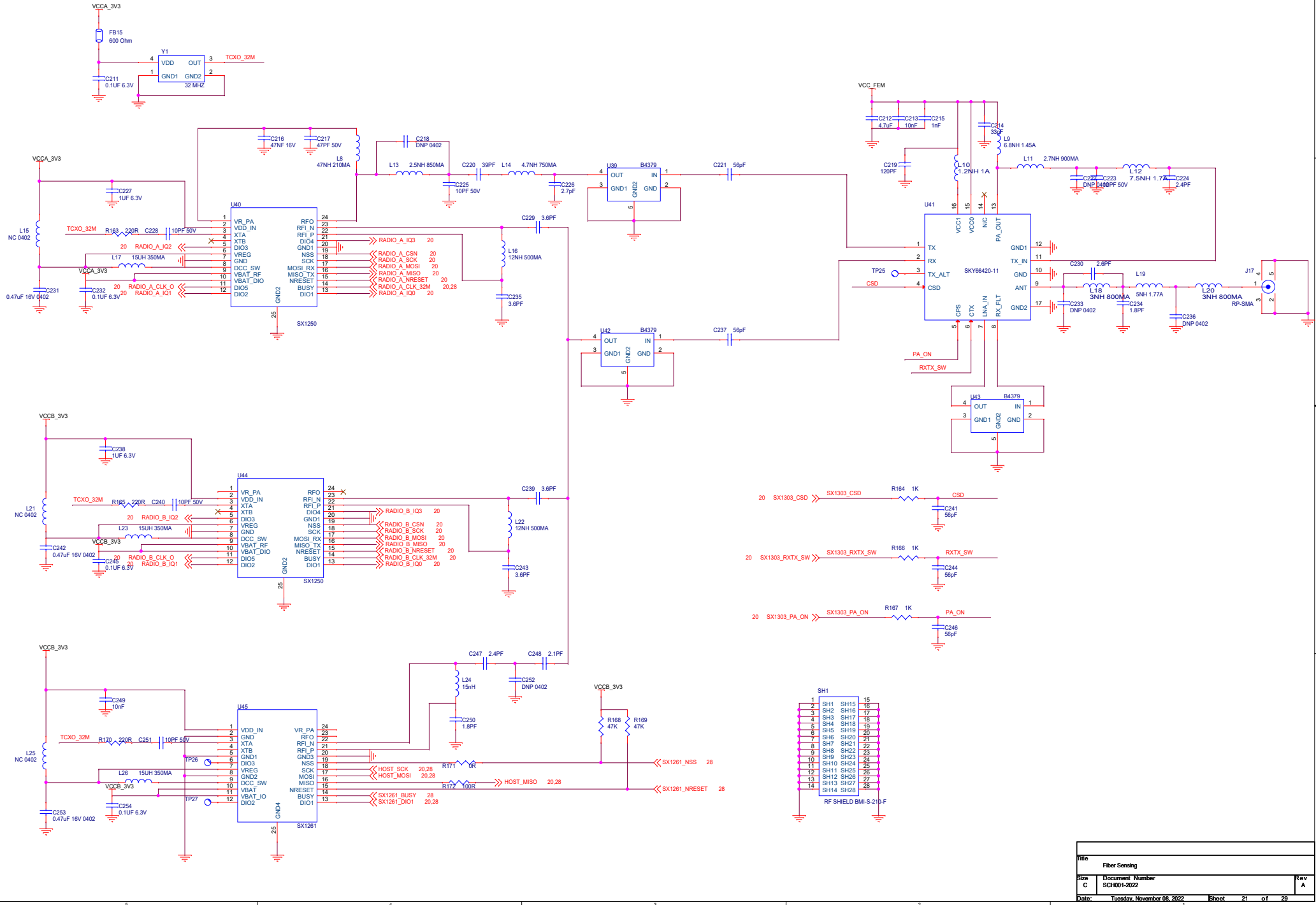
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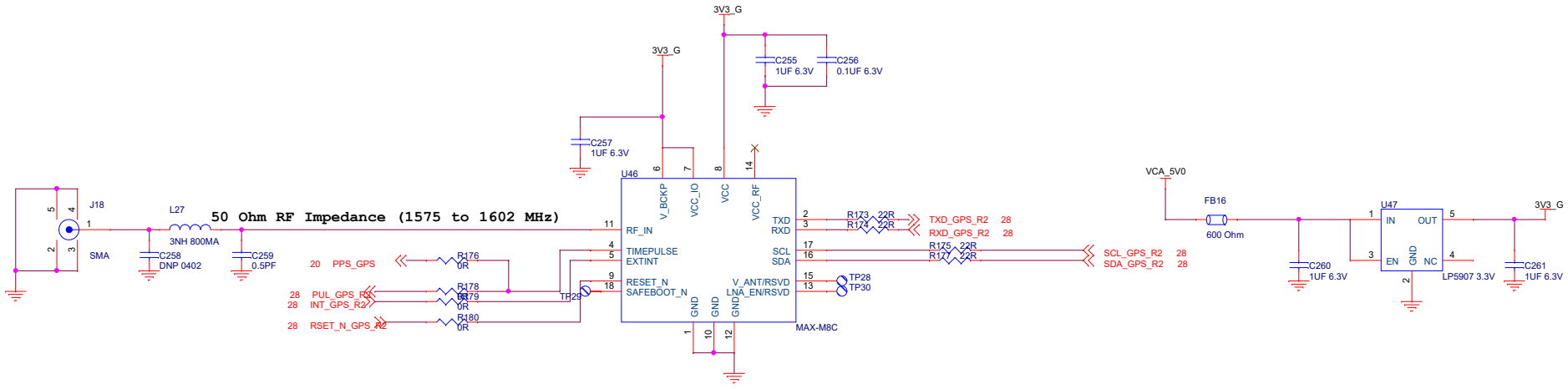
SX1302/03 CoreCell Reference Design with SX1250 RF Front-Ends



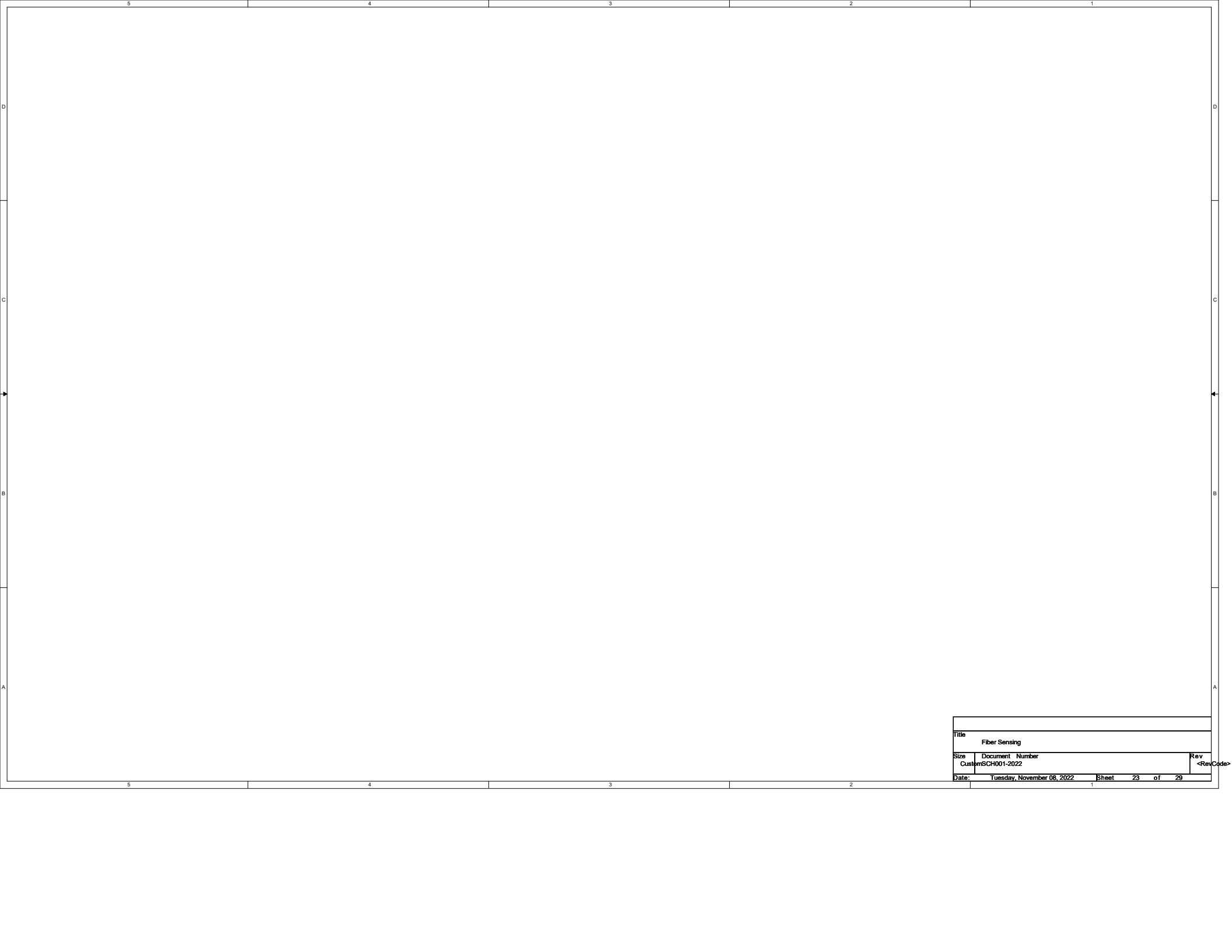
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# SX130x CoreCell Reference Design - RF Part with 2x SX1250 RF Front-Ends:

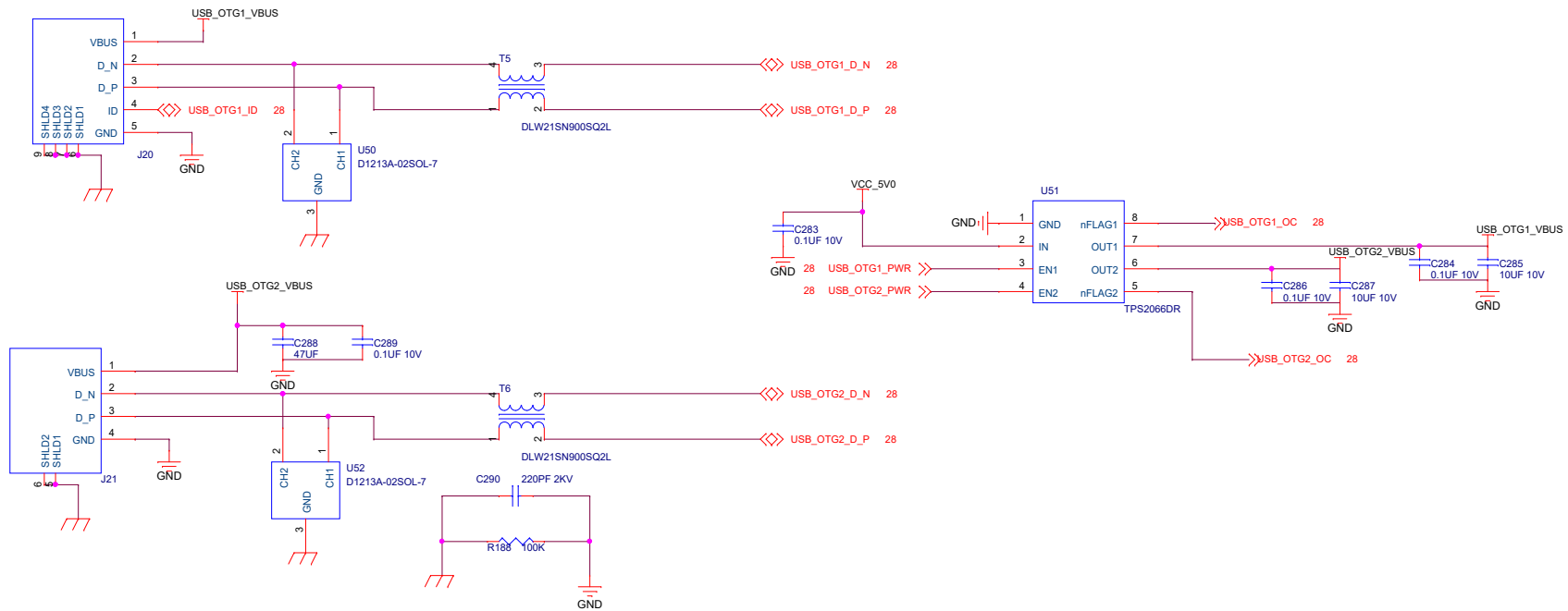




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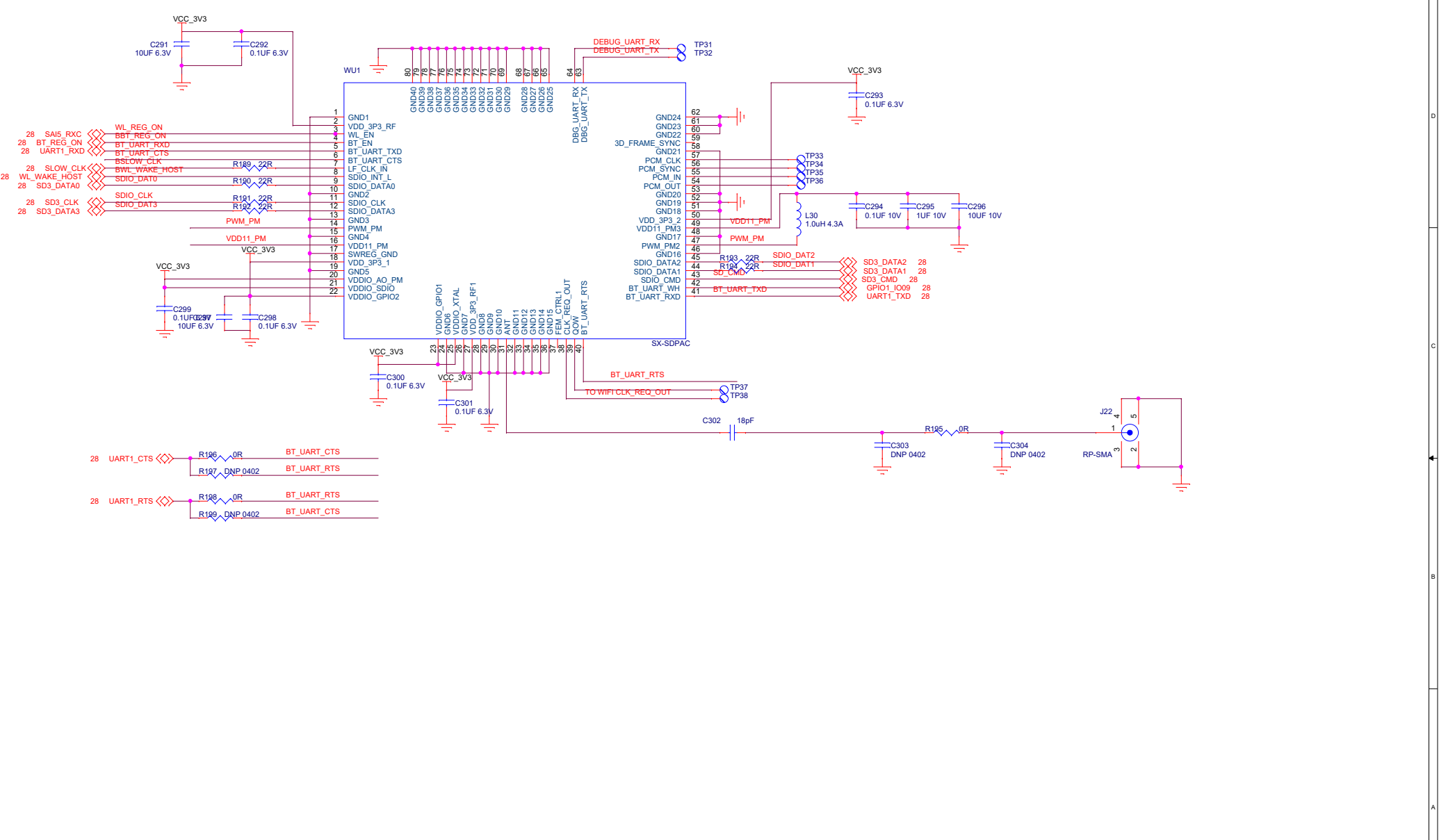


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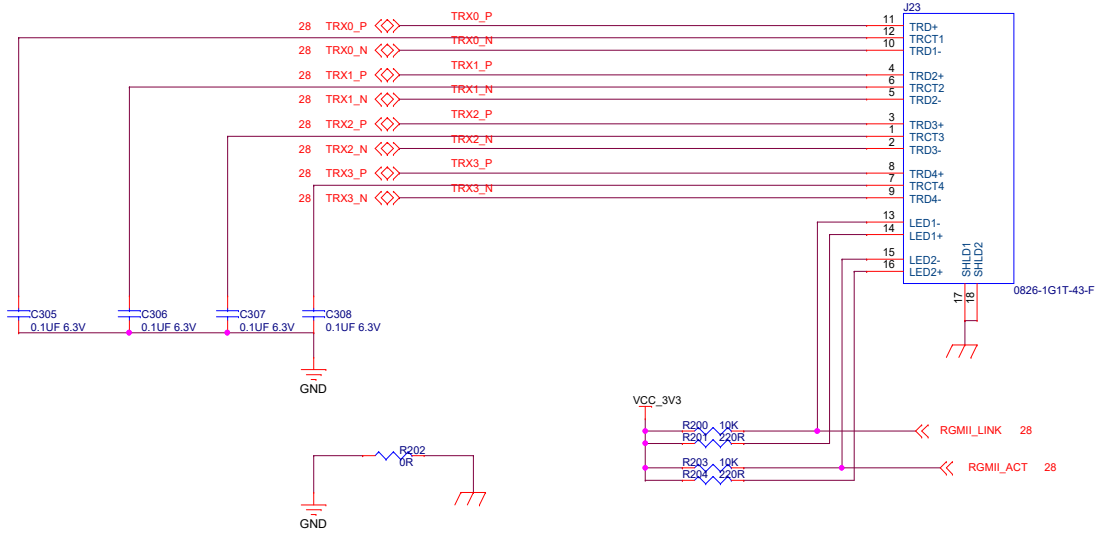
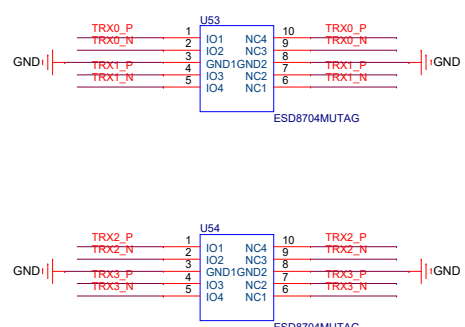


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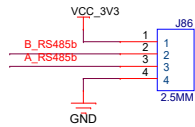
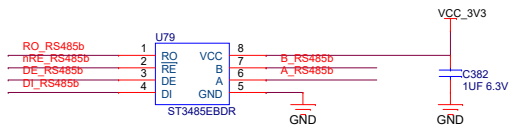
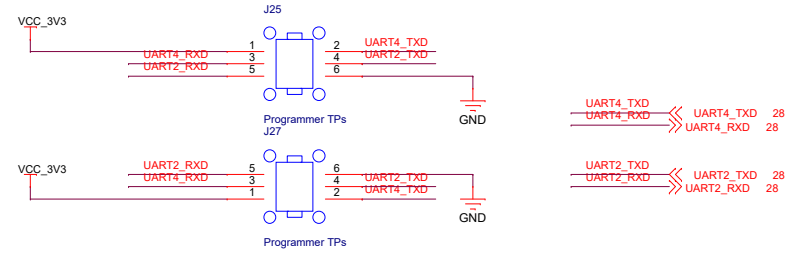
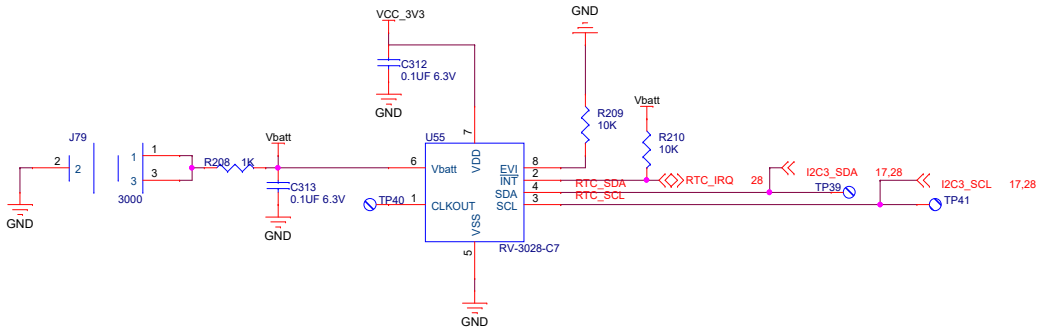
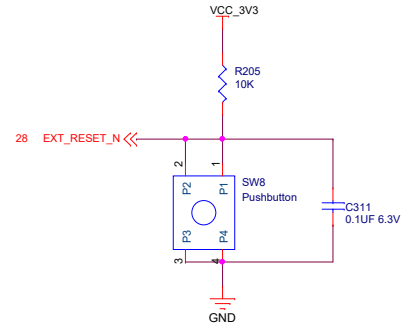
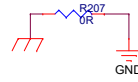
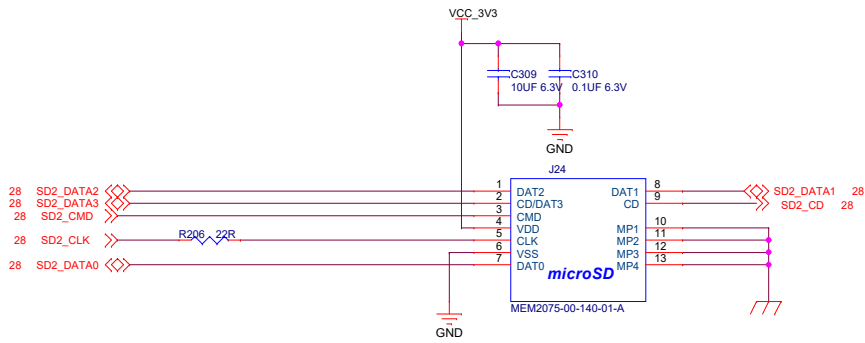




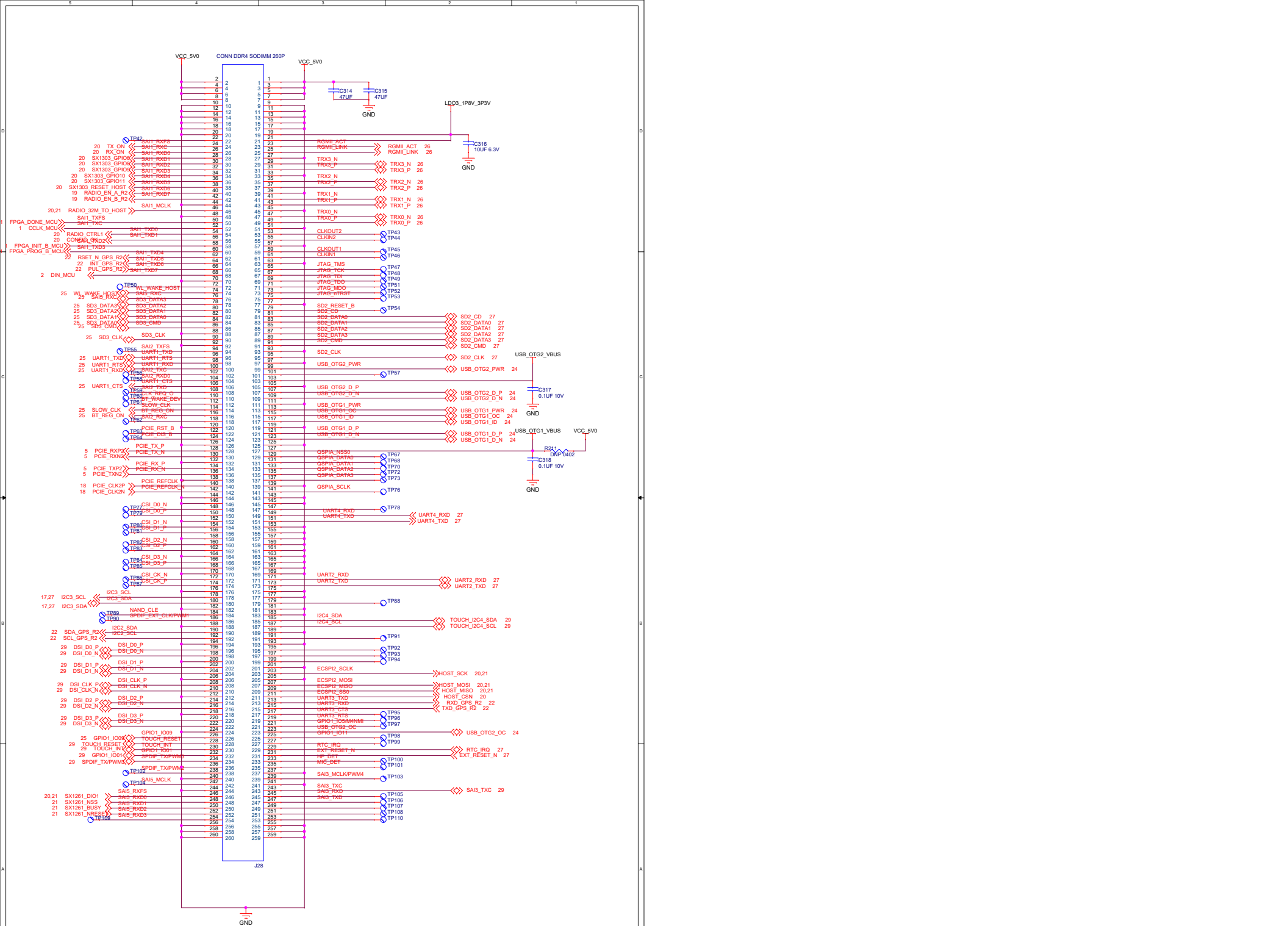
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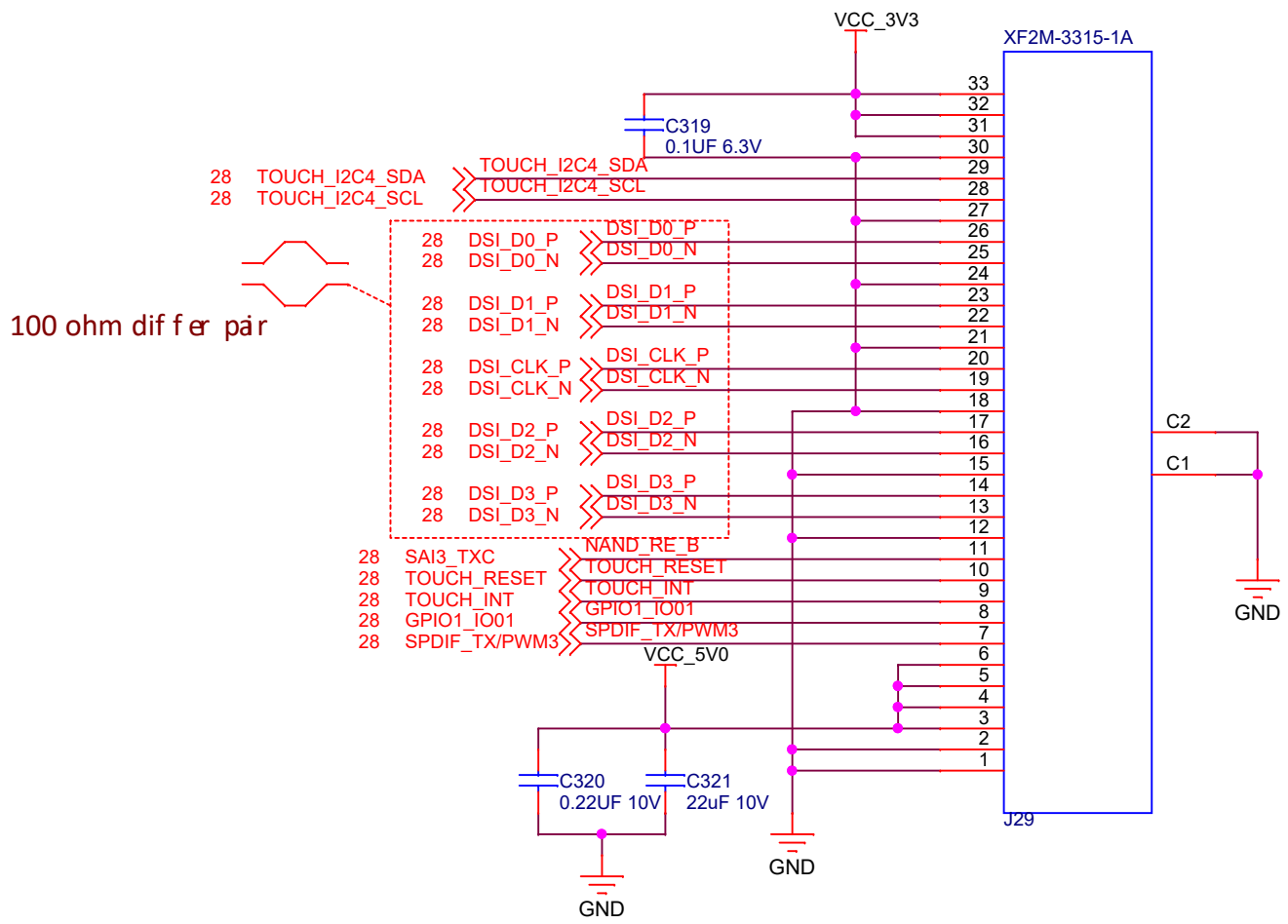


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