Input Impedance Extraction and Application for High Speed Amplifiers, Insight #9.

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As operating speeds increase, the effect of the internal impedance at the input nodes become more critical to achieving the desired frequency response. The most common issues revolve around the common mode and differential mode input capacitances for high speed Voltage Feedback Amplifiers (VFAs). While there are always physical input capacitive terms, their data sheet reporting is uneven at best. Assuming a device data sheet accurately reports both elements, then getting those into the public simulation models has also been hit or miss. Here, model testing steps will be shown for the VFA then external adjustments to match reported data sheet numbers will be shown. A couple of example applications that depend strongly on these terms will then be featured. These steps will also be extended to current feedback amplifiers (CFAs) and Fully Differential Amplifiers (FDAs).

Input capacitance model and extraction for VFAs.

All VFAs physically have two common mode input impedance elements on each input to the supplies along with a differential input impedance between the two inputs. Normally, the resistive elements are large enough to be ignored in VFAs. Here, the parasitic input capacitance terms will be the focus where the common mode terms are assumed to be matched on each input pin. Figure 1 shows this model drawing from one of the most common applications that is very sensitive to input capacitance – the transimpedance amplifier (Figure 1, Reference 1). This drawing does not show the C_{cm} on the V+ input as that is shunted to ground in this case. Also, the C_{cm} on the inverting input is shown to ground as that is equivalent to connecting it to the supplies for analysis purposes (normally, op amps do not have a ground pin separately from the two supplies).

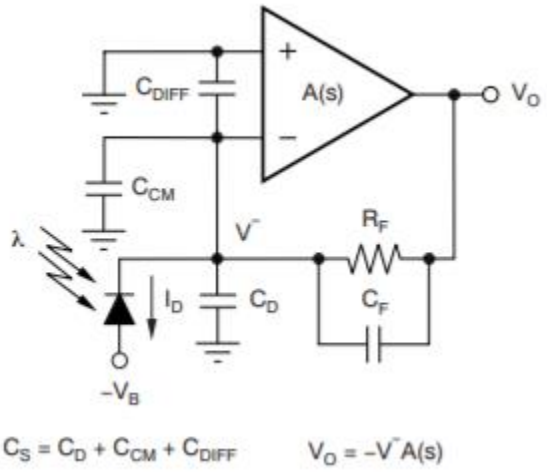

Figure 1. Typical Transimpedance design analysis schematic.

For loop gain analysis purposes, the transimpedance design needs to consider the C's of Figure 1. Both the C_{cm} and C_{diff} need to be accurately reported in the datasheet and captured by the public simulation models. Starting with the datasheet reported numbers from the OPA350 (Reference 2) in Figure 2, does the original 1999 TINA (model library in Reference 3) model show these values internally?

INPUT IMPEDANCE			
Differential		10^{13} || 2.5	Ω || pF
Common-mode		10^{13} || 6.5	Ω || pF

Figure 2. Reported input impedance numbers for the 38MHz RRIO CMOS OPA350 VFA.

One approach to checking the model is to go inside the netlist and search out what is on the input pins. Sometimes a combination of capacitors, protection diodes, and transistors makes that more effort than simply simulating what the model shows. There are always multiple valid approaches to any model testing effort. The first step used here is to isolate on the C_{cm} element using the approach of Figure 3. This is operating the op amp in a non-inverting gain of 1V/V configuration where a large series input resistor to the V+ input will create a single pole response to the V+ input depending the internal C_{cm}. That resistor value (in decade steps from the value shown) can be used to adjust for the 2π term to easily take the measured single pole F_{-3dB} back to a 1/(2πRC) solution for the C_{cm}. This closed loop simulation will be bootstrapping out the effect C_{diff} as long as the closed loop op amp bandwidth far exceeds the pole introduced at the V+ input. This same approach can be used for decompensated amplifiers operating at a higher than minimum stable gain and a closed loop bandwidth far exceeding the pole introduced at the V+ input by the source R_s and internal C_{cm}.

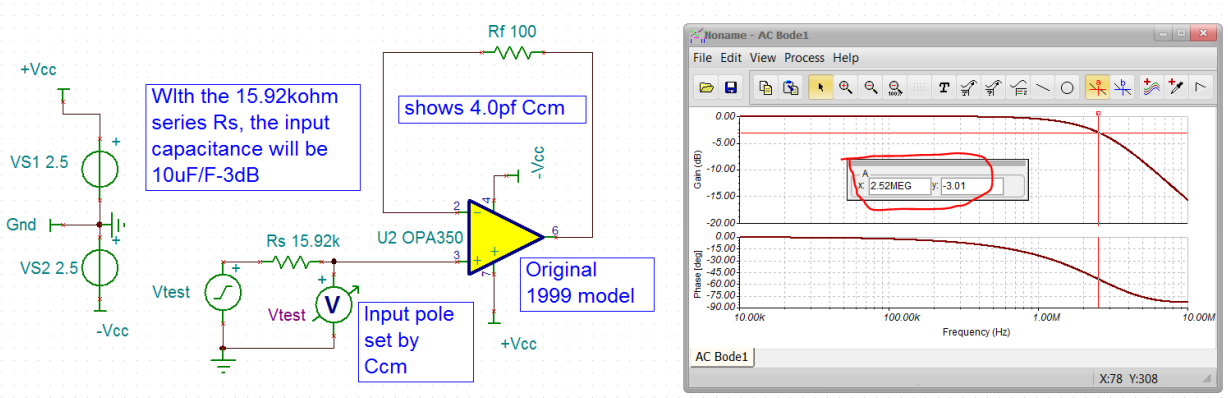

Figure 3. V+ input pin test for C_{cm}

This simple test solves this single pole response to 10µF/2.52MHz = 4pF internally for its V+ input common mode capacitance. Since the gain of 1 closed loop bandwidth at 38Mhz is far higher than this input pole, the differential input capacitance is removed from this test by the loop gain. It would appear that a 2.5pF external V+ capacitor to ground is needed to match the data sheet specified C_{cm} value of 6.5pF.

Numerous efforts to extract the differential input capacitance within the model led to the simple approach of Figure. 4. Here, the large feedback inductor closes the DC loop to find a centered DC operating point, then opens up at the first small signal frequency step while the large capacitor is open at DC then shorts out on the first small frequency step. This places the V+ input C_{cm} capacitance + the C_{diff} in parallel as a load on the source resistor. The C_{cm} on the V- node is shorted out by the large cap in this simulation. Solving for that total C as 10µF/802kHz = 12.5pF. Removing the 4pF C_{cm} term, the model apparently has a C_{diff} = 8.5pF. There is evidence in the phase of a higher zero coming into this simulation. With -41deg at F_{-3dB} (vs. -45deg ideal single pole), this is still approximately accurate. Getting the model

to match the 2.5pF C_{diff} from Figure 1 requires a -6.0pF element added across the inputs. Fortunately, this negative C (or L, or R) is a feature supported by TINA.

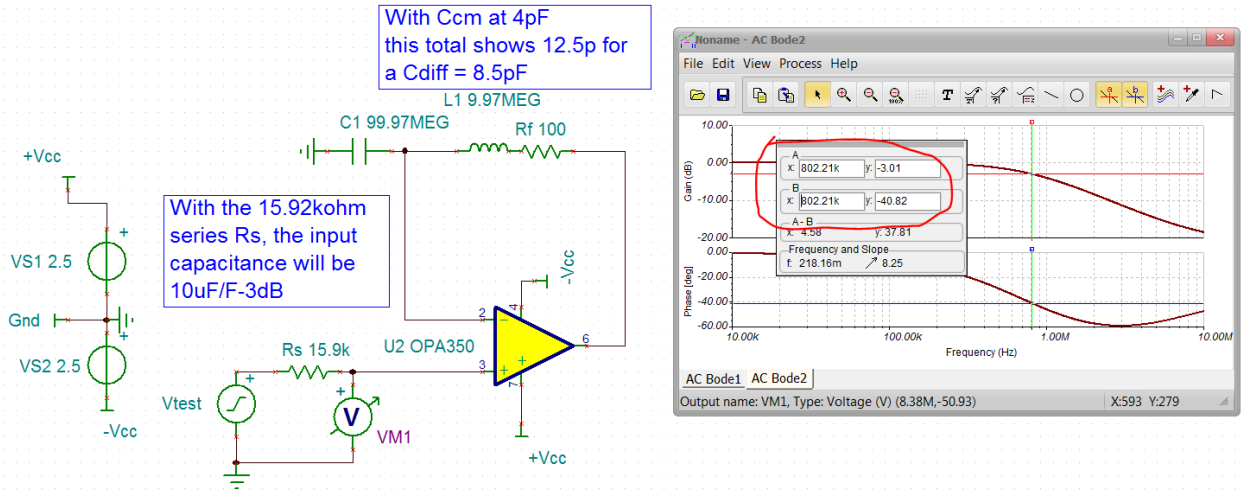

Figure 4. V+ input test for C_{cm} + C_{diff} by opening the loop in simulation.

Normally you would expect what V+ C_{cm} has been added to the model appears identically on the V- input pin. To check that, the inverting input test circuit of Figure 5 can be used. This is essentially the same test as Figure 4 but isolating on the V- input C_{cm} in parallel with a C_{diff} value. Grounding the V+ input removes the positive side C_{cm} from this simulation. Oddly, this shows lower total capacitance than the previous test with a perfect single pole response as shown by the -45deg phase at F_{-3dB}. This solves out to a total C of 10µF/1.11MHz = 9pF. With the 8.5pF C_{diff} in the model, this suggests the apparent internal C_{cm} on the V- input is only 0.5pF. Adding a 6pF externally to ground on the V- node will be necessary to match the data sheet 6.5pF number in Figure 1. It appears the inverting input Ccm terms was simply added to the Cdiff in this model. That will give equivalent performance vs. having the two terms in most, but not all, application circuits.

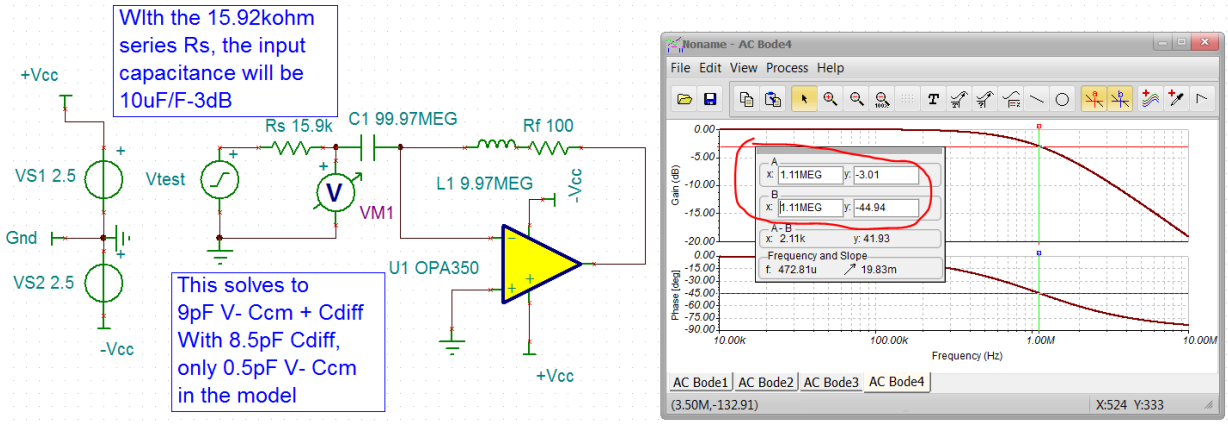

Figure 5. V- input pin test for C_{cm} +C_{diff}

Testing the modified OPA350 model in a Transimpedance Application.

The design flow for a transimpedance application (Reference 1) needs the sum of the C_{cm} on the inverting input and the C_{diff}, along with the detector capacitance to set the feedback capacitor to achieve a desired Q in the closed loop response (Equation 3, Reference 4). Taking a test case of a detector source capacitance of 10pF with a desired transimpedance gain of 100kΩ. The 1999 OPA350 TINA model has a true Gain Bandwidth Product of 38MHz with a 1kΩ load. In order to make the test design more sensitive, target a 2dB peaked gain with a Q=1.0. Equation 1 gives a good approximation to the required feedback C_f to hit any design shape.

$$C_f = \frac{1}{Q}\sqrt{\frac{C_s}{2\pi R_f GBP}} \qquad \text{Eq. 1.}$$

Putting a C_s = 10pF (diode) + 6.5pF (datasheet C_{cm}) + 2.5pF (datasheet C_{diff}) = 19pF and a GBP = 38MHz with Q = 1 gives a required Cf = 0.89pF. Figure 6 adjusts the 1999 model to match the data sheet (using external C elements) and runs this transimpedance simulation showing a very close 1.7dB peaking in Figure 6.

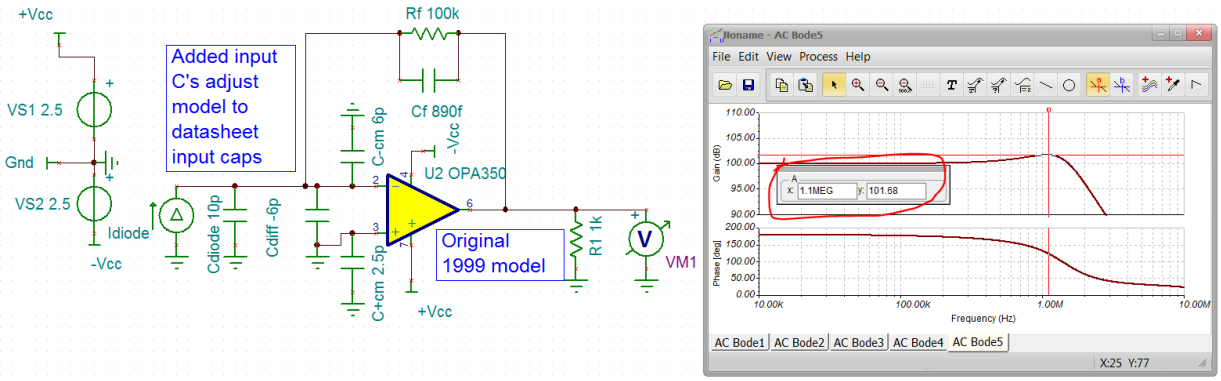

Figure 6. Transimpedance simulation using externally adjusted input C with OPA350 1999 TINA model.

The net adjustment for the C_{diff} + C_{-cm} is 0pF here, so there would be no apparent difference in this application to remove those external adjustments. For all applications, this full externally adjusted subcircuit for this model could be used in any circuit to more accurately estimate small signal response.

However, this OPA350 model (Reference 5) was completely updated in early 2019 to more accurately match the data sheet performance. Stepping through the input capacitance extraction steps shown here indicate this 2019 update exactly matches the data sheet input capacitance numbers of Figure 1 with two 6.5pF common mode input capacitors and a 2.5pF differential input capacitor. The GBP shifted up slightly in this new model to 41MHz. Re-running Eq. 1 for the required feedback capacitor to hit a 2dB peaked transimpedance response gives C_f = 0.86pF. Re-running this design with the new model and the external input caps removed with a slight shift in the C_f value, gives the 1.2dB peaking in Figure 7. This is only approximately matching the expected 2dB peaking probably due to the large change in the reactive open loop output impedance going from the 1999 model to this 2019 OPA350 model update.

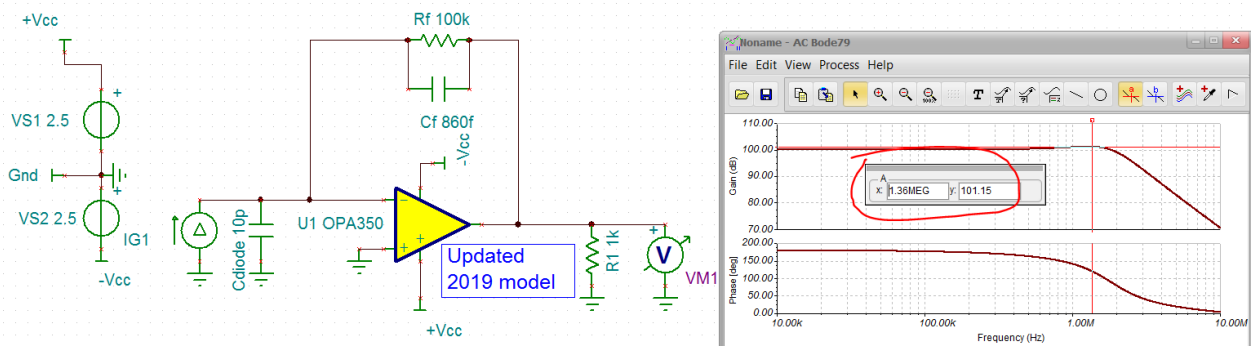

Figure 7. Transimpedance simulation using the corrected 2019 OPA350 TINA model.

This example showed only a modest impact from an earlier, less accurate, model to the latest update but illustrates a flow to test any VFA model for input capacitance. In summary,

1. There are a surprising number of high-speed VFA datasheets that report no, or only C_{cm}, input capacitances. That cannot be physically correct, so perhaps a model extraction can be used to define what is in the device. Sometimes these numbers are not in the specification tables, but in the applications text. For instance, the LMP7721 (Reference 6) shows a common mode input C_{cm} on page 18 as 11pF with nothing in the specification tables. The original 2008 model had no input capacitance in the model, whereas a recent 2019 update shows C_{cm}=15pF and a C_{diff}=5pF.
2. Where both CM and DM input impedance lines appear in a datasheet, it is by far the most common case that the Cdiff < Ccm. Where that is reversed, proceed with caution (Reference 7).
3. Since the data sheet numbers are usually from the IC designers, those might have the most accuracy. Lacking any other data, use those, and the tests shown here, to validate and adjust the model to match the datasheet.
4. While the TINA V11 includes a vast range of industry op amp models, be sure to check if the vendor web site offers an updated version that might have improved accuracy on this, and other, parameters.

The Impact of Input Capacitance on Common Applications

Aside from the transimpedance design example above, many other applications are vulnerable to input C induced issues as well. A very common one would be a simple non-inverting gain op amp using excessively high a resistor values. Continuing with the 2019 updated OPA350 model, Figure 8 shows a simple gain of +2V/V using 1kΩ R_f=R_g values. Even this relatively low selection for R's is introducing a pole in the feedback loop due the 9pF sum of C_{cm}+C_{diff}. For loop gain purposes those are added. Figure 8 shows a low impedance driving the V+ input. There will be no added response pole due to the V+ C_{cm} and the source shorts out that element for Loop Gain (LG) analysis. If the source impedance was not zero, the V+ C_{cm} would be part of the response as both a pole in the response to the V+ input and as part of the divider network to develop the "differential" feedback voltage for Loop Gain analysis.

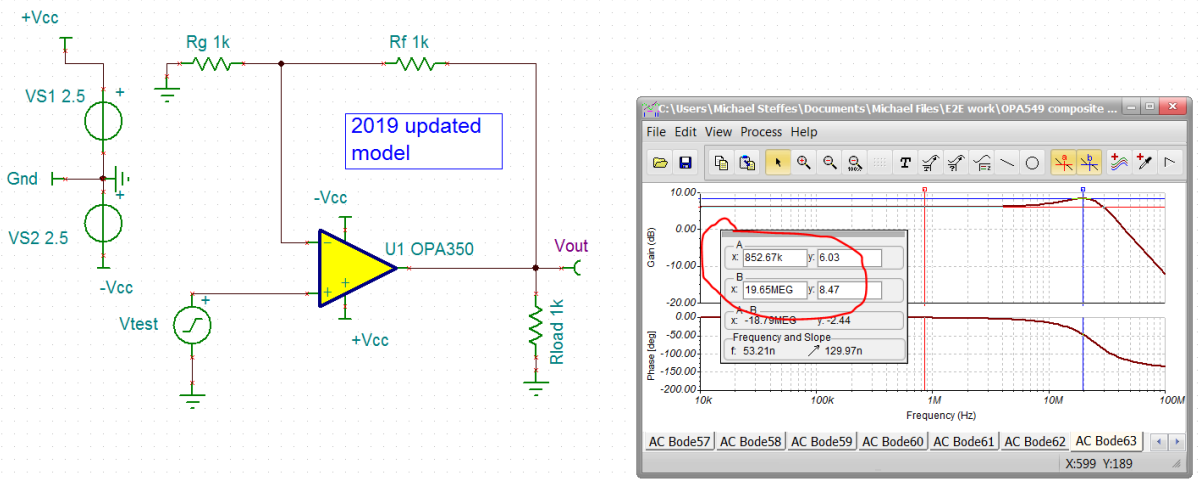

Figure 8. Non-inverting gain of +2V/V using R_f=R_g=1kΩ.

The relatively high 9pF on the summing junction in this corrected model is giving 2.45dB peaking at 19.7Mhz. The original 1999 model showed almost no peaking dropping it into the simulation of Figure 8. And, the datasheet (Reference 2) shows no closed loop response curves suitable to this design. Running a LG Phase Margin (PM) test (Reference 4) on this design gives the 51deg phase margin of Figure 9.

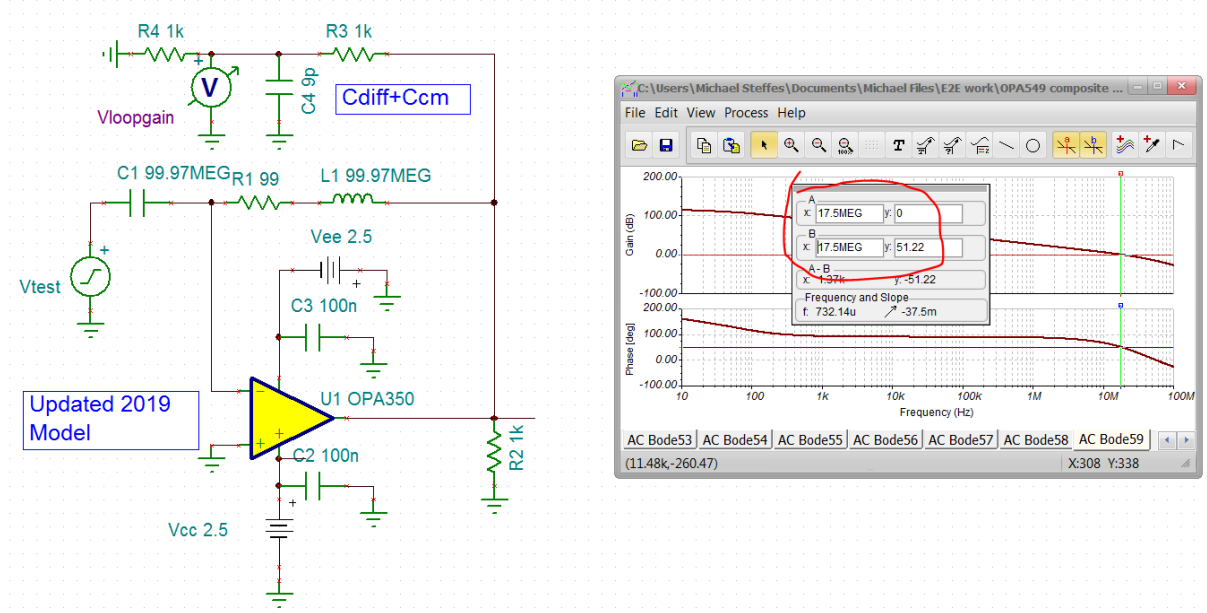

Figure 9. Loop Gain Phase Margin for a gain of +2V/V using 1kΩ resistors.

Removing the 9pF at the summing junction increases this PM = 77deg. A common way to improve phase margin in this situation is to add a compensating capacitor across the R_f resistor (Figure 16, Reference 8) as shown in Figure 10. This C_f = 9pF indeed flattens the response out and give a 28MHz closed loop F_{-3dB}. Of course, this depends on knowing what the model is delivering in its internal C_{cm} and C_{diff}. Placing this same 9pF into the LG simulation of Figure 9 gives 75deg PM.

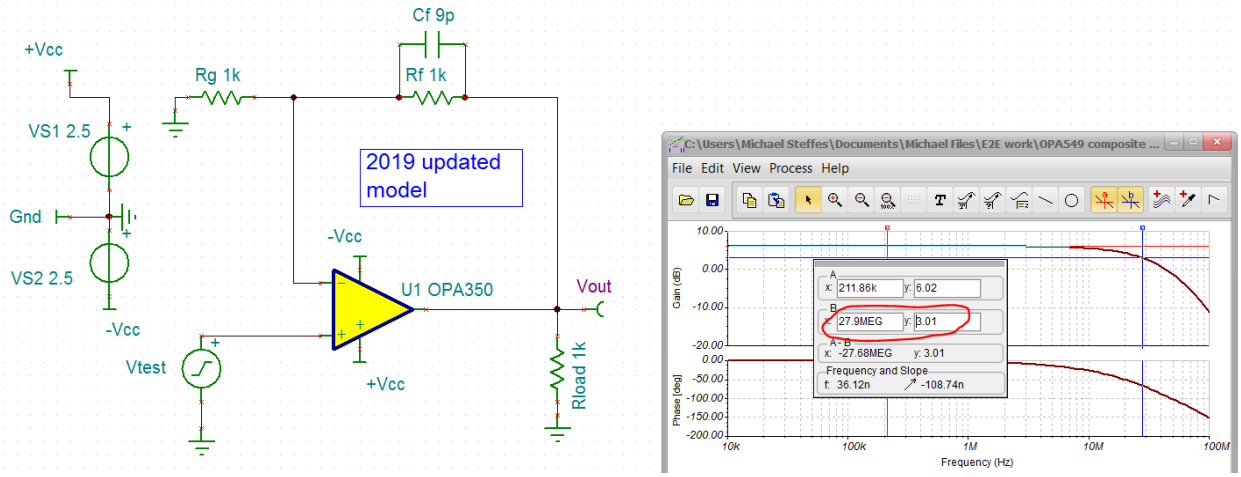

Figure 10. Compensating the response flat using a feedback capacitor

Another approximate approach to improving the response flatness when the device model is showing a relatively high input capacitance is to reduce the resistor values. Starting from a no summing junction capacitance phase margin case, Eq. 2 gives the maximum R_f to limit the reduction in phase margin from there by no more than 10deg. This equation is approximate in that it is not including the reactive open loop output impedance updated in the 2019 updated OPA350 model.

$$R_{f_{phase}} \leq \frac{K_0^2}{2\pi C_p \left(4 * GBP\right)}$$

Eq. 2

K_o is the gain (2, here)

GBP is the true model single pole Gain Bandwidth Product in Hz – 41MHz here.

C_p is the C_{cm} + C_{diff} or 9pF for the OPA350 updated model.

Putting those numbers into Eq. 2 shows a maximum Rf of 431ohms. Putting the closest E96 values into the LG simulation drops the phase margin from the no input C, 1kohm Rf=Rg, PM=77deg to 63.5deg. Putting those into a closed loop gain of +2V/V simulation of Figure 11 gives a very nice (nearly Butterworth) flat response with F_{-3dB} = 37MHz. This all starts from knowing the model values for the input parasitic capacitors. This example does point to one of the dangers of higher speed devices with higher input parasitic C's. You can quickly get into a lower phase margin condition with higher R values and to get out of trouble you may need to use resistor values lower than you might want from a power dissipation standpoint.

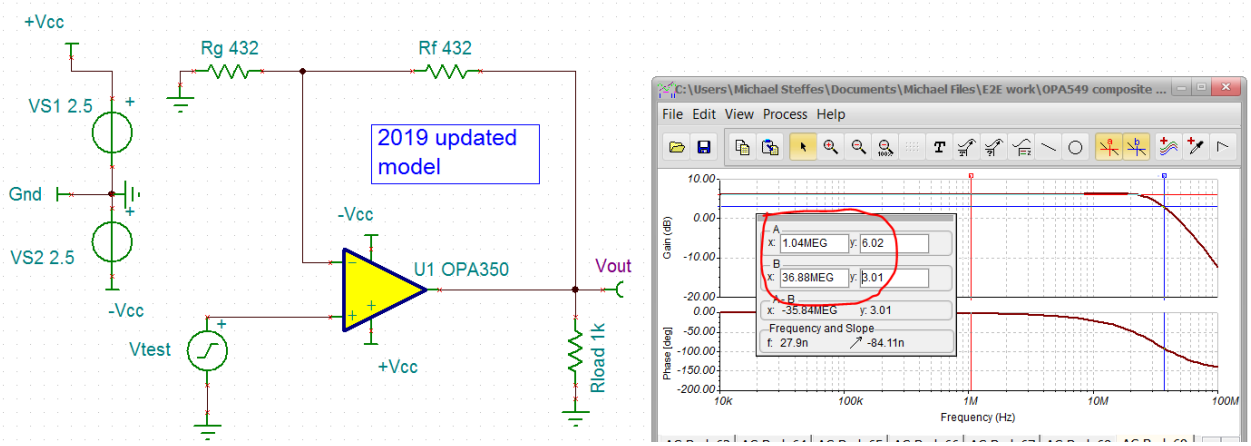

Figure 11. Gain of +2V/V with lower R_f=R_g values to improve phase margin.

Higher speed VFAs all physically have some input common mode and differential mode capacitance. Knowing what those are in the vendor models is a pre-requisite to fixing any response peaking issues. Use the steps shown here to test and/or modify the model to datasheet numbers – if available.

Input Impedance Considerations for High Speed Current Feedback Amplifiers (CFAs)

All CFAs use a unity gain buffer from the V+ input to the V- input. The most recent (2018) CFA introduction (ref. 9) shows a detailed input impedance specification in Figure 12.

INPUT						
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V
Z_{IN+}	Noninverting input impedance	Closed-loop measurement		50 || 1.2		kΩ || pF
Z_{IN-}	Inverting input impedance	Open-loop measurement	8	15	18	Ω

Figure 12. Input impedance specifications for the THS3491 CFA

High source impedances driving the V+ input will get bandlimited by that 1.2pF input capacitance. That model capacitance can be extracted using the same approach as Figure 3. Make sure to use a feedback resistor at least as high as the recommended value for stability in that simulation. There is not, however, any such thing as a differential input C for a CFA. The inverting input resistance becomes part of the CFA Loop Gain and can be tested in the model as shown in Reference 10.

Input Impedance Considerations for High Speed Fully Differential Amplifiers (FDAs)

Extracting the differential input impedance for a CFA based FDA is shown in Figure 1, Reference 11. A typical extraction for the differential input impedance for a VFA based FDA is shown in Figure 13. One unique aspect to this THS4551 simulation is to remove the internal 0.6pF feedback capacitors by adding external negative -0.6pF capacitors. These are shown in Section 8.2 of the product data sheet for the THS4551 (Reference 12). This dBohm plot of input impedance shows 100dB (100kΩ) at DC with a single pole response solving to a 1.2pF differential input capacitance in parallel. These exactly match the datasheet specifications (Reference 12).

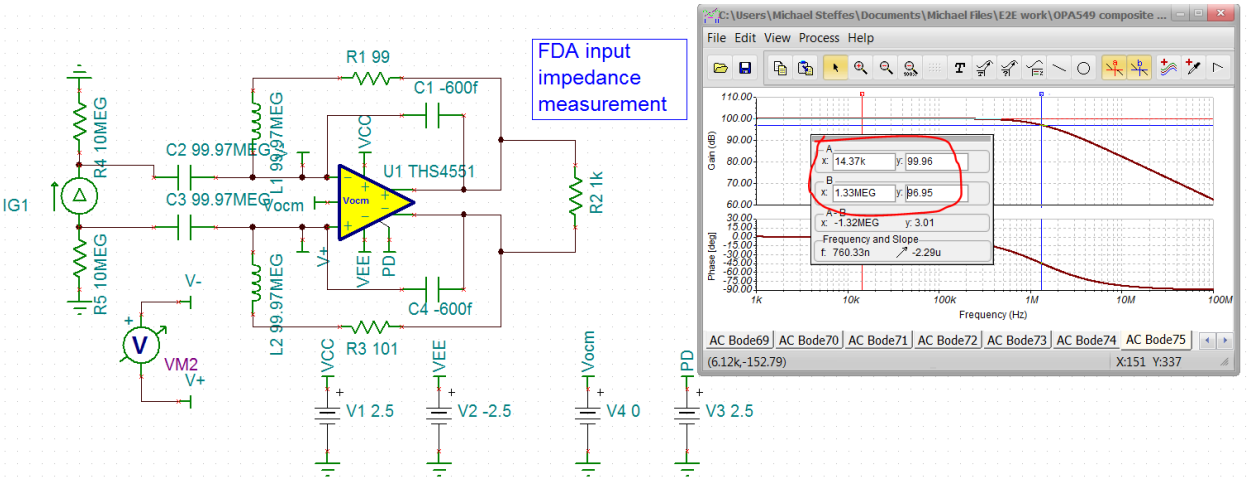

Figure 13. Open loop differential input impedance extraction for the THS4551 FDA.

It is this differential input impedance that must be pulled out and placed outside the loop breaking inductors for an FDA LG simulation (Reference 11). Checking an alternate, but older (2011), FDA model for the ADA4940 shows a simple 10MΩ differential input resistance. To adjust that model, add the specified (Reference 13) 33kΩ and 1pF values externally across the two input pins. Again, in that case, also checking for a model update over the 2011 version in the TINA V11 library would be prudent.

One interesting question is why is there no common mode input impedance specifications for VFA based FDA's? That element might have some impact in single ended input to differential output applications where the input common mode voltage moves with the input signal. Extensive testing with artificially placed common mode caps (externally), then collapsing those into an equivalent differential value, showed no differences across numerous closed loop and LG tests. So, apparently, the simple differential input RC model is adequate for these VFA based FDA's. Next up, using high speed decompensated VFA op amps across a wide range of application circuits – hitting your performance targets while tuning phase margin.

References for input impedance extraction

1. TI application note, Xavier Ramus, Nov. 2009,"Transimpedance Considerations for High Speed Amplifiers", http://www.ti.com/lit/an/sboa122/sboa122.pdf
2. TI, OPA350, "High-Speed, Single-Supply, RRIO MicroAmplifier Series", http://www.ti.com/lit/ds/symlink/opa4350.pdf
3. TINA simulator available from DesignSoft for <$350 for the Basic Plus edition. Includes a wide range of vendor op amps and is the standard platform for TI op amp models.
4. Planet Analog article "Stability Issues for High Speed Amplifiers: Introductory Background and Improved Analysis, Insight #5", Michael Steffes, Feb. 3, 2019, https://www.planetanalog.com/author.asp?section_id=3404&doc_id=565056&
5. Updated (2019) OPA350 TINA model, http://www.ti.com/product/OPA350/toolssoftware
6. TI, LMP7711, "Precision, 17MHz, Low Noise, CMOS Input Amplifier", http://www.ti.com/lit/ds/symlink/lmp7711.pdf

7. TI,LMV881, “23Mhz, Low Power, CMOS EMI Hardened Op Amp with 1.8V Logic Shutdown”, http://www.ti.com/lit/ds/symlink/lmv881.pdf
8. Planet Analog article “Stability Issues for High Speed High Speed Voltage Feedback Op Amps, Insight #6”, Michael Steffes, March 10, 2019, https://www.planetanalog.com/author.asp?section_id=3404&doc_id=565077
9. TI, THS3491, “900MHz, 500mA High Power Output Current Feedback Amplifier”, http://www.ti.com/lit/ds/symlink/ths3491.pdf
10. Planet Analog article “Stability Issues and Resolutions for High Speed Current Feedback Op Amps, Insight #7”, Michael Steffes, April 7, 2019, https://www.planetanalog.com/author.asp?section_id=3404&doc_id=565097&
11. Planet Analog article “Stability Issues and Resolutions for High Speed Fully Differential Amplifiers (FDAs), Insight #8”, Michael Steffes, May 1, 2019, https://www.planetanalog.com/author.asp?section_id=3404&doc_id=565122
12. TI, THS4551, “Low Noise, 150MHz, Fully Differential Amplifier”, http://www.ti.com/lit/ds/symlink/ths4551.pdf
13. ADI, ADA4940, “Ultralow Power, Low Distortion, Fully Differential ADC Drivers”, https://www.analog.com/media/en/technical-documentation/data-sheets/ada4940-1_4940-2.pdf