500Hz 4th order Butterworth active filter with the THP210

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I don’t do filters this low in F very often, it turned out I needed to update a few things in my MFB design tool – useful to do that occasionally,

1. I update with the highest <$0.1 in 1k 2% C0G MLCC cap values – yes, they have moved up a bit from the last time I looked, Murata standard E24 values up through 47nF look available now.
2. The FDA design flow is complicated in that you use 2X the physical value across the inputs for the equations. In this 500Hz target, that means using 2\*47nF =94nF for the equations where the final physical C will be 47nF and everything flows from there – this gives a little lower R values for this max C design – reducing noise.

1st need the pole locations – for an overall gain of 1 filter, yes the higher Q should be last. On filters with gain, it should be a descending Q sequence, these Filterpro RC solutions are primitive, can slightly improve on the overall integrated noise with better RC values. But I just really wanted the Fo and Q targets out of Filterpro – of course with Butterworth the poles are on a circle of equal Fo in the negative s-plane, only the Q’s change



I just needed the target Fo and Q for a design flow that will give best fit standard values with reduced noise gain peaking,

1st stage solution is here, this is the Q=0.54 stage, . Note the C1 row is 94nF for calculation purposes but 47nF for implementation. The green column is ideal op amp R values, the final R’s adjust for GBP and E96 best fit standard values, not much change here given the THP210 vastly exceeds the required GBP for a good fit.



And then the 2nd stage, this is the Q=1.31 stage



Doing the 1st stage in TINA, I do worry about phase margin with that big 27nF feedback C, quick way to look is spot noise at the outputs – there is little peak, probably ok, but connecting that feedback C outside those inside the loop R’s (0ohm for now) gives a tune to improve that. The 27nF gives you a 0dB noise gain, that is hitting the Aol curve around the 8MHz GBP showing <50deg phase margin is seems from that little noise peak out there,



And then here are the two stages together,



Putting the higher Q stage 1st will reduce integrated noise but risk step response overshoot clipping, here is the integrated noise for this ascending Q design, little under 4uVrms or about .24mVpp

