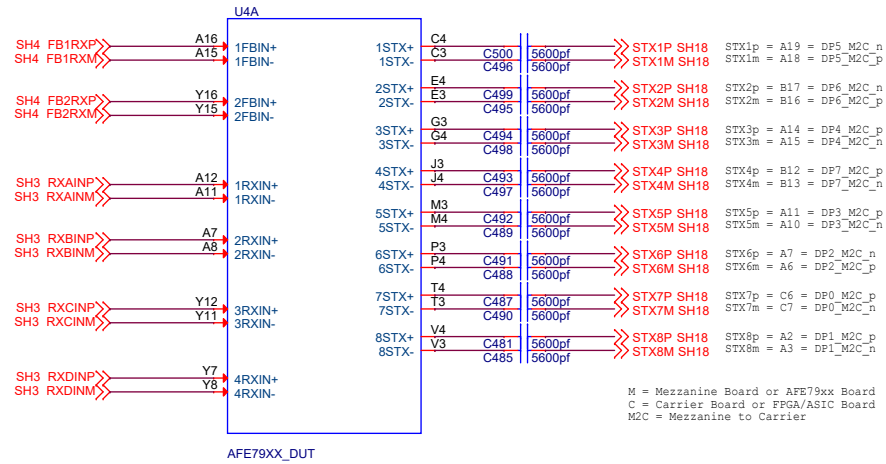



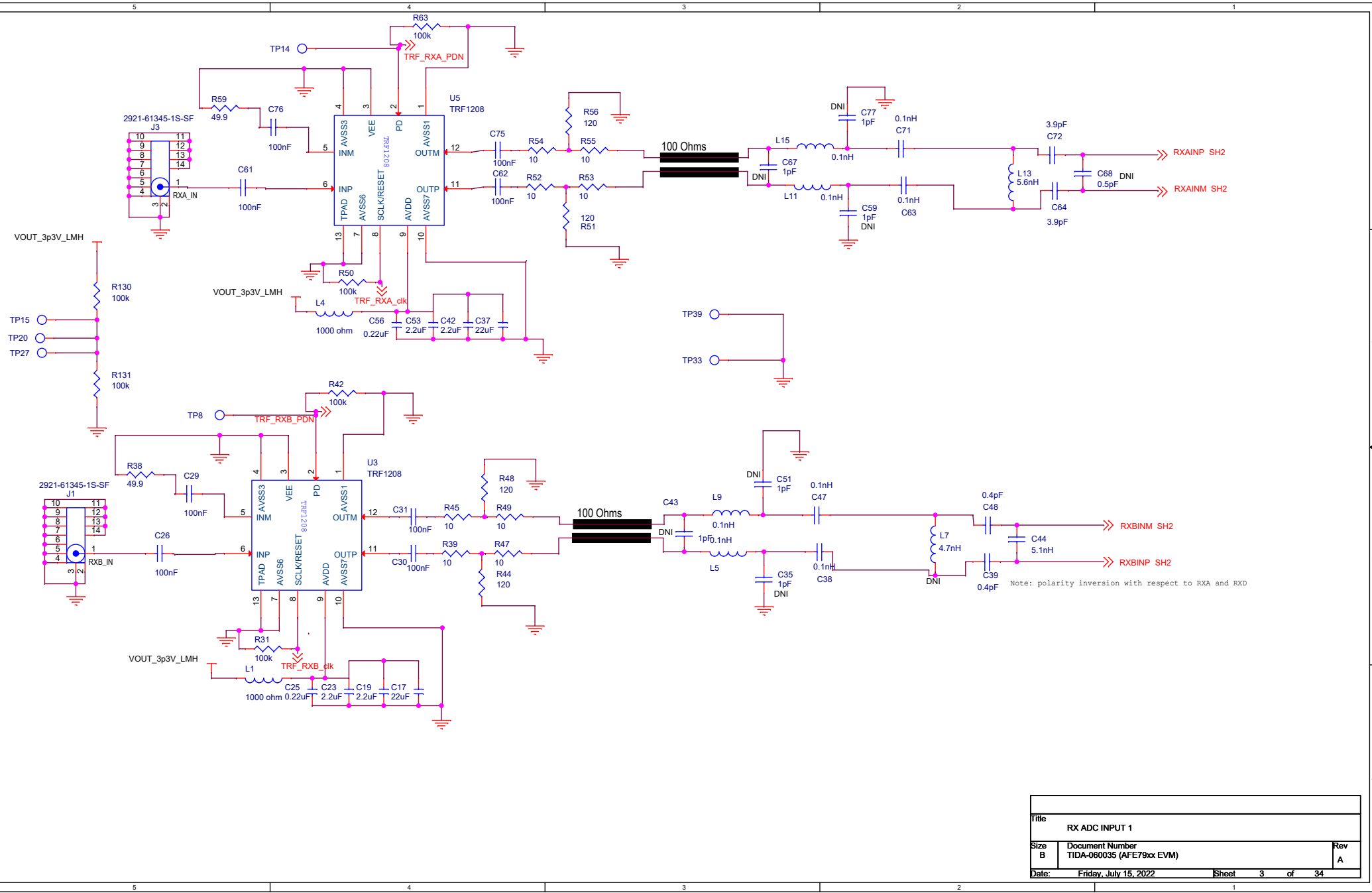
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Block Diagram		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 1 of 34



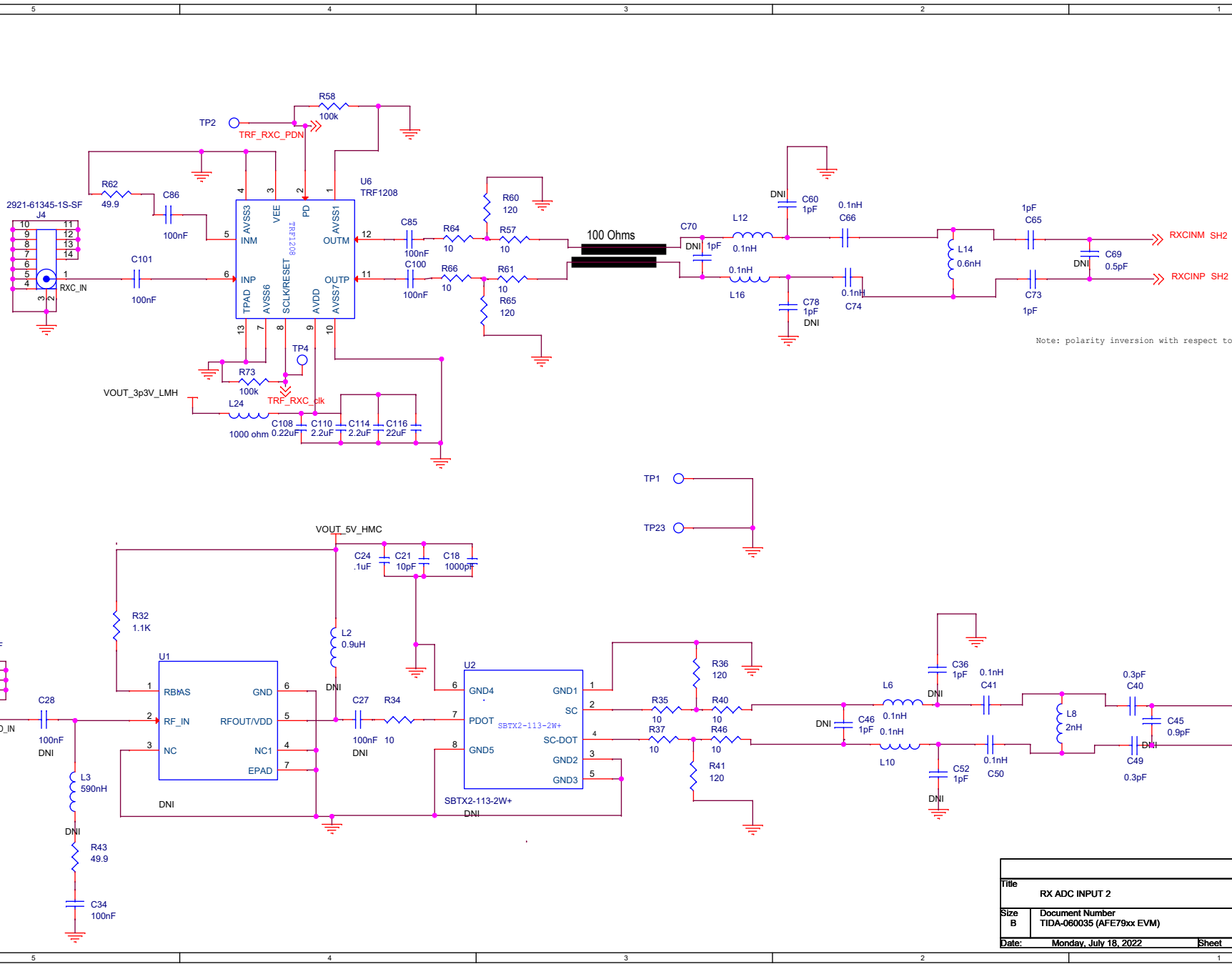
 **TEXAS INSTRUMENTS**

Title: DUT ADC

Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
Date: Wednesday, July 13, 2022	Sheet 2 of 34	

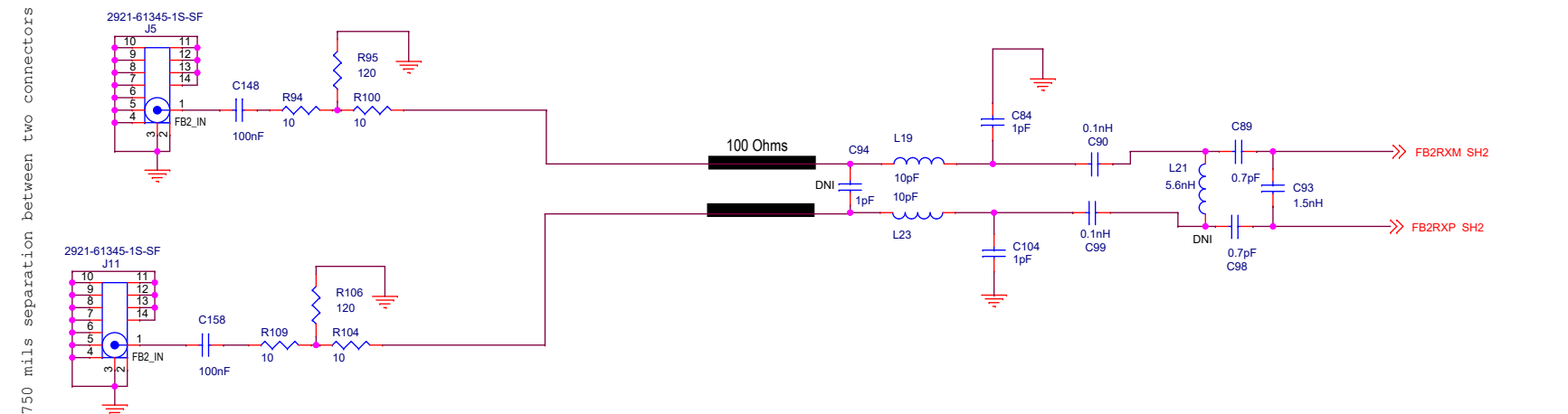
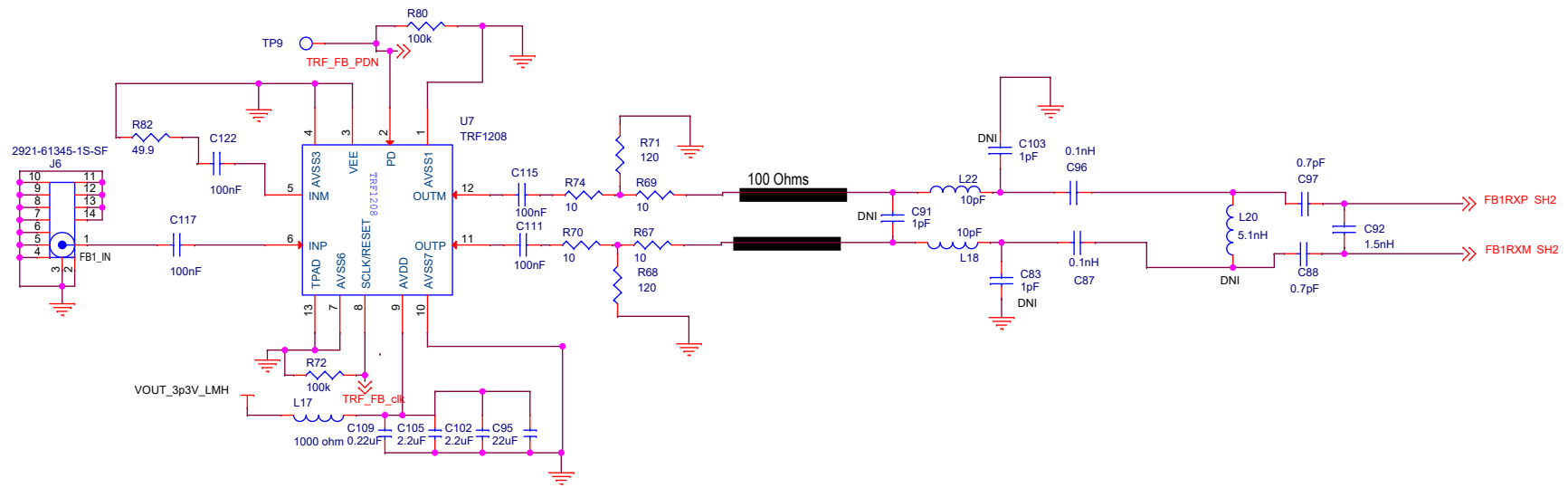


Title		
RX ADC INPUT 1		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Friday, July 15, 2022	Sheet 3 of 34



Note: polarity inversion with respect to RXA and RXD

Title		RX ADC INPUT 2	
Size	Document Number	TIDA-060035 (AFE79xx EVM)	
B		A	Rev
Date:	Monday, July 18, 2022	Sheet	4 of 34

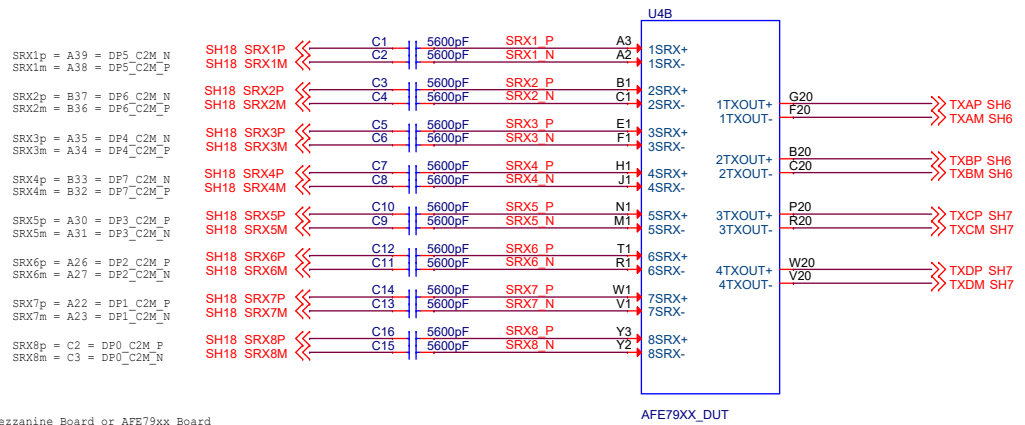


TEXAS INSTRUMENTS

Title: FB ADC INPUT

Size B Document Number TIDA-060035 (AFE79xx EVM) Rev A

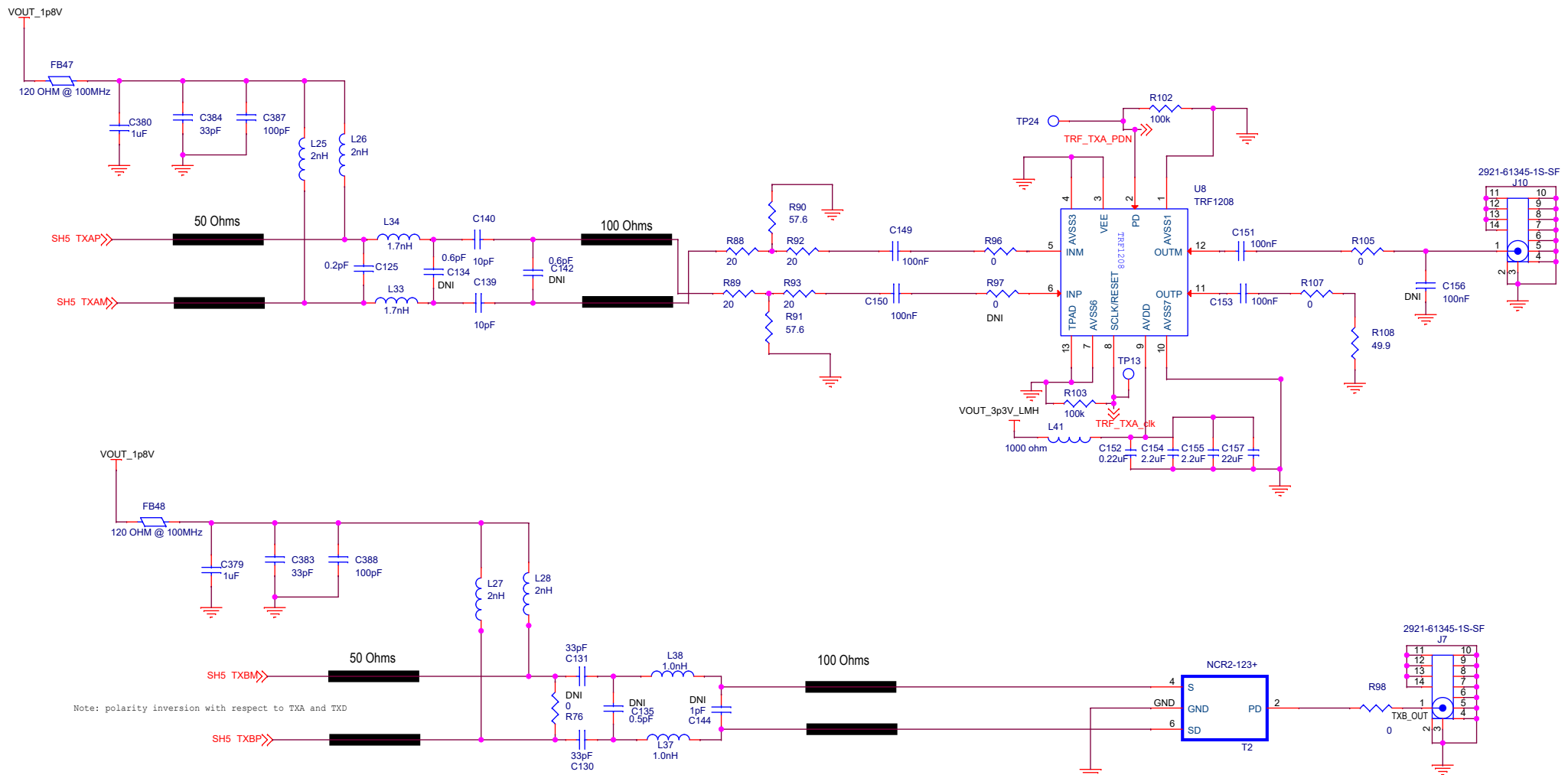
Date: Friday, July 15, 2022 Sheet 5 of 34



M = Mezzanine Board or AFE79xx Board
 C = Carrier Board or FPGA/ASIC Board
 M2C = Mezzanine to Carrier

TEXAS INSTRUMENTS

Title		DUT DAC
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date: Wednesday, July 13, 2022		Sheet 6 of 34



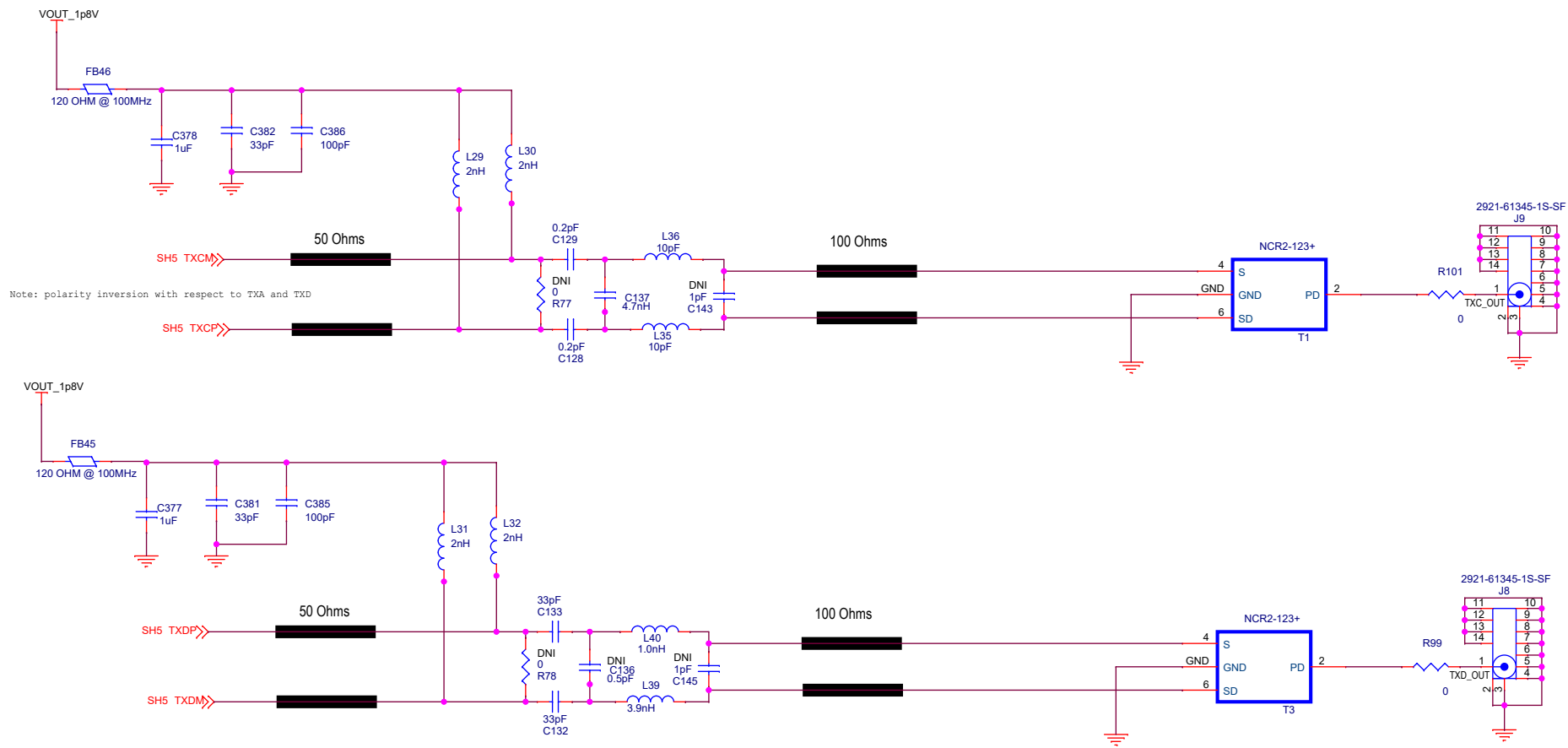
Note: polarity inversion with respect to TXA and TXD

TEXAS INSTRUMENTS

Title: DAC OUTPUT 1

Size B | Document Number: TIDA-060035 (AFE79xx EVM) | Rev A

Date: Friday, July 15, 2022 | Sheet 7 of 34

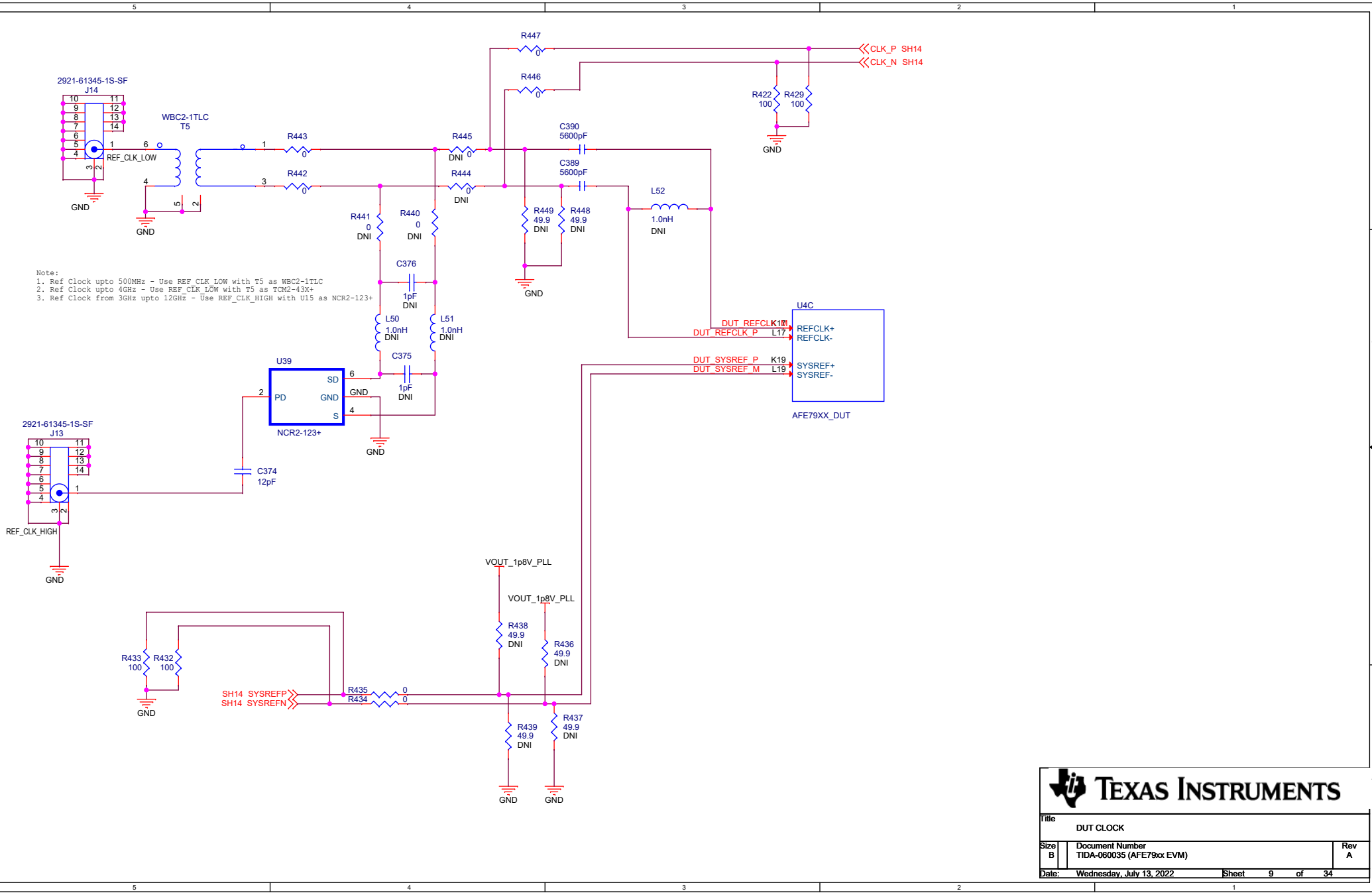


TEXAS INSTRUMENTS

Title: DAC OUTPUT 2

Size B Document Number TIDA-060035 (AFE79xx EVM) Rev A

Date: Friday, July 15, 2022 Sheet 8 of 34

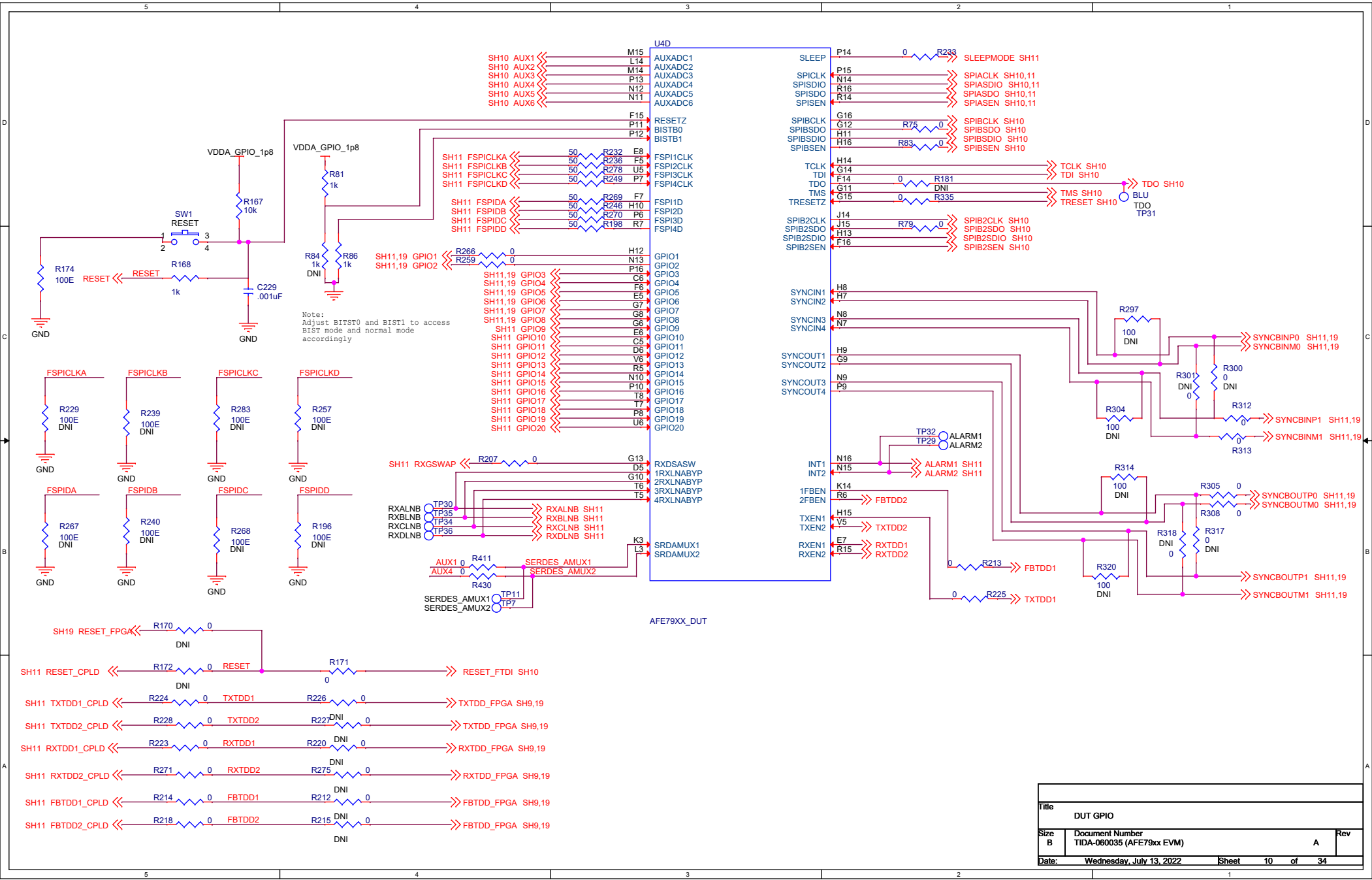


Note:
 1. Ref Clock upto 500MHz - Use REF_CLK_LOW with T5 as WBC2-1TLC
 2. Ref Clock upto 4GHz - Use REF_CLK_LOW with T5 as FCM2-43X+
 3. Ref Clock from 3GHz upto 12GHz - Use REF_CLK_HIGH with U15 as NCR2-123+

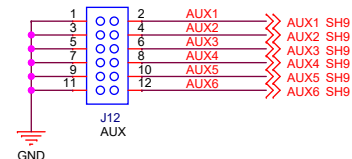
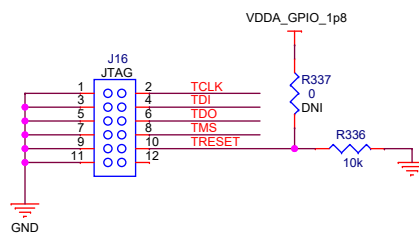
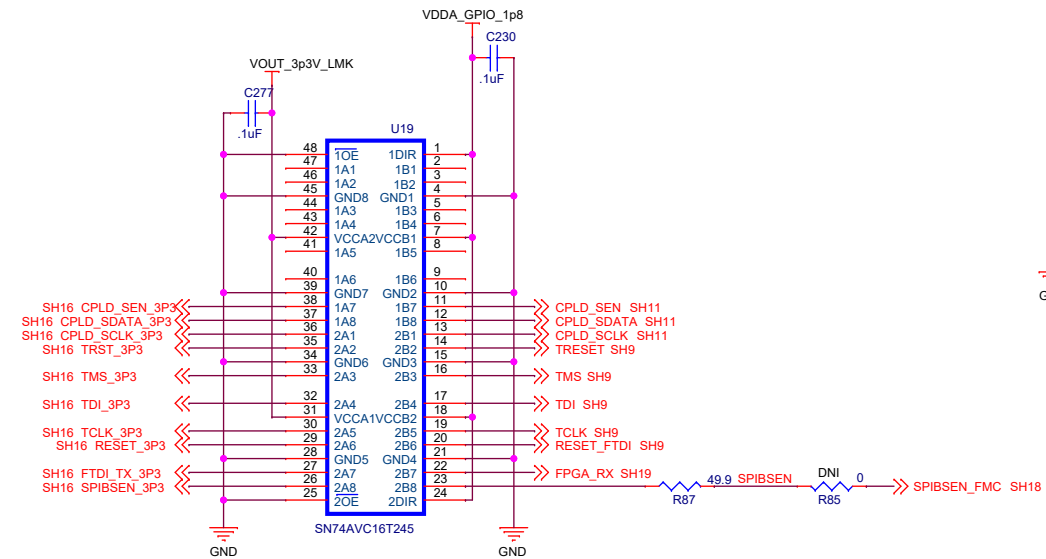
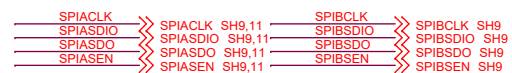
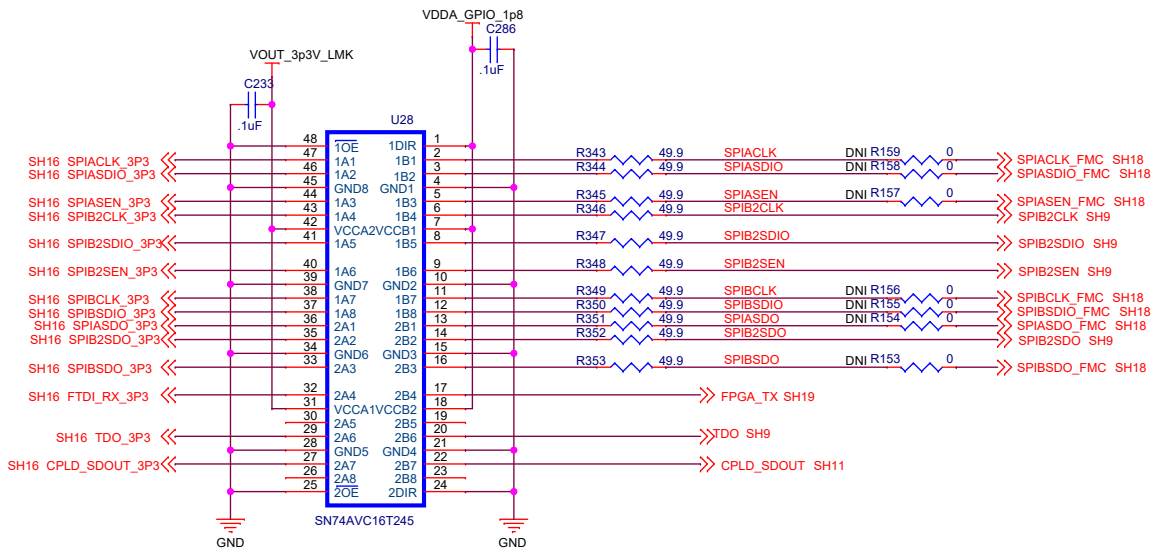
TEXAS INSTRUMENTS

Title: DUT CLOCK

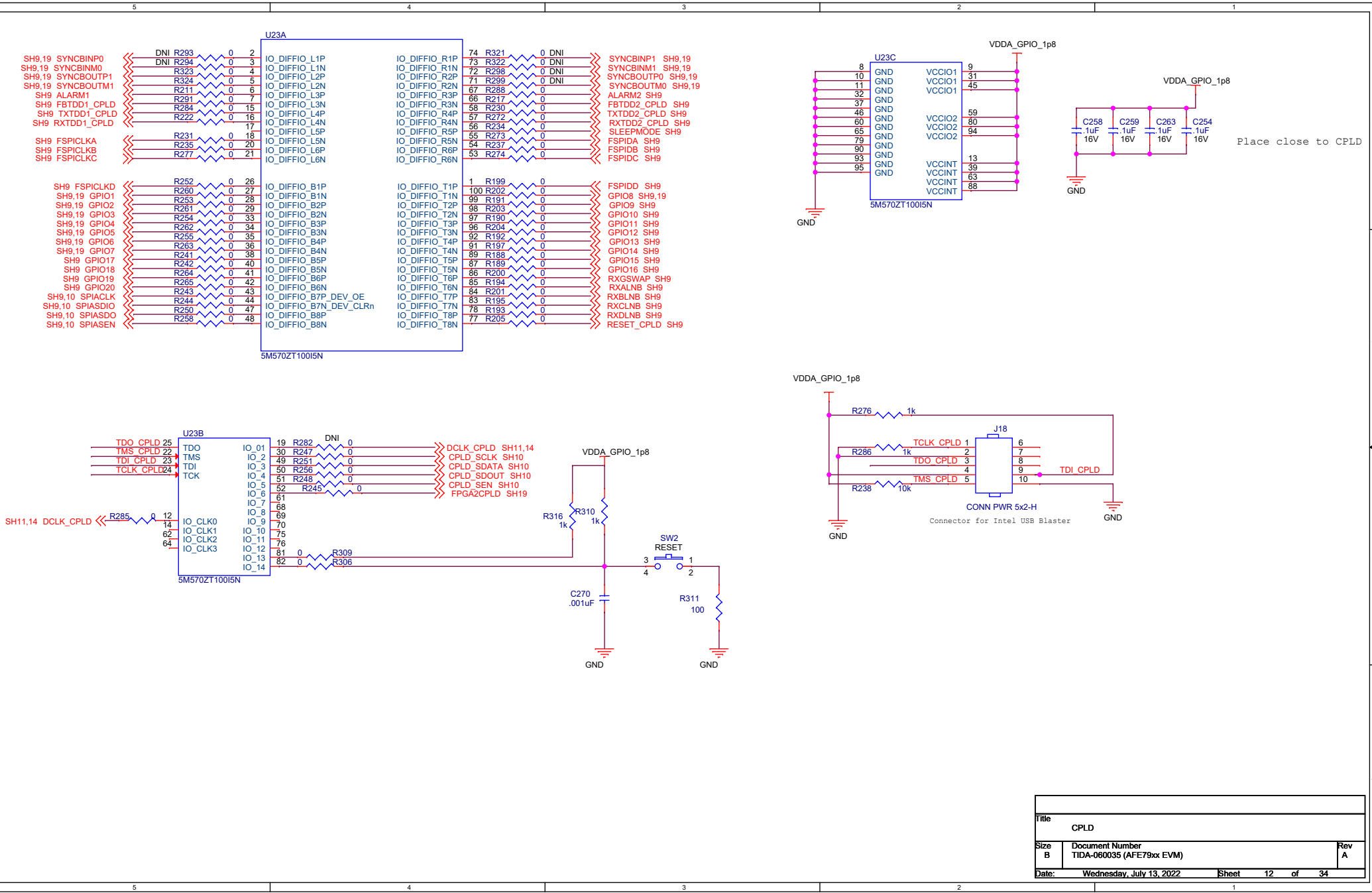
Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
Date: Wednesday, July 13, 2022	Sheet 9 of 34	



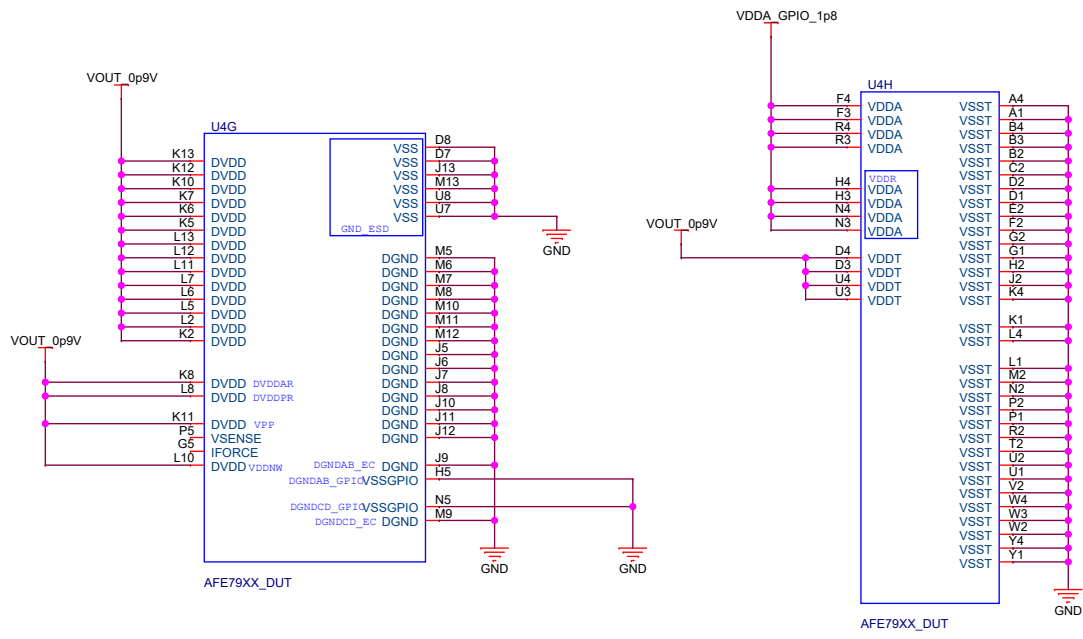
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Size	Document Number		Rev
B	TIDA-060035 (AFE79xx EVM)	A	
Date:	Wednesday, July 13, 2022	Sheet	10 of 34



Title		
LEVEL SHIFTERS		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet
	11	of 34



Title			CPLD
Size	Document Number	Rev	
B	TIDA-060035 (AFE79xx EVM)	A	
Date:	Wednesday, July 13, 2022	Sheet	12 of 34

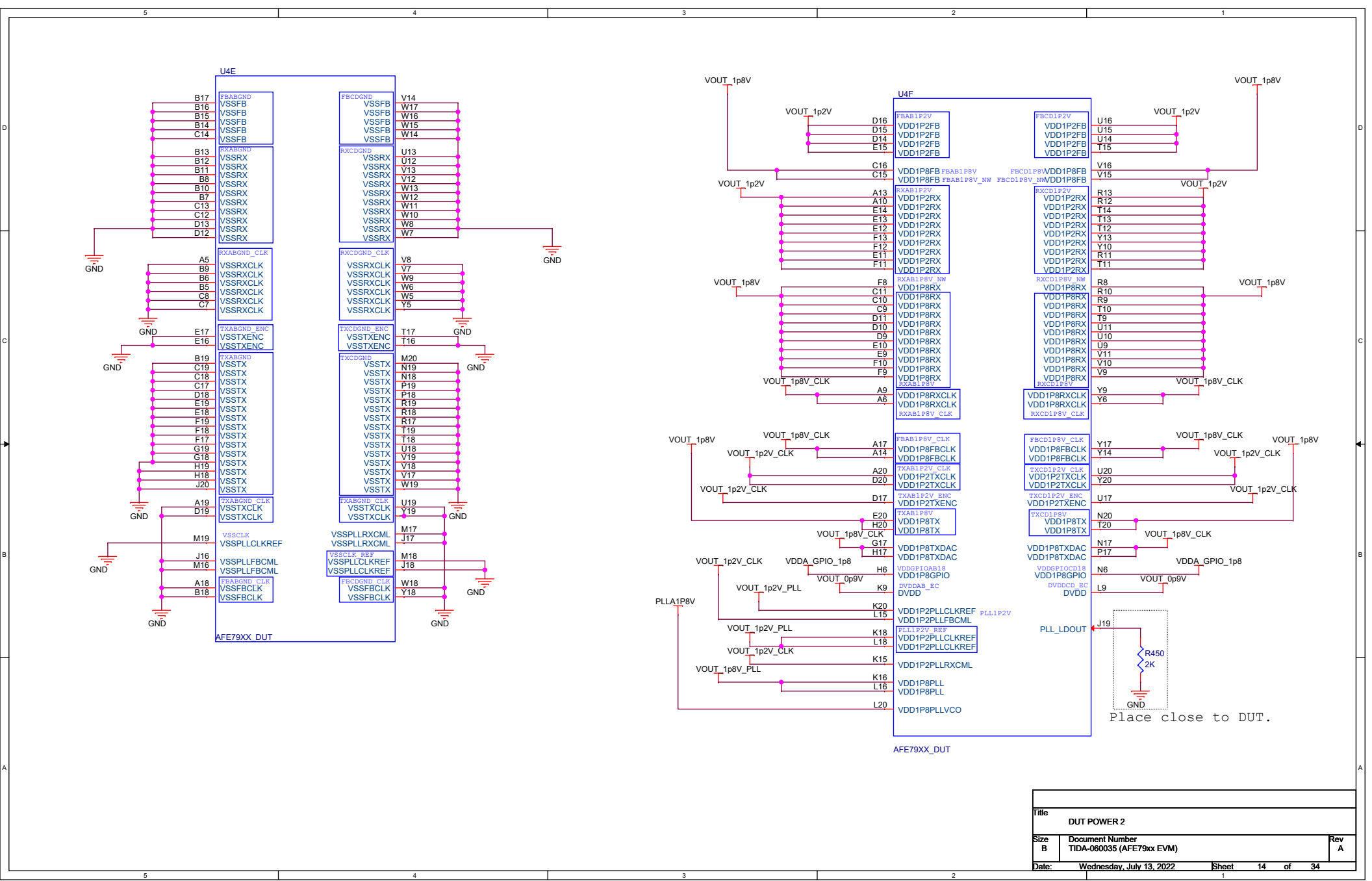


TEXAS INSTRUMENTS

Title: DUT POWER 1

Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
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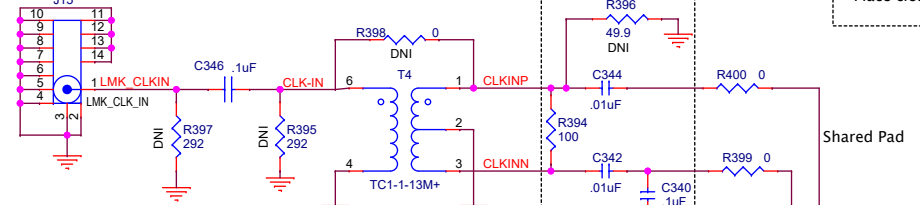
Date: Wednesday, July 13, 2022 Sheet 13 of 34



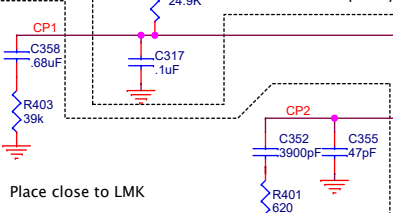
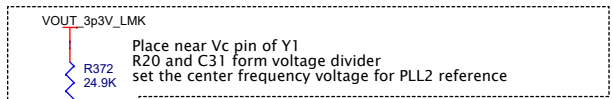
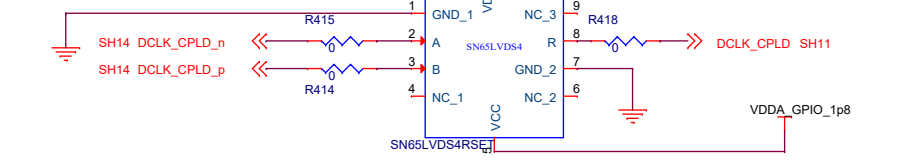
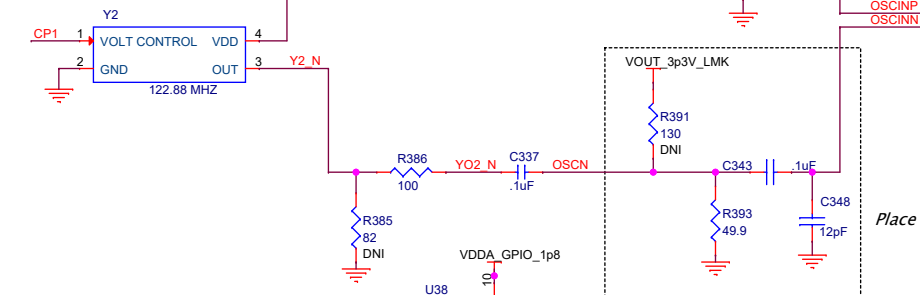
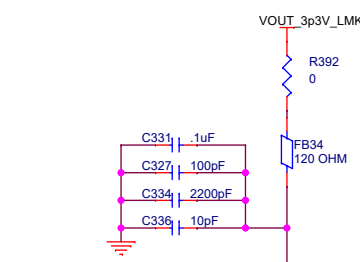
Place close to DUT.

Title		
DUT POWER 2		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 14 of 34

2921-61345-1S-SF
J15



R251 TO SHARE PADS W/ T3

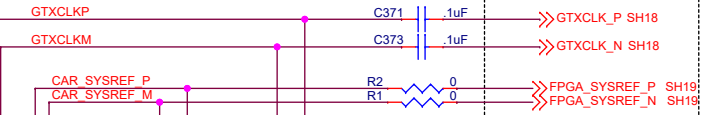


Place close to LMK

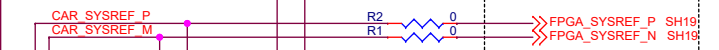
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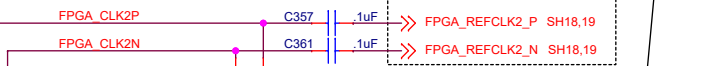
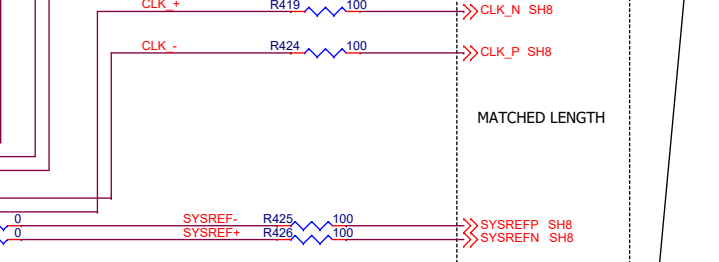
Place close to LMK



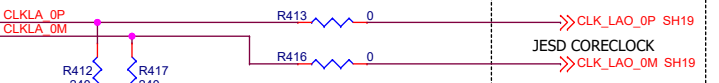
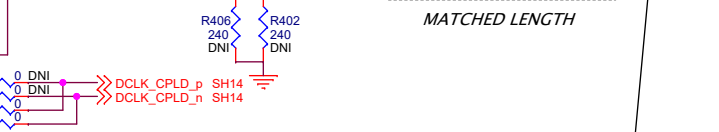
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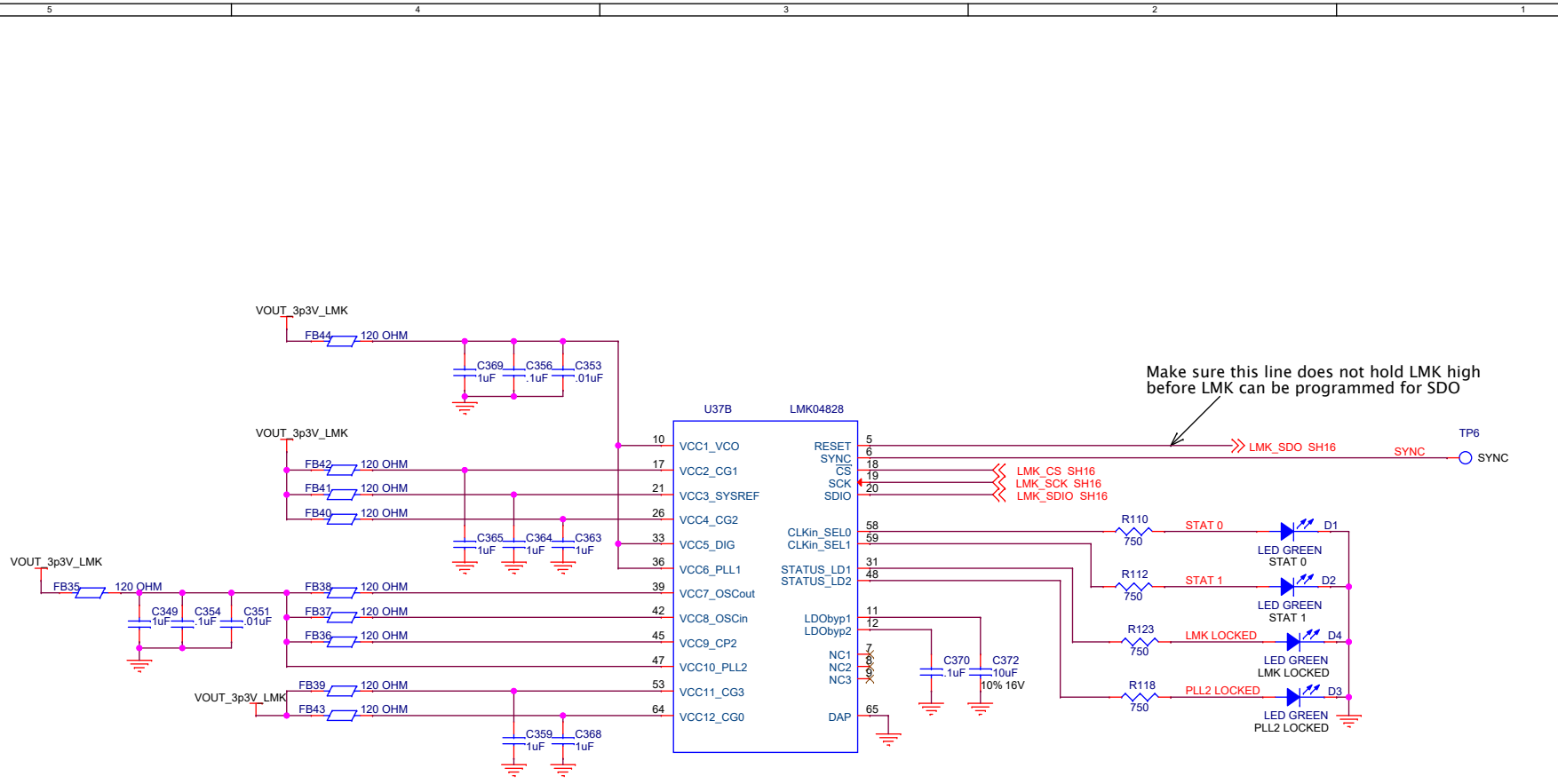
MATCHED LENGTH



MATCHED LENGTH

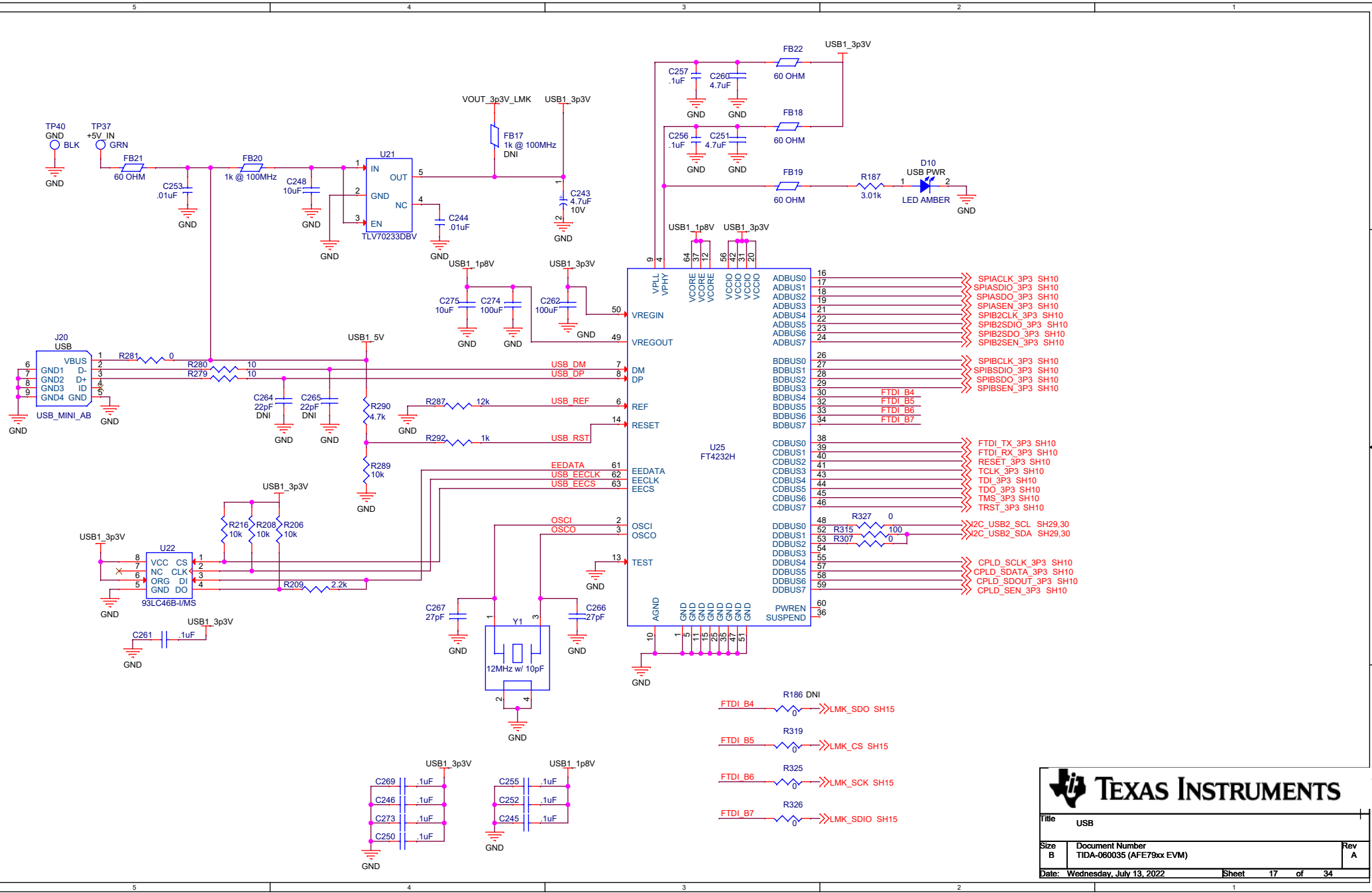


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Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
Date: Wednesday, July 13, 2022	Sheet 15	of 34



TEXAS INSTRUMENTS

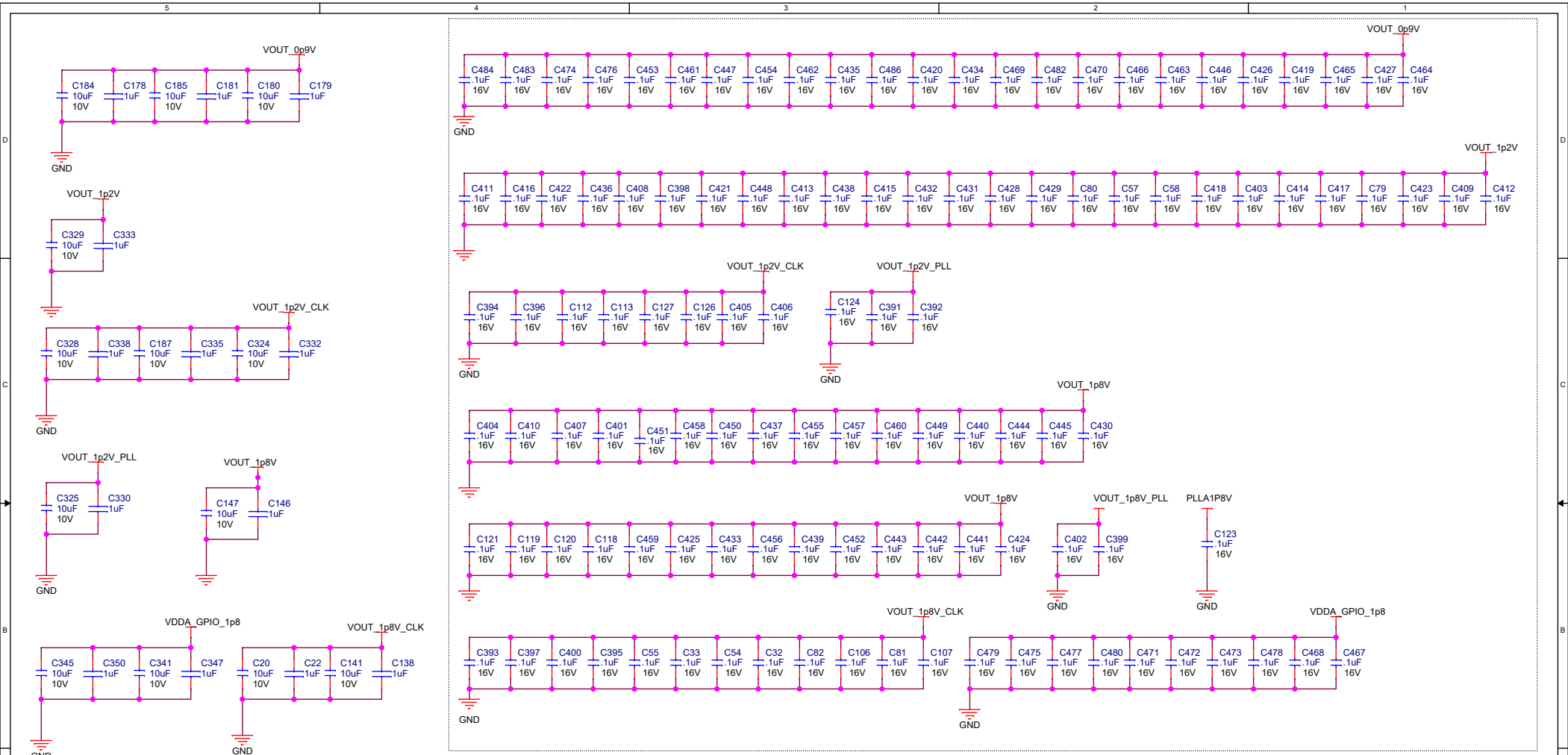
Title LMK		
Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
Date: Wednesday, July 13, 2022		Sheet 16 of 34



- FTDI B4 → R186 DNI → LMK_SDO SH15
- FTDI B5 → R319 → LMK_CS SH15
- FTDI B6 → R325 → LMK_SCK SH15
- FTDI B7 → R326 → LMK_SDIO SH15



Title			USB
Size	Document Number	Rev	
B	TIDA-060035 (AFE79xx EVM)	A	
Date:	Wednesday, July 13, 2022	Sheet	17 of 34



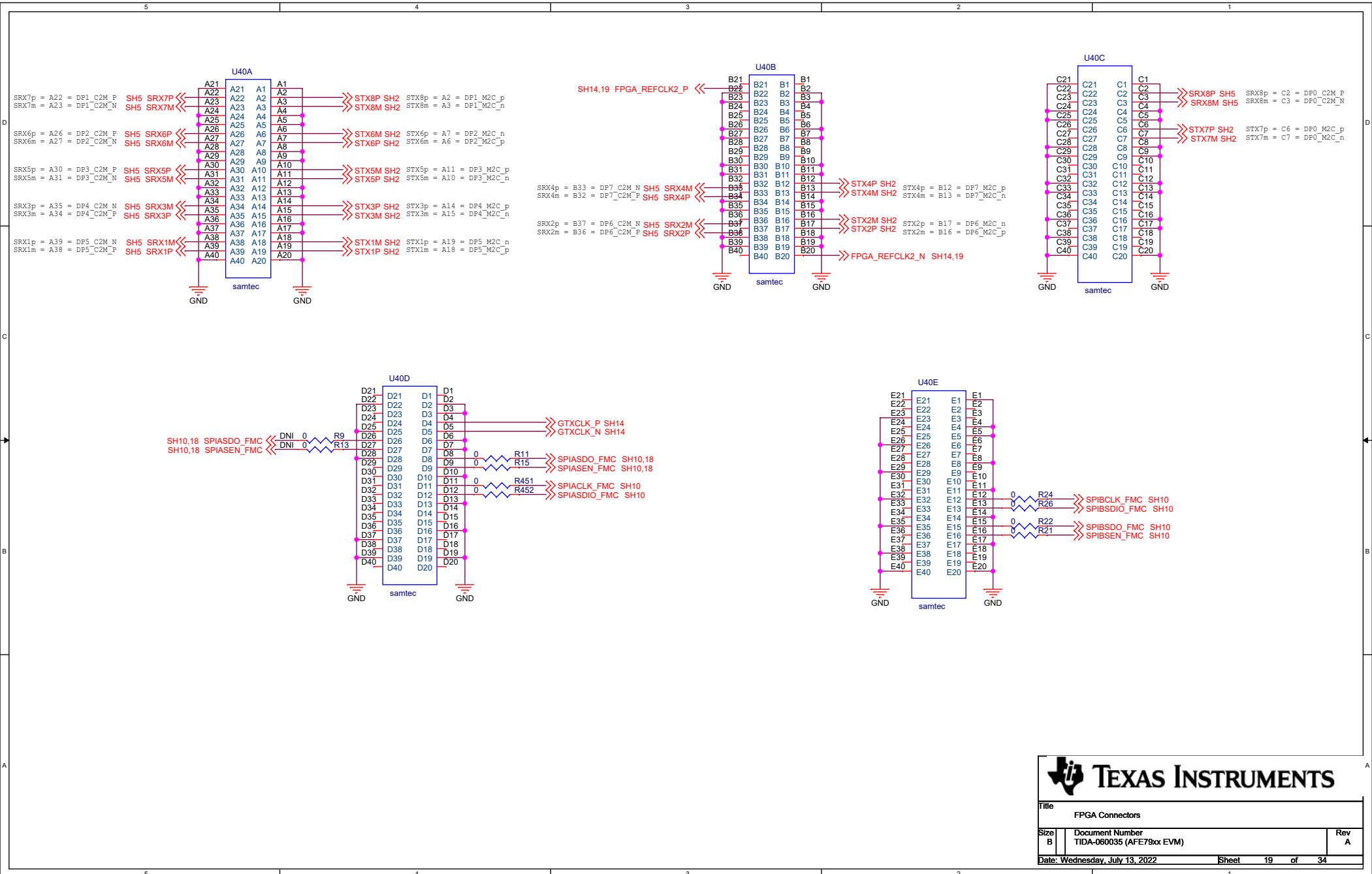
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TEXAS INSTRUMENTS

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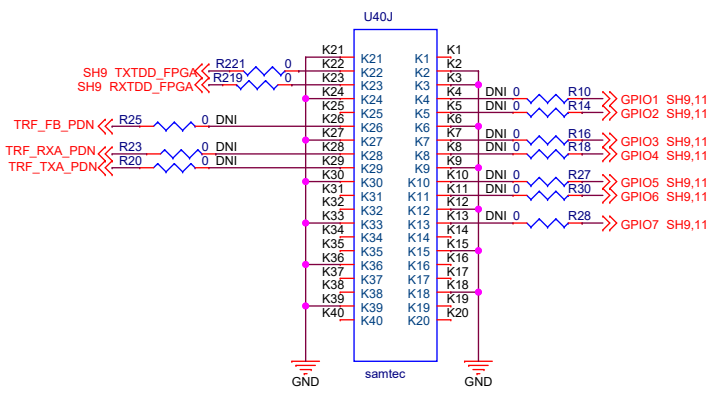
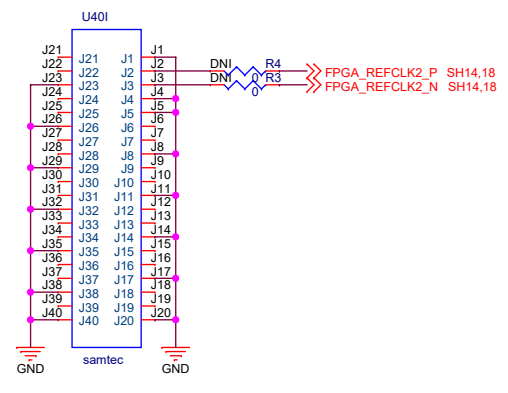
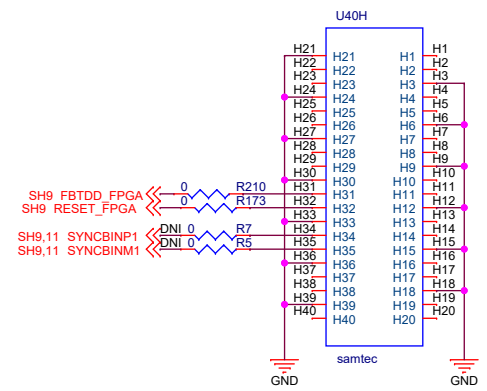
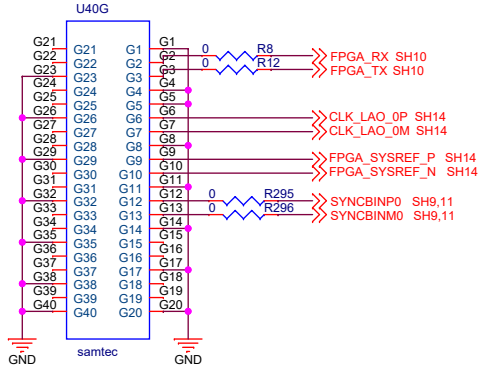
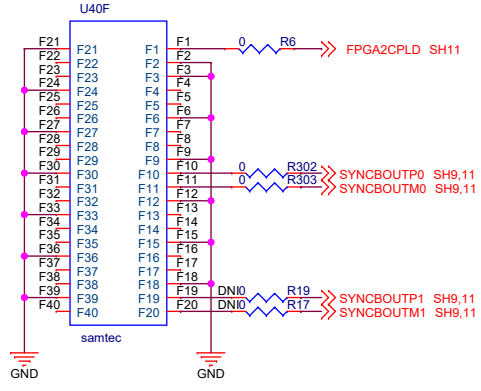
Size B | Document Number: TIDA-060035 (AFE79xx) | Rev EVM

Date: Wednesday, July 13, 2022 | Sheet 18 of 34



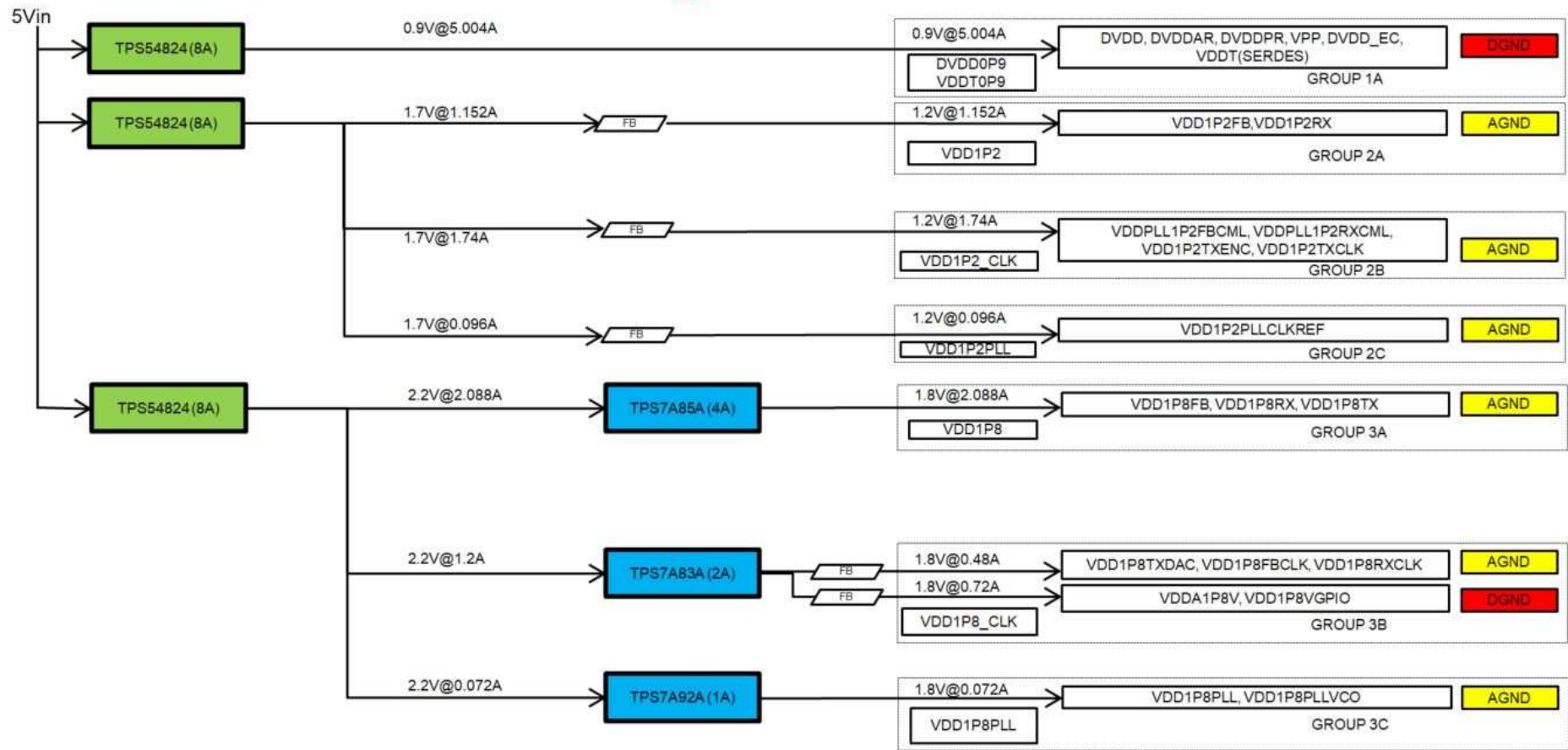
TEXAS INSTRUMENTS

Title FGPA Connectors		
Size B	Document Number TIDA-060035 (AFE79xx EVM)	Rev A
Date: Wednesday, July 13, 2022		Sheet 19 of 34

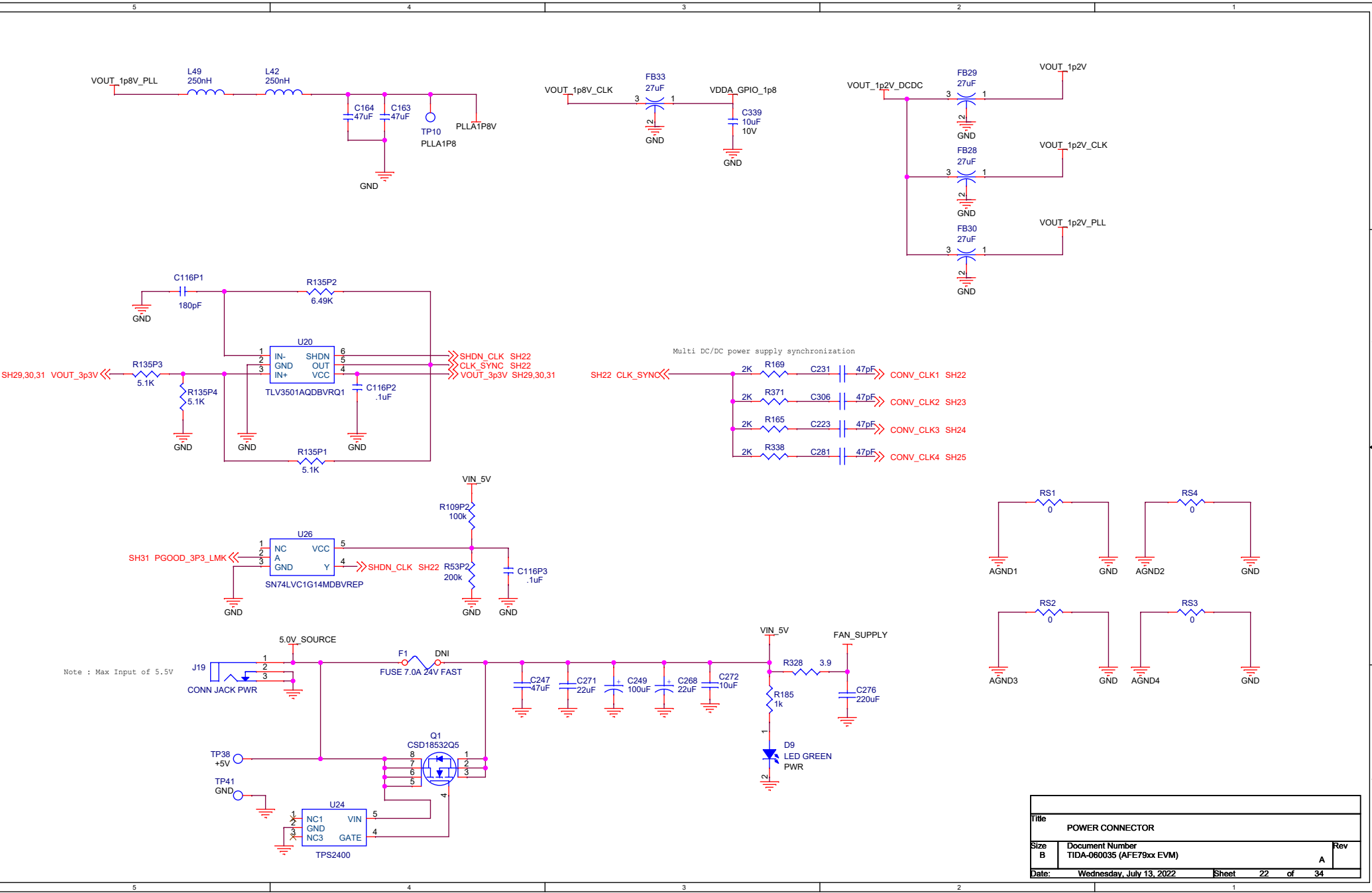


Title		
FPGA Connectors		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 20 of 34

1x AFE78xx Block Diagram

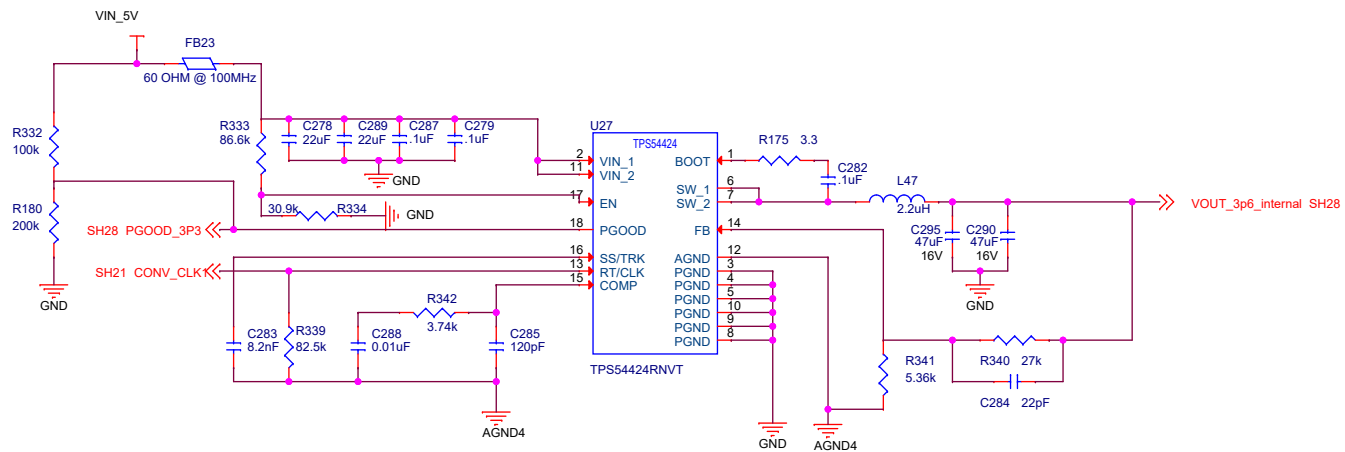


Title		
POWER TREE		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 21 of 34

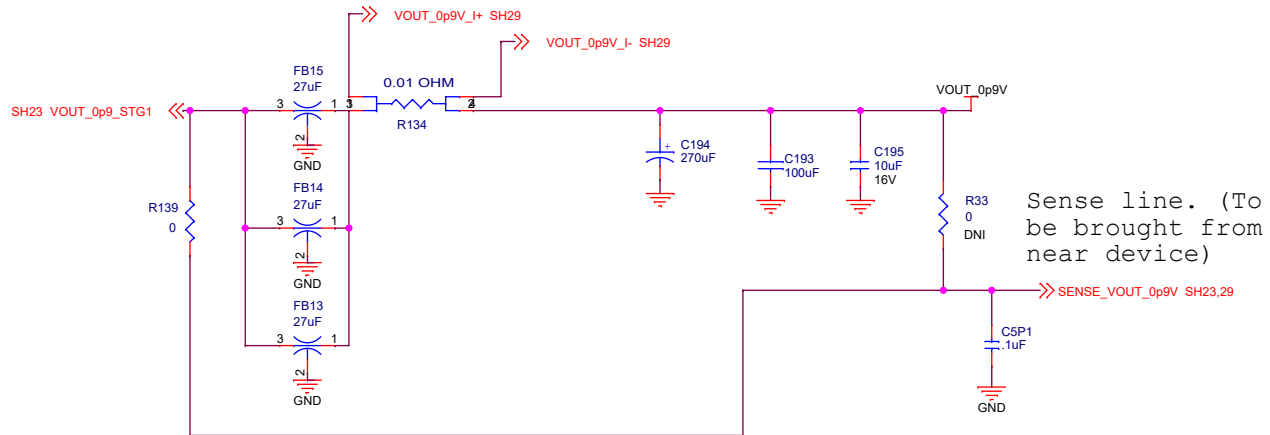
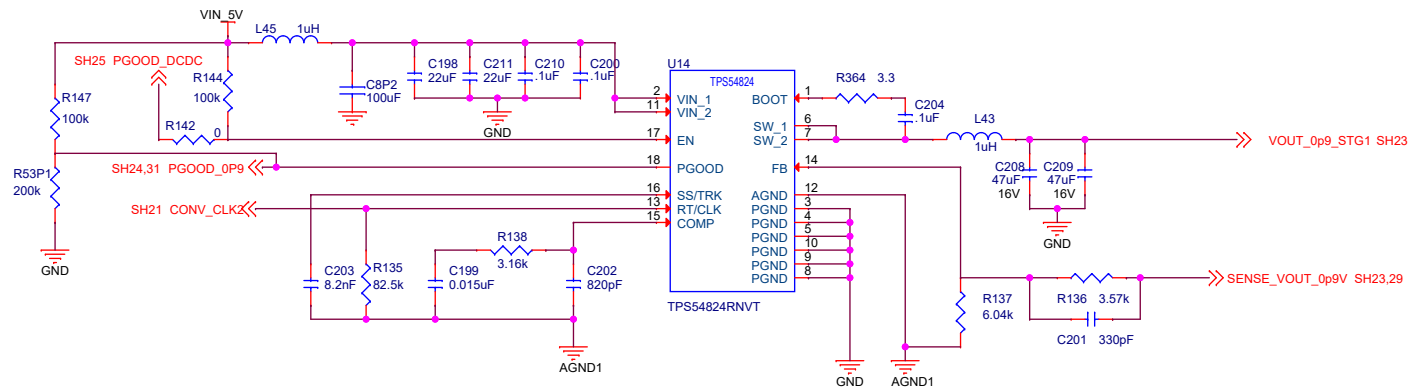


Note : Max Input of 5.5V

Title		
POWER CONNECTOR		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 22 of 34

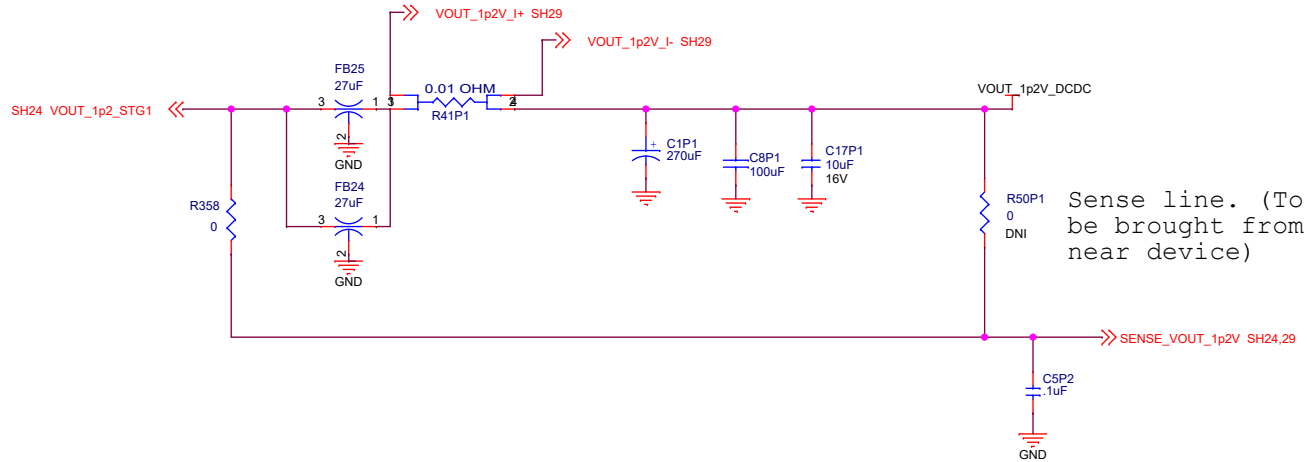
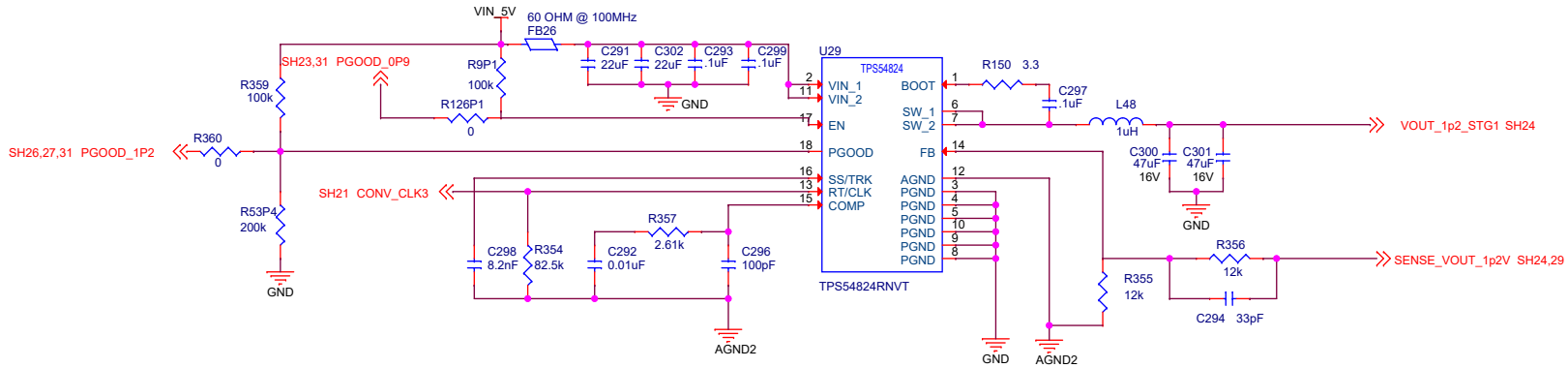


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DCDC 3.3V		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 23 of 34

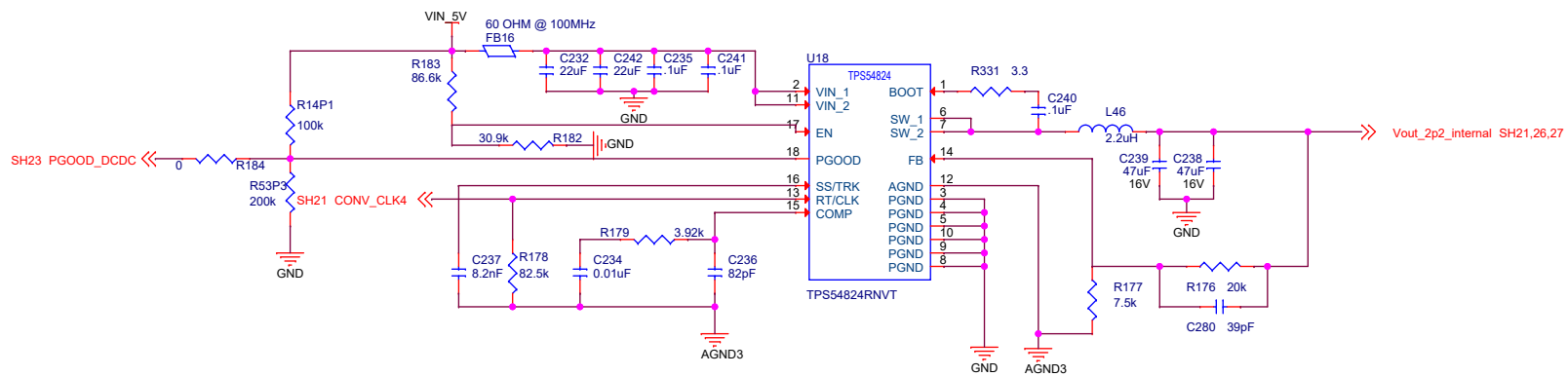


Sense line. (To be brought from near device)

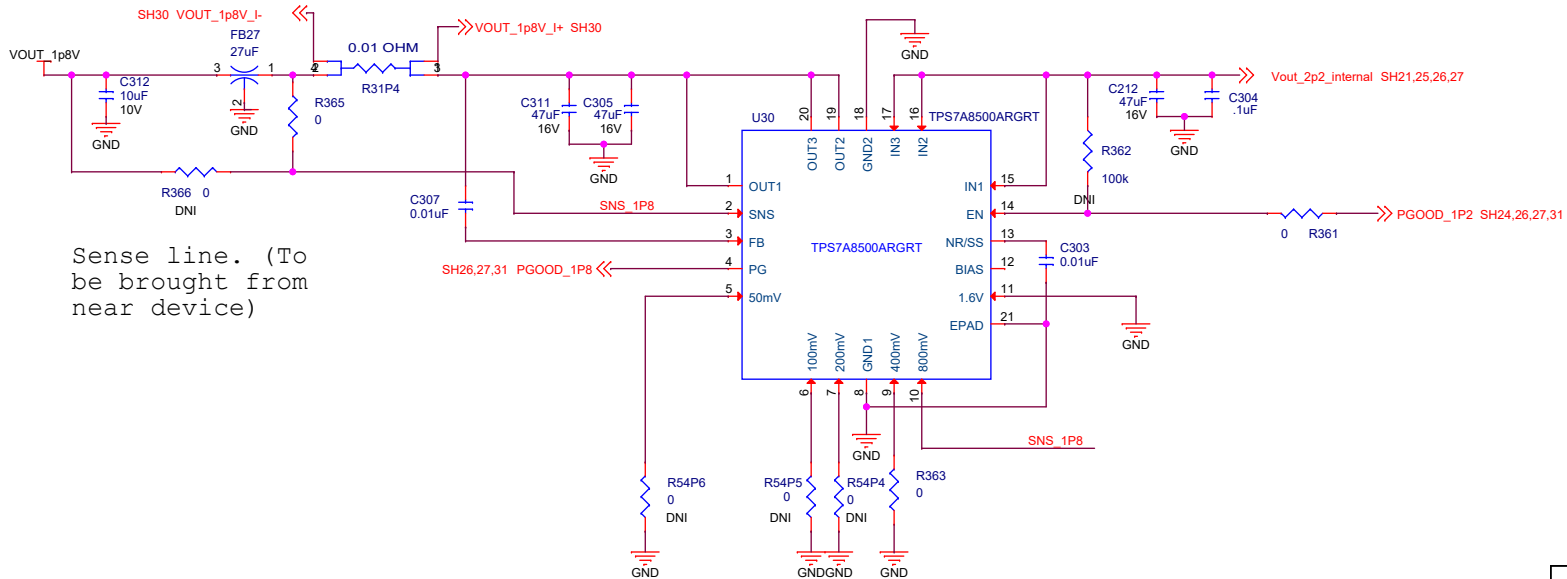
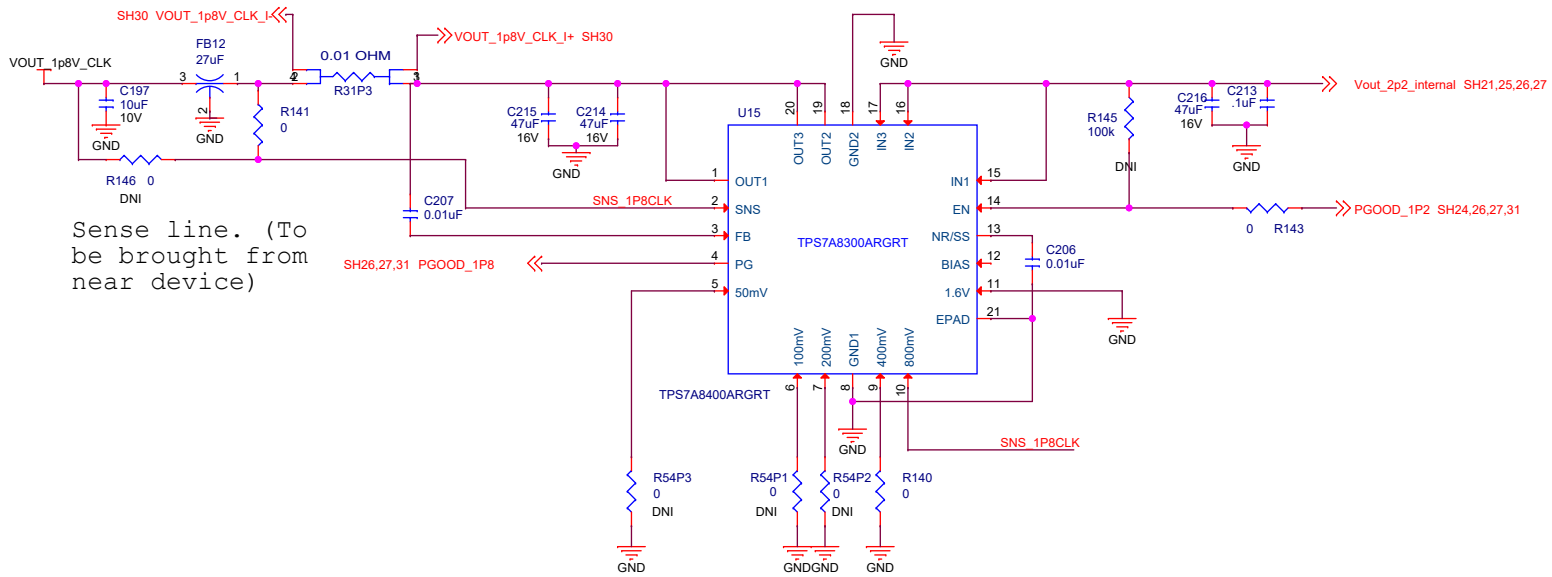
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Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 24 of 34



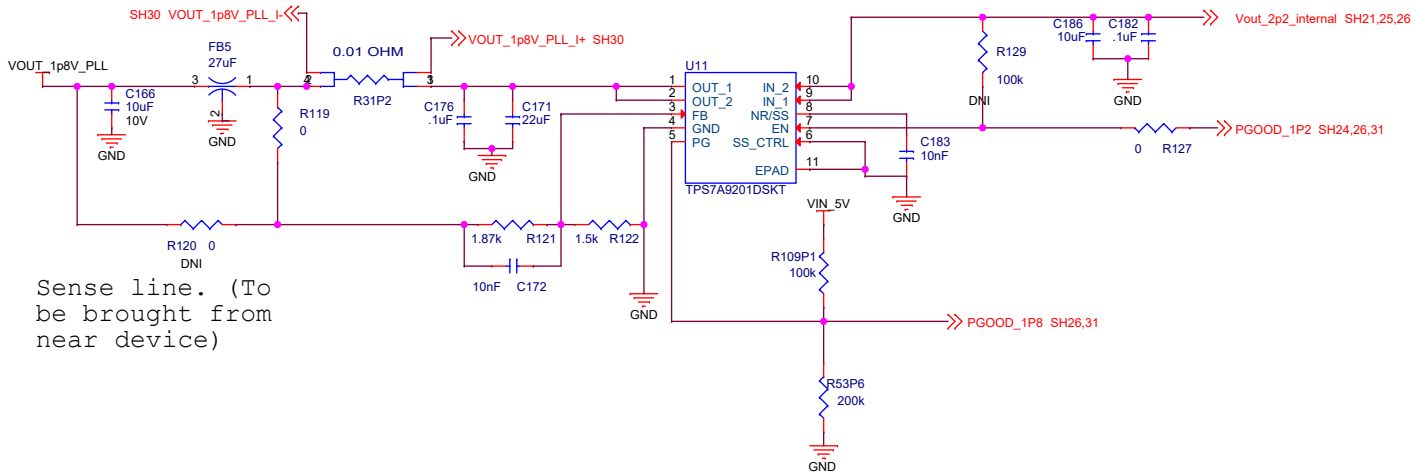
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Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 25 of 34



Title		
DCDC1.8V		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 26 of 34

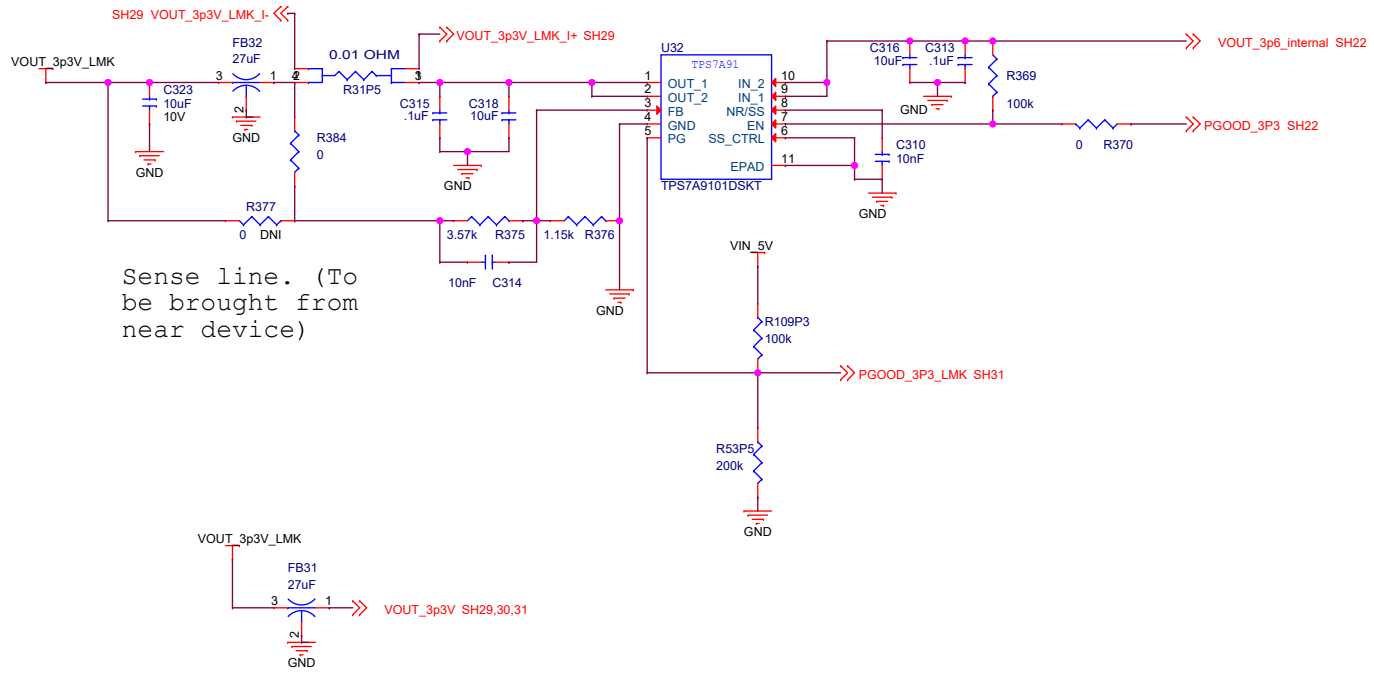


Title		
LDO 1.6V 1		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Friday, July 15, 2022	Sheet 27 of 34

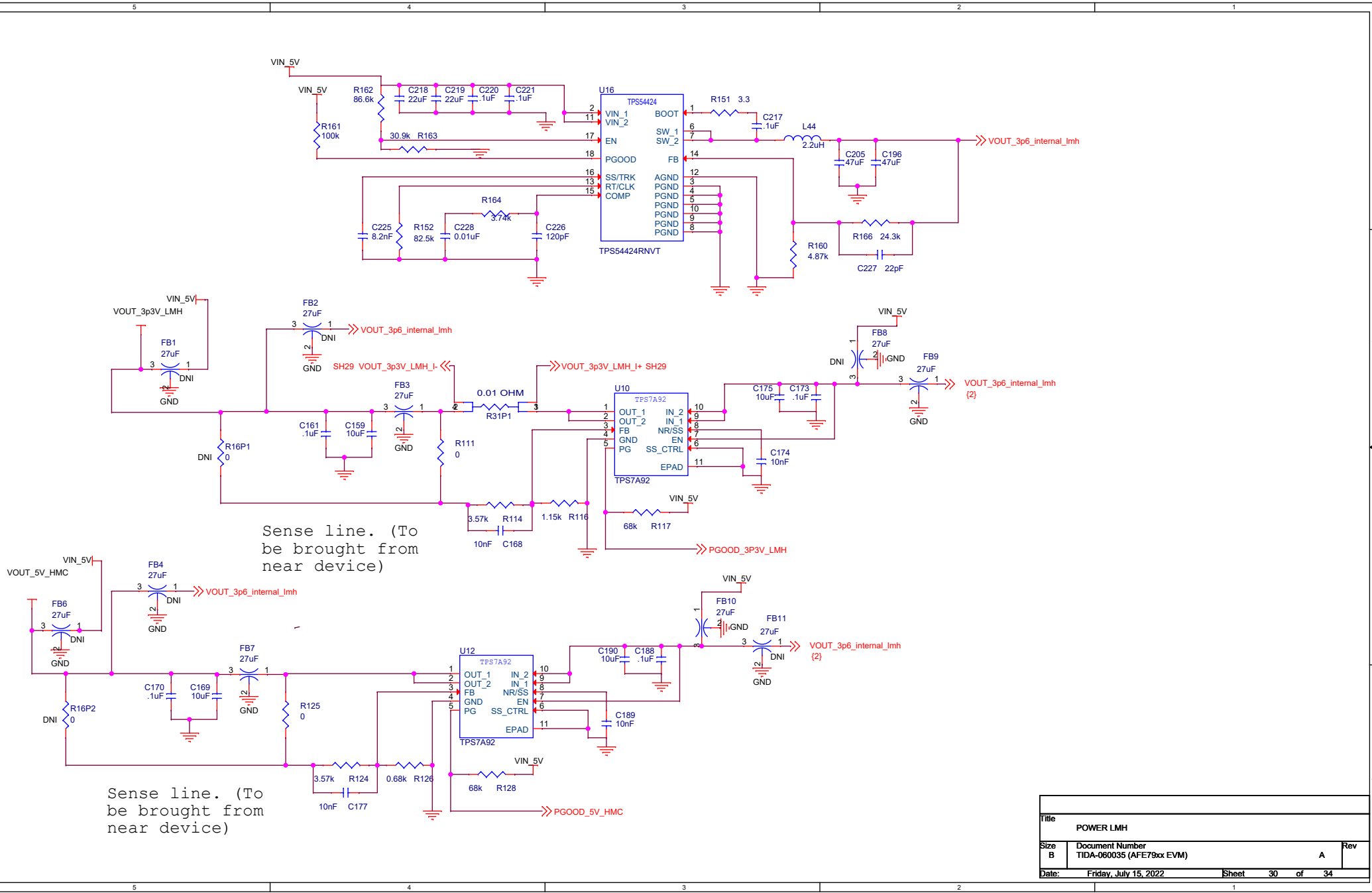


Sense line. (To be brought from near device)

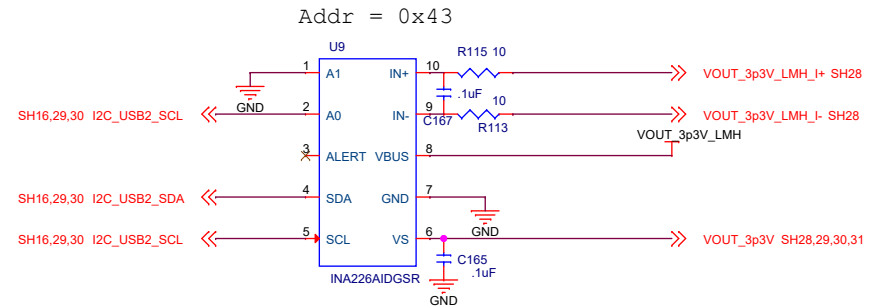
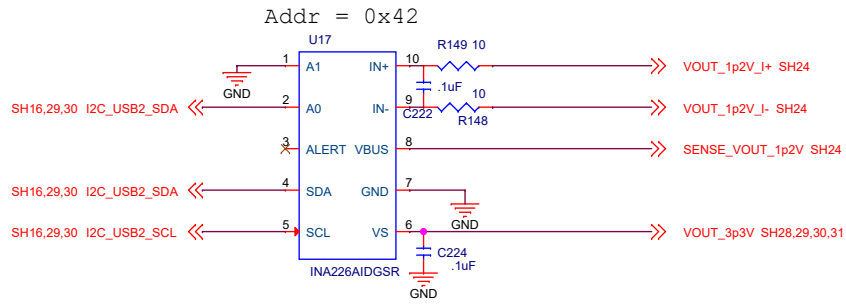
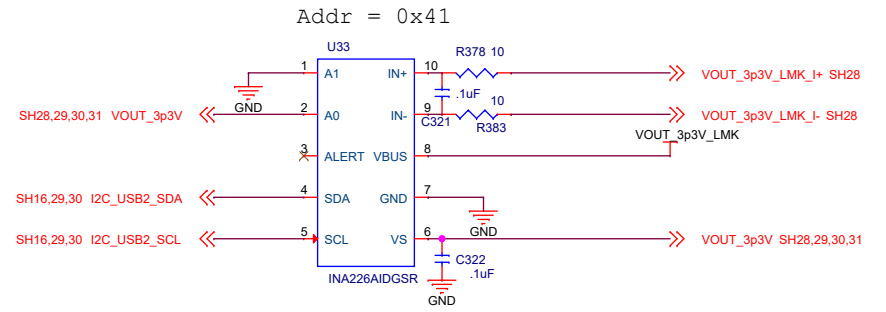
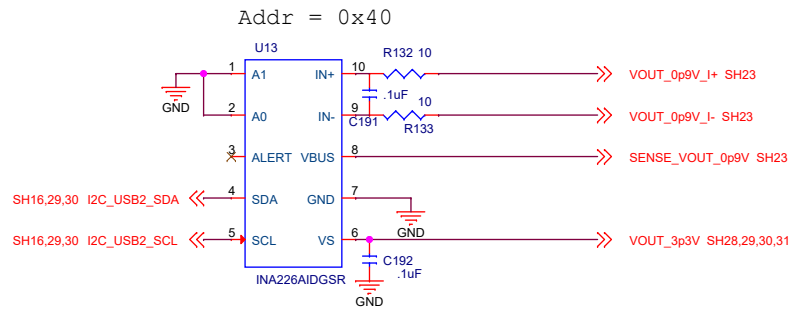
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Size	Document Number	TIDA-060035 (AFE79xx EVM)	
B		Rev A	
Date:		Friday, July 15, 2022	Sheet 26 of 34



Title		
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Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Friday, July 15, 2022	Sheet 29 of 34

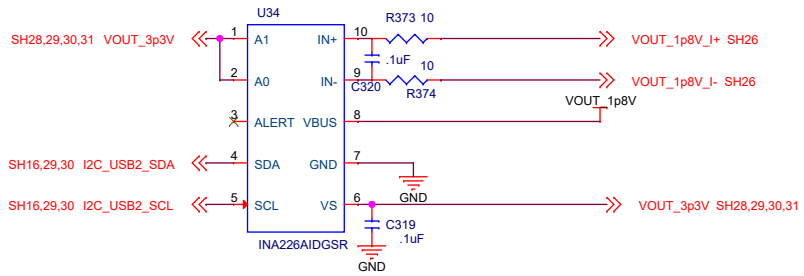


Title			
POWER LMH			
Size	Document Number	A	Rev
B	TIDA-060035 (AFE79xx EVM)		
Date:	Friday, July 15, 2022	Sheet	30 of 34

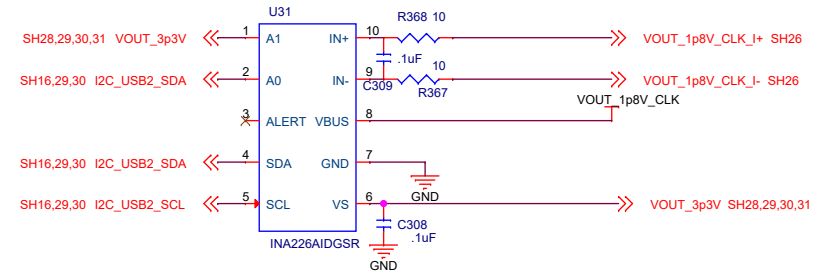


Title		
CURRENT SENSING 1		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 31 of 34

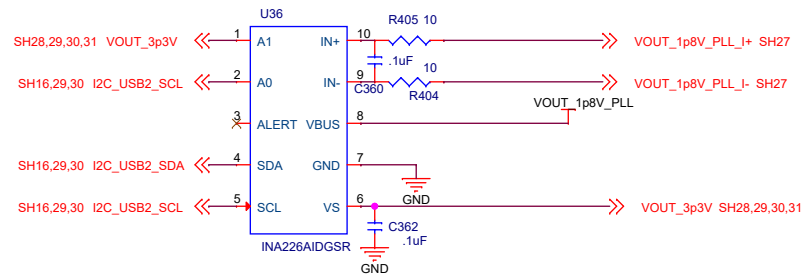
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Addr = 0x46

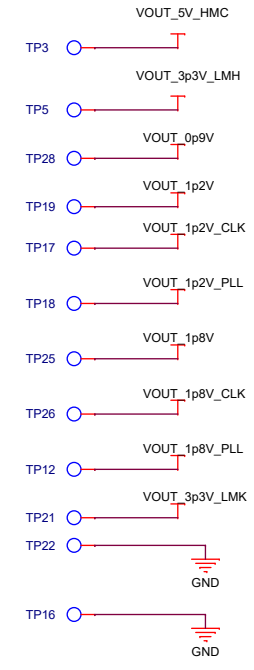
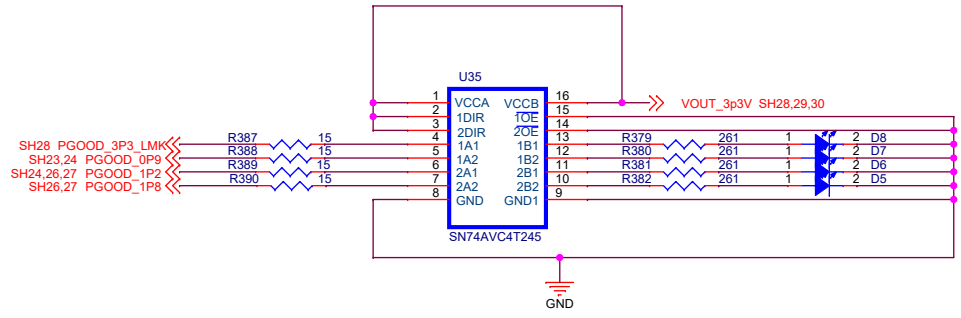


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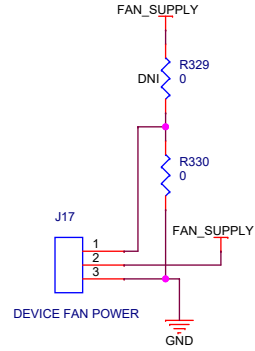
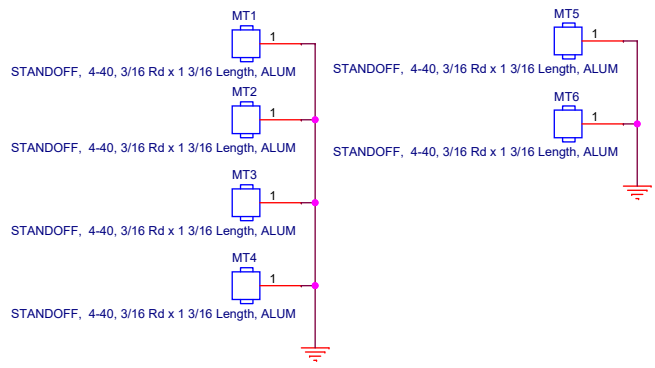
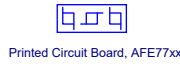
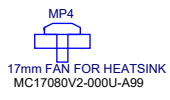
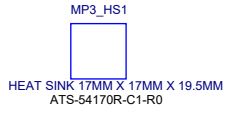


All VBUS to be connected to sense lines of LDO

Title		
CURRENT SENSING 2		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 32 of 34



Title		
POWER LEDS		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 33 of 34



Title		
HARDWARE		
Size	Document Number	Rev
B	TIDA-060035 (AFE79xx EVM)	A
Date:	Wednesday, July 13, 2022	Sheet 34 of 34