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Here's An Easy Way To Test Wideband Transimpedance Amplifiers

A Network Analyzer And Simple Three-Element Interface Are All That's Needed To Gather Meaningful Performance Data.

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As if building and compensating a wideband transimpedance amplifier for photodiode applications weren't challenging enough, measuring the amplifier's ac performance independently of the photodiode also presents a considerable hurdle. Often, the photodiode intended for the application has its own frequency response. In addition, if the photodiode is used to evaluate the amplifier, the technique used for injecting an optical signal into the photodiode may introduce an unknown frequency response.

To circumvent these problems and observe just the performance of the transimpedance amplifier itself, you can use a network analyzer source connected to the simple interface circuit described here. This passive circuit will deliver a low-level current signal from a capacitive source impedance, thus emulating the photodiode signal current and capacitance to the amplifier circuit.

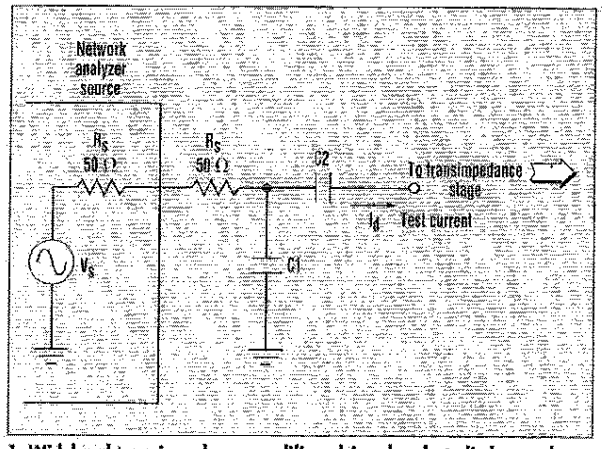
The test interface circuit from the network analyzer to the transimpedance amplifier under test is shown *(Fig. 1)*. Capacitor C2 would connect into the input of the transimpedance gain stage. If this is implemented using a high-open-loop-gain operational amplifier, the test current (I_d) will drive into a low impedance virtual ground. Intuitively, both C1 and C2 short out at high frequencies and the network analyzer simply delivers a current into the 50-Ω input-matching resistor, R_s.

On the other side of the matching resistor, that current splits between the two capacitors, with most of it going through C1 when C1>>C2. Continuing the assumption that C1 >> C2, and looking back toward C2 from the transimpedance gain stage, it will simply see a capacitive source impedance equal to C2 as C1 shorts to ground and both impedances become less than the resistive source impedances.

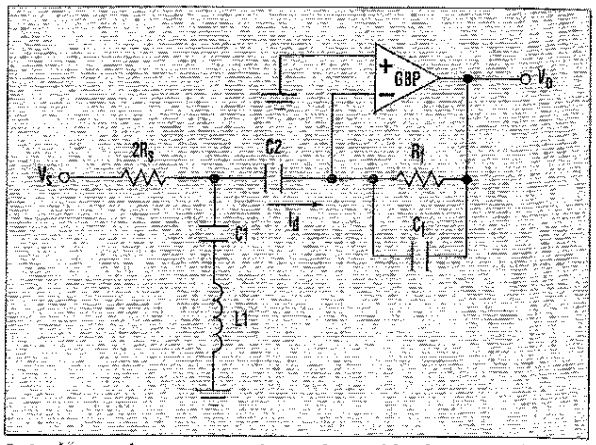
Continuing the assumption that C2 is feeding into a virtual ground, the Laplace transfer function for the transconductance from V_s to I_d for the interface circuit of Figure 1 may be written as:

$$\frac{I_d}{V_s} = \frac{1}{2R_s\left(1+\frac{C1}{C2}\right)} \cdot \frac{s}{\left(s+\frac{1}{2R_s(C1+C2)}\right)} \quad (1)$$

This equation shows a zero at dc and a high-frequency pole at $1/2\pi(2R_s(C1 + C2))$ Hz. At dc, there is no signal current injected through C2. The test current, I_d, increases with frequency until the pole frequency. Beyond this, a constant current set by the transconductance from the V_s source to I_d, $1/(2R(1+C2/C1))$, is delivered through C2. Equation 2 gives the Laplace expression for the output impedance looking back from the transimpedance gain stage towards C2.



1. Wideband transimpedance amplifiers driven by photodiodes can be tested using a network analyzer and a simple three-component interface circuit. The interface circuit emulates the photodiode's signal current and capacitance.



2. As this complete test circuit shows, the amplifier being tested connects to the interface circuit via capacitor C2. The circuit details the parameters that must be taken into account when calculating the component values for the interface circuit.

$$Z_o = \frac{1}{\frac{C1 \times C2}{C1 + C2}} \cdot \frac{s + \frac{1}{2R_s(C1 + C2)}}{s\left(s + \frac{1}{2R_sC1}\right)} \quad (2)$$

The source impedance for the test interface circuit starts out at infinity at dc, decreasing with frequency due to the first pole at s = 0 until it reaches a zero that occurs at the same frequency as the pole in the transconductance shown in Equation 1. This source impedance then goes through another pole at $1/2\pi(2R_sC1)$ Hz. This causes the source impedance to look like a capacitor equal to the series combination of C1 and C2 above that corner frequency.

Although this zero/pole pair in the source impedance doesn't exactly match the simple source capacitance of a photodiode detector, the key requirement is that it look capacitive at frequencies on the order of the closed-loop transimpedance bandwidth for the amplifier under test. When C1>> C2, the zero/pole pair in Equation 2 cancels each other giving just the desired capacitive source impedance equal to the series combination of C1 and C2.

With C1>>C2, the source capacitance for the transimpedance stage will be nearly equal to C2. This will constrain C2 to equal the expected photodiode capacitance (C_d) that the circuit is intended to emulate. With the input resistor, R_s, set to match the network analyzer's source impedance (normally 50 Ω), only C1 remains to be set. The value for C1 will determine both the low frequency corner for the current delivered through C2 (where it goes flat with frequency) and the transconductance from V_s to I_d—neither of which are critical.

One important parasitic does need to be considered before setting C1. Capacitor C1 may go through self-resonance due to its series inductance prior to the expected corner frequency of the completed transimpedance amplifier under test. The resulting increase in the current delivered through C2 can obscure the actual roll-off frequency for the amplifier. This suggests that the value for C1 be set to give a self resonant frequency much higher than the expected closed-loop transimpedance bandwidth.

However, decreasing C1 to move this self-resonant frequency up also increases the pole frequency for the transconductance from V_s to I_d. Capacitor C1 must be set to balance the requirement to bring I_d flat with frequency well before the anticipated transimpedance bandwidth. This suggests a high C1 value; but, C1 must be low enough in value to move its own self-resonance well beyond the test frequency range of interest.

To show the constraints that will lead to a solution for C1, consider Figure 2. This diagram shows the input interface feeding into an op-amp transimpedance amplifier where the op amp has a gain bandwidth product equal to GBP (in Hz).

To use this test interface circuit, while minimizing the interaction with L1, set the self resonant frequency, F_r, as given in Equation 3.

$$F_R = \frac{1}{\sqrt{L1C1}} = \beta F_{-3dB} \quad (3)$$

In this equation, F_{-3dB} is the anticipated transimpedance bandwidth and β is the ratio of the self-resonant frequency to F_{-3dB}.

One useful design point for setting the transimpedance compensation is to set C_f to give a maximally-flat Butterworth closed-loop frequency response. This can be achieved by setting:

$$\frac{1}{R_fC_f} = \frac{2\pi F_o}{\sqrt{2}} \quad (4)$$

$$F_o = \sqrt{\frac{GBP}{2\pi R_fC_s}} \quad (5)$$

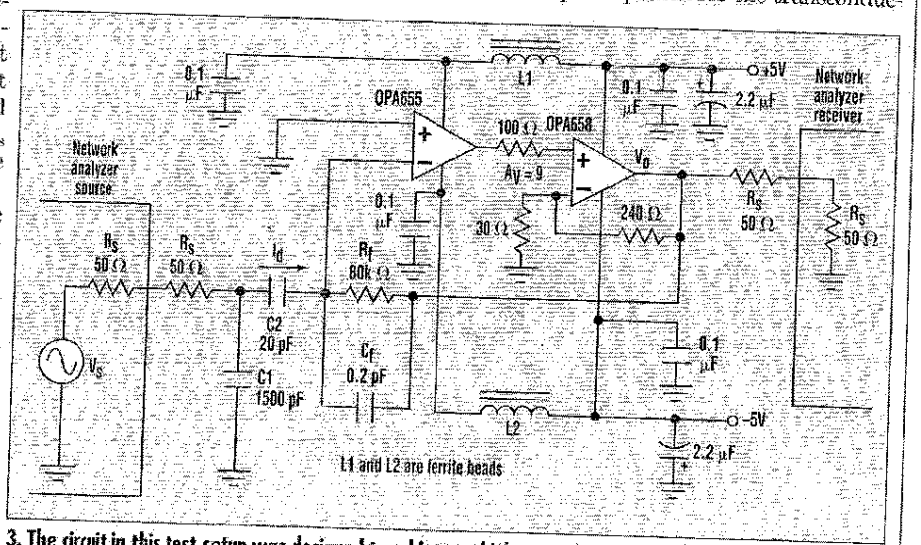
In Equation 5, C_s is the total capacitance on the inverting op-amp pin, which is equal to (C1C2/(C1+C2)) + C_p, where C_p equals the op-amp input capacitance.

In this analysis, we are simply trying to set C1 approximately, in order to measure the high-frequency roll-off of the transimpedance amplifier. So, approximate C_s = C2 in the equation for F_o in the analysis to get C1. However, the total value for C_s (including the op-amp input parasitics) will need to be used in setting C_f for the correct compensation.

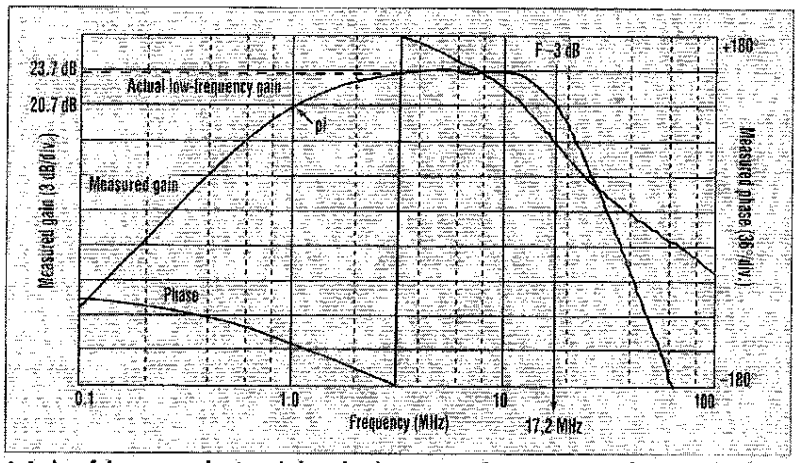
One useful feature in setting C_f to get this maximally-flat compensation is that the resulting closed-loop frequency response will then show an $F_{-3dB} = F_o$. This allows the F_o shown above (with C_s replaced by C2) to be placed into Equation 3 in place of F_{-3dB}. Once that is done, a solution for C1 may be written:

$$C1 = \frac{1}{L1\beta^2(2\pi F_o)^2} \quad (6)$$

Equation 6 gives one constraint on C1. Putting this expression for C1 into the pole equation for the transconduc-



3. The circuit in this test setup was designed to achieve as high a transimpedance gain as possible when driven by a 20-pF source capacitance and achieving a 14-MHz signal bandwidth.



4. A plot of the measured gain and phase for the transimpedance test circuit shows results that closely matched those predicted by circuit analysis.

tance from V_s to I_d. (Equation 1) gives:

$$P_1 = \frac{L1\beta^2(2\pi F_o)^2}{2R_s(2\pi)}\,Hz \qquad (7)$$

Here, (C1+C2) in the pole expression has been simplified to C1 (when C1>>C2). Now, substituting in for F_o from Equation 4 (and using $C_s = C2$), gives:

$$P_1 = \frac{L1\beta^2(2\pi)^2}{2R_s(2\pi)}\,\frac{GBP}{R_fC2(2\pi)}\,Hz \qquad (8)$$

$$= \frac{L1\beta^2 GBP}{2R_sR_fC2}\,Hz$$

With everything on the right side of Equation 8 determined by the design, and with a β selected, the low frequency pole (P1) for Equation 1 will be set. This will determine the low frequency point at which the test current into the transimpedance amplifier, I_d, becomes constant with frequency.

It is generally unnecessary to measure the low-frequency transimpedance response since an op amp implementation is generally dc coupled. However, the range from P1 (where I_d becomes flat with frequency) up to where the amplifier is expected to be band limited, should be adequate to show the amp's gain and flatness. To ensure this, an additional variable, $\alpha = F_o/P1$, should be defined. If, for instance, α were set to 10, you should see approximately one decade of flat transimpedance gain in making this measurement. Equation 9 shows this equation for $\alpha = F_o/P1$ where F_o from Equation 4 and P1 from Equation 8 have been substituted.

$$\alpha = \frac{2R_sR_fC2\sqrt{\frac{GBP}{2\pi R_fC2}}}{L1\beta^2 GBP} \qquad (9)$$

$$= \frac{2R_s\sqrt{\frac{1}{2\pi}}}{L1\beta^2\sqrt{\frac{GBP}{R_fC2}}}$$

If we now pick an α (which is the ratio of the expected transimpedance bandwidth to the low-frequency point at which I_d becomes constant with frequency), Equation 9 may be solved for β to get:

$$\beta = \sqrt{\frac{2R_s\sqrt{\frac{1}{2\pi}}}{L1\alpha\sqrt{\frac{GBP}{R_fC2}}}} \qquad (10)$$

Selecting values for all of the terms on the right side of Equation 10 will give the maximum allowed value for β. Picking a β less than or equal to this value will set up the interface to provide a test current with certain properties. The test current is constant over some frequency range greater than α, but below the expected F_{-3dB}, and it does not show an increasing I_d due to the self resonance of C1 until a frequency βF_{-3dB} is reached. With β selected less than or equal to the evaluation of Equation 10, a value for C1 may be set using Equation 6.

There is an alternative approach to accounting for the frequency dependent test current delivered by this interface circuit. Perform a swept frequency calibration of I_d vs. V_s and then use the network analyzer's calibration features to normalize out this nonuniformity. Since we are trying to produce a test current into a virtual ground, this normalization would require an ideal transimpedance stage.

Alternatively, a wideband passive current probe (such as the CT-2 probe from Tektronix) could be used, recognizing that the probe reflects a load impedance into the circuit. A probe does, however, introduce its own frequency response artifacts that must be separated from the DUT response. The totally passive approach shown here will give good results with a lot less effort once C1 is carefully selected.

To show measurement results using this test interface, we tested a very challenging transimpedance design that uses off-the-shelf components. This design sets out to deliver as much transimpedance gain as possible from a 20-pF source capacitance, while achieving a 14-MHz signal bandwidth and as low an output integrated noise as possible. This design achieved 80-KΩ transimpedance gain with the required 14-MHz bandwidth. It also had an equivalent input current noise density (if integrated at the output to 0.707 × 14 MHz) of 7.5 pA/√Hz. The completed test circuit and measurement interface are shown in Figure 3.

The design uses a wideband, unity gain stable, FET-input op amp (the OPA655) along with an additional gain stage inside the loop of this first amplifier. This second-stage amplifier, a very wideband current feedback op amp (the OPA658), essentially increases the gain-bandwidth product of the first-stage amplifier. Multiplying the 240-MHz gain-bandwidth product (GBP) of the OPA655 by the second-stage gain of +9 gives the equivalent of a 2.2-GHz GBP to work with. The design for maximum transimpedance gain is limited by the minimum achievable feedback capacitor, C_f.

In this case, a 0.2 pF minimum value allowed an 80-KΩ transimpedance gain to be achieved with a flat frequency response. Evaluating Equation 5 using this 2.2-GHz GBP and C_s = 20 pF + 2 pf (OPA655 input parasitic capacitance), shows that F_o = 14 MHz.

Since the feedback impedance pole at $1/R_fC_f$ has been set equal to $0.707F_o$, the resulting $F_{-3dB} = F_o$.

To set the values for the test interface circuit, Equation 10 must be evaluated. This design initially targeted an $\alpha = 10$ and assumed a maximum L1 = 3 nH. This value for L1 is a reasonable estimate for chip capacitors or leaded ceramic capacitors if the leads are kept very short. Equation 11 shows the calculation for maximum β.

$$\beta \le \frac{2(100\Omega)\sqrt{\frac{1}{2\pi}}}{\sqrt{3nH(10)}\sqrt{\frac{2.2GHz}{80K\Omega(20pF)}}} = 8.5 \quad (11)$$

For this design, an initial β = 5 was selected. This will put the self resonant frequency for C1 at a frequency at least five times the anticipated transimpedance bandwidth. Solving Equation 5 for this design gives Equation 12:

$$C1 = \frac{1}{3nH(5)^2(2\pi 14MHz)^2} \quad (12)$$
$$= 1725\ pF$$

The design target for C1 was reduced to a standard value of 1500 pF in practice. Using 1500 pF will set the low frequency pole in Equation 1 to 1 MHz.

Recognizing that the total capacitive source impedance is the series combination of C1 and C2, will increase the required C2 from its ideal value of 20 pf to 20.3 pF. This adjustment was within the capacitor tolerances—so we simply used a 20-pF value for C2.

The last factor to consider is the anticipated measured transimpedance gain. The first part of Equation 1 shows the anticipated transconductance from V_s to I_d in the midband frequency range once the P1 pole frequency is exceeded. This transconductance is then multiplied by the transimpedance gain (equal to R_f) to get the expected voltage gain from V_s to V_o. Equation 13 combines these into an expected voltage gain.

$$\frac{V_o}{V_s} = \frac{R_f}{2R_s\left(1 + \frac{C1}{C2}\right)} \quad (13)$$

Substituting the values from Figure 3 predicts a measured gain of 10.53 V/V (or 20.45 dB). The network analyzer will actually measure the gain after the 6-dB loss is taken through the series matching resistor at the output. Output matching is optional for this application but very useful for network analyzer measurements. Since the OPA658 will deliver this output signal, and it's optimized to drive 100-Ω loads with no loss in performance, this should not introduce errors into the measurement.

The 6-dB loss through this output matching resistor can be normalized out by performing a "thru" calibration of the analyzer by itself. Do this by connecting the output of V_s directly into the measurement port with a cable and performing a "thru" calibration. This will normalize out this last 6-dB loss and any nonuniformities in the signal source or measurement port over the test frequency.

Figure 4 shows the measured gain and phase for the transimpedance gain stage plus the test interface of Figure 3. These measured results very closely match those predicted by the analysis. The increasing portion of the gain curve comes from the zero in the transconductance of the test interface circuit as shown by Equation 1.

The frequency response for just the transimpedance amplifier will continue flat down to dc at the midband gain of Figure 4 (shown as a dotted line). The measured low-frequency corner occurs exactly at the predicted 1 MHz point. The measured 23.7 dB midband gain is very close to the predicted 23.45 dB. The difference is attributable to component tolerances.

The measured high-frequency corner comes at a slightly higher frequency than predicted—17.2 MHz vs. a predicted 14 MHz. This is likely due to the additional phase shift inside the loop introduced by the OPA658 gain stage. Even though this amplifier has a small signal bandwidth greater than 200 MHz at the gain of +9 used here, its 0.8-ns propagation delay introduces an additional 8° phase shift at the loop-gain crossover frequency of 28 MHz. This slight degradation in phase margin is extending the closed-loop bandwidth.

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