

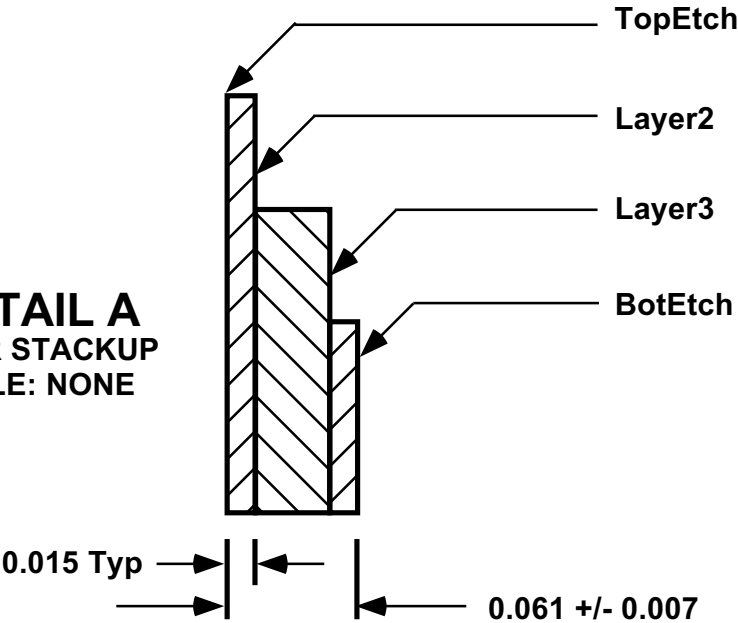
NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: PER IPC-4101/24
- 1A. LAMINATE: HIGH-TEMPERATURE FR4
- 1B. FINISHED BOARD: .0020 +/- .0005 INCH OUTSIDE LAYERS AND .0014 +/- .0005 INCH INSIDE LAYERS, COPPER.
- 1C. ALL COPPER LAYERS MUST BE SPACED PER DETAIL "A".
- 1D. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER. ANY TIN, TIN/LEAD OR GOLD PLATING, SOLDERMASK AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN FINISHED BOARD THICKNESS.
- 1E. ALL INNER LAYERS MUST BE OXIDE COATED.
2. THE CONDUCTOR PATTERN MUST BE ETCHED USING ARTWORK 880012941-002 REV A SUPPLIED WITHIN FABRICATION FILES' ARCHIVE 885012941-002 REV A OR GREATER.
3. ALL CONDUCTOR LAYERS MUST BE REGISTERED WITHIN +/- .005 INCH FROM TRUE POSITION.
4. ETCH TOLERANCES:
- 4A. ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0015 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
- 4B. ALL INTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0010 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
5. BOARD MUST BE NC DRILLED USING DRILL DATA SUPPLIED.
6. DRILL TOLERANCES AND HOLE SIZES ARE FOR FINISHED BOARD:
- ALL .008 & .010 INCH DIA. PLATED THROUGH HOLES ARE + .001/ -.008 INCH.
- ALL PLATED THROUGH HOLES TO .080 INCH ARE +/- .003 INCH.
- ALL PLATED THROUGH HOLES OVER .081 INCH ARE +/- .005 INCH.
- ALL NON-PLATED THROUGH HOLES ARE +/- .005 INCH.
7. ALL HOLES MUST BE REGISTERED WITHIN +/- .003 INCH FROM TRUE POSITION.
8. MINIMUM ANNULAR RING MUST BE .002 INCH.
9. PLATING:
- 9A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0015 INCH MAX. THICK COPPER.
- 9B. FINISH: IMMERSION GOLD: 2 TO 8 MICROINCHES GOLD OVER 120-240 MICROINCHES OF ELECTROLESS NICKEL.
10. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
11. SOLDERMASK: PER IPC-SM-840
- 11A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
- 11B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
- 11C. COLOR GREEN AND SOLVENT FREE.
- 11D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK MEASURED OVER COPPER PLATING.
12. SILKSCREEN TOP AND BOTTOM SIDES USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON GOLD AREAS, ON PADS OR IN HOLES.
13. ROUTE BOARD OUTLINE, PER DRAWING DIMENSIONS. PANELIZE INTO AN 11x8 INCH ARRAY, PROJECTED (5x6=) 30 MODULES PER ARRAY (0.4" SIDE BORDERS)
14. DO NOT BREAK MODULES OFF ARRAYS UNTIL AFTER ASSEMBLY.

15. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE AND ANY OTHER IDENTIFICATION MARKS ON TOP SIDE PANEL BORDER ETCH, NOT ON INDIVIDUAL MODULES.
16. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
17. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC. MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
18. FINISHED BOARD MUST MEET UL94V-0 RATING AND RoHS COMPLIANCE.
19. DOCUMENTATION THAT MUST BE DELIVERED WITH BOARDS:
- 19A. CROSS SECTION REPORT (SPACING BETWEEN COPPER LAYERS AND COPPER THICKNESS)
- 19B. ELECTRICAL TEST CERTIFICATION OF COMPLIANCE (ACCORDANCE WITH IPC-ET-652 CLASS II)
- 19C. CERTIFICATION OF COMPLIANCE (BOARD HAS BEEN MANUFACTURED TO DRAWING REQUIREMENTS)
- 19D. RoHS CERTIFICATE OF COMPLIANCE.
- 19E. IMPEDANCE REPORT (REQUIRED IMPEDANCE TRACES PER NOTE 20)
20. ALL TOP LAYER .025 TRACES (D-CODE D24) TO BE 50 OHM IMPEDANCE. TRACE WIDTH AND LAYER SPACING MAY BE CHANGED TO ACCOMMODATE FABRICATION PROCESS BUT PRIOR APPROVAL IS REQUIRED BEFORE TRACE WIDTH OR LAYER SPACING CHANGES ARE MADE.


REVISIONS			
REV	DESCRIPTION	DATE	APPD
A	Etch 002 Production Release	05/02/07	

DETAIL A  
LAYER STACKUP  
SCALE: NONE

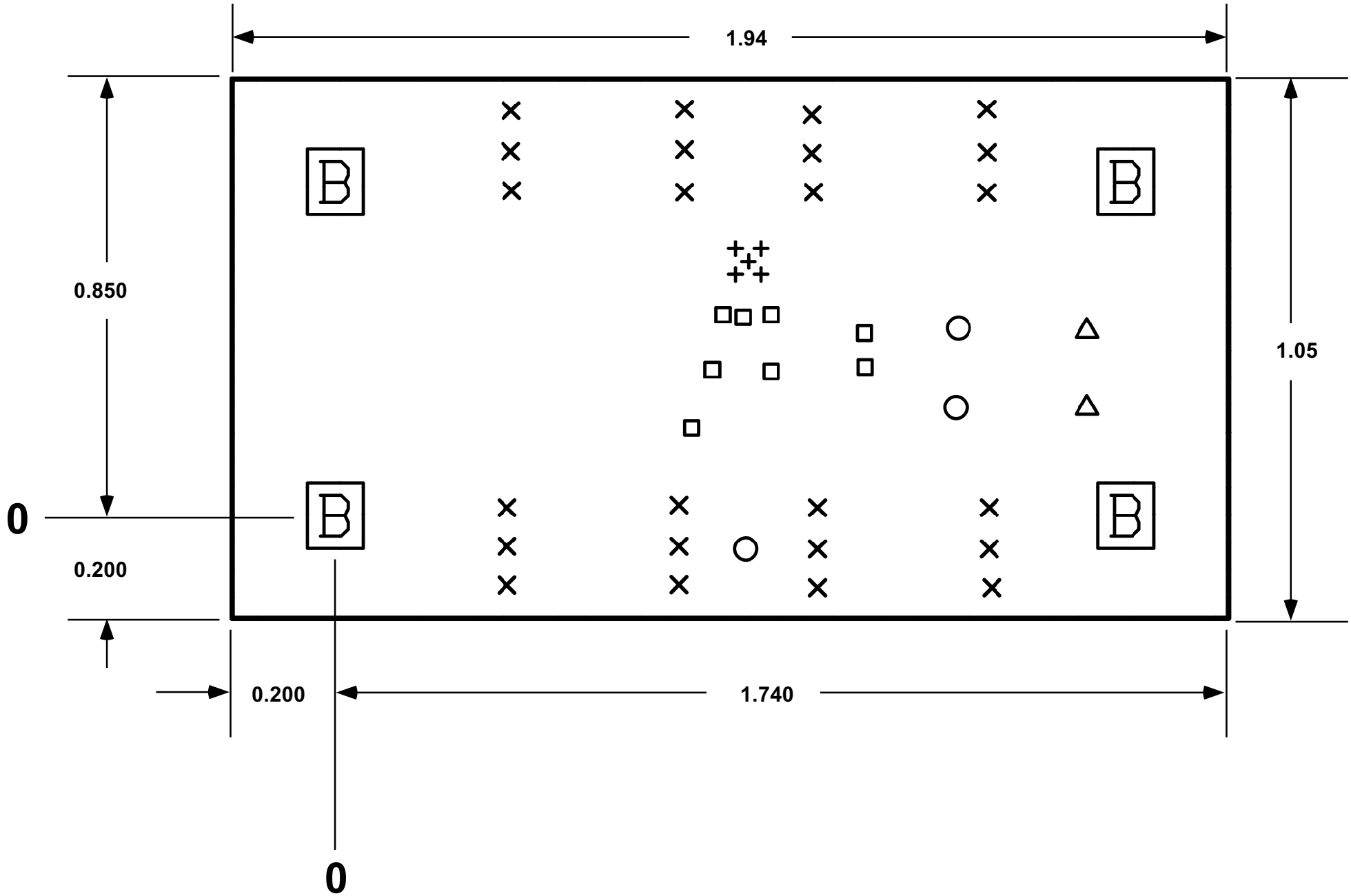


Board Fabrication Information	
	Smallest Feature
Air Gap	.007 inch
Trace Width	.010 inch
Hole Size	.008 inch
Pad Size	.25 x .60 mm
Surface Mount	Top & Bottom

UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES


MATERIAL: SEE NOTES			DRAWN: Ernesto Rey		DATE: 02-May-07		 National Semiconductor <sup>™</sup>			BOARD & SYSTEM BUSINESS OPERATIONS						
FINISH: SEE NOTES			CHECKED:		DATE:		PCB FABRICATION DRAWING LMH6555 SQA16A Eval									
TOLERANCES			ENGINEER:		DATE:											
1 PL	2 PL	3 PL	Hooman Hashemi													
± .02	± .01	± .005	DO NOT COPY, DISPLAY, OR USE DRAWING WITHOUT AUTHORIZATION DO NOT SCALE DRAWING						B		DRAWING: 551012941-002		A			
									SCALE:		NONE		SHEET 1 OF 2		REV	

REVISIONS
SEE SHEET #1



DRILL CHART			
ALL UNITS ARE IN INCHES			
SYM	SIZE	PLATED	QTY
+	0.008	YES	5
□	0.010	YES	8
△	0.015	YES	2
×	0.016	YES	24
○	0.040	YES	3
B	0.120	NO	4

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DO NOT SCALE DRAWING

 <b>National</b> <i>Semiconductor</i>		<b>BOARD &amp; SYSTEM BUSINESS OPERATIONS</b>	
<b>PCB FABRICATION DRAWING LMH6555 SQA16A Eval</b>			
<b>B</b>	<b>DRAWING:</b>	<b>551012941-002</b>	<b>A</b>
<b>SCALE:</b>		<b>SHEET 2 OF 2</b>	<b>REV</b>
<b>NONE</b>			