深圳市盛弘电气有限公司

承　认　书

SPECIFICATION FOR APPROVAL

深圳市盛弘电气股份有限公司

2016-08-29

受控文件

产 品 名 称：运算放大器

产 品 品 牌：TI

物 料 编 码：A50050077

供 应商型号：TLV2171AID(R)

版　　本:A00

供应方确认（Approved）

拟制（Prepared By）	
审核（Audit）	
批准（Approval）	

使用方确认（Approved）

项目审核（Project Audit）	
安规审核（Safety Audit）	
批准（Approval）	2016.08.29 14:47:50 +08'00'

版本	更改内容	更改人	更改日期	版本	更改内容	更改人	更改日期

表格编号：SZSH-QR-PD-017

TEXAS INSTRUMENTS

TLV171, TLV2171, TLV4171

–JULY 2016

TLVx171 36-V, Single-Supply, SOT553, General-Purpose Operational Amplifiers

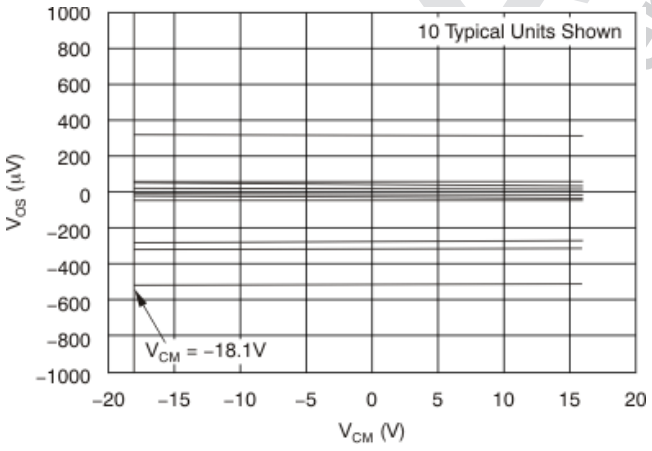
1 Features

- Supply Range: 2.7 to 36 V, ±1.35 V to ±18 V
- Low Noise: 14 nV/√Hz
- Low Offset Drift: ±0.3 µV/°C (Typical)
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 475 µA per Amplifier
- High Common-Mode Rejection: 120 dB (Typical)
- Low-Input Bias Current: 8 pA
- Industry-Standard Packages:
  - 5-Pin SOT
  - 8-Pin SOIC
  - 8-Pin MSOP
  - 14-Pin TSSOP

2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

Offset Voltage vs Common-Mode Voltage



3 Description

The TLV171, TLV2171, and TLV4171 (TLVx171) are a family of 36-V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most operational amplifiers, which are specified at only one supply voltage, the TLVx171 family is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The TLVx171 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. These devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

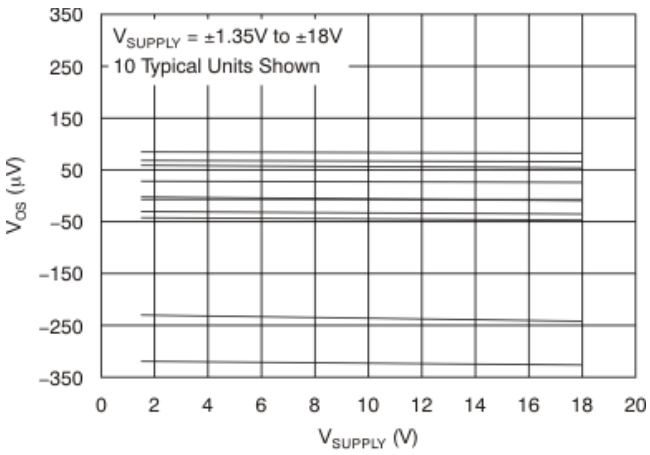
The TLVx171 series of operational amplifiers are specified from –40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV171	SOT23 (5)	1.60 mm × 2.90 mm
TLV2171	SOIC (8)	3.90 mm × 4.90 mm
TLV4171	TSSOP (14)	4.40 mm × 5.00 mm
	SOIC (14)	3.90 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Offset Voltage vs Power Supply



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

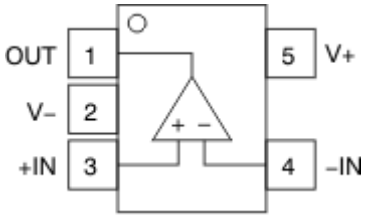
5 Device Comparison Table (1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV171	SOT23-5	DBV	OSUI	TLV171AIDBVT	Tape and Reel, 250
				TLV171AIDBVR	Tape and Reel, 3000
	SO-8	D	O171A	TLV171AID	Rail, 75
				TLV171AIDR	Tape and Reel, 2500
TLV2171	MSOP-8	DGK	OPMI	TLV2171AIDGK	Rail, 80
				TLV2171AIDGKR	Tape and Reel, 2500
	SO-8	D	2171A	TLV2171AID	Rail, 75
				TLV2171AIDR	Tape and Reel, 2500
TLV4171	SO-14	D	TLV4171	TLV4171AID	Rail, 50
				TLV4171AIDR	Tape and Reel, 2500
	TSSOP-14	PW	TLV4171	TLV4171AIPW	Rail, 90
				TLV4171AIPWR	Tape and Reel, 2000

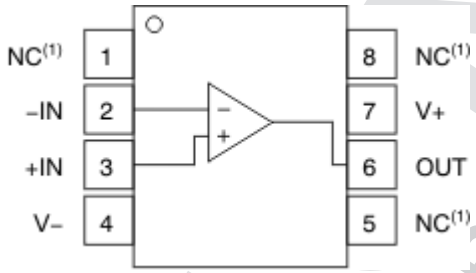
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

6 Pin Configuration and Functions

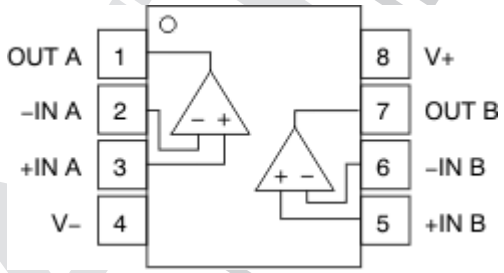
DBV Package: TLV171
SOT23-5
Top View



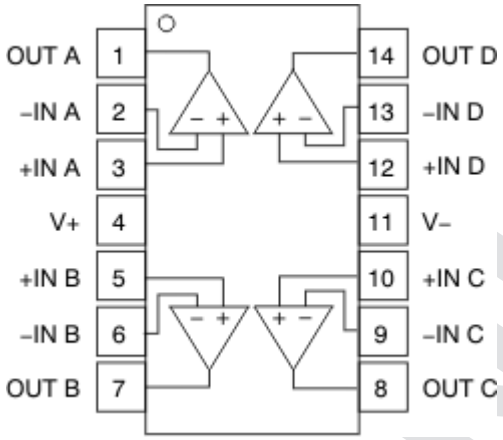
D PACKAGE: TLV171
SO-8
Top View



D and DGK Packages: TLV2171
SO-8 and MSOP-8
Top View



D and PW Packages: TLV4171
SO-14 and TSSOP-14
Top View



(1) No internal connection.

Pin Functions: TLV171

PIN			I/O	DESCRIPTION
NAME	DBV	D		
+IN	3	3	I	Noninverting input
–IN	4	2	I	Inverting input
OUT	1	6	O	Output
V+	5	7	—	Positive (highest) supply
V–	2	4	—	Negative (lowest) supply
NC	—	1, 5, 8	—	No internal connection (can be left floating)

Pin Functions: TLV2171

PIN			I/O	DESCRIPTION
NAME	DGK	D		
+IN A	3	3	I	Noninverting input
+IN B	5	5	I	Noinverting input
–IN A	2	2	I	Inverting input
–IN B	6	6	O	Inverting input
OUT A	1	1	O	Output
OUT B	7	7	—	Output
V+	8	8	—	Positive (highest) supply
V–	4	4	—	Negative (lowest) supply

Pin Functions: TLV4171

PIN			I/O	DESCRIPTION
NAME	DCU	DGK		
+IN A	3	3	I	Noninverting input
+IN B	5	5	I	Noninverting input
+IN C	10	10	I	Noninverting input
+IN D	12	12	I	Noninverting input
–IN A	2	2	I	Inverting input
–IN B	6	6	I	Inverting input

Pin Functions: TLV4171 (continued)

PIN			I/O	DESCRIPTION
NAME	DCU	DGK		
–IN C	9	9	I	Inverting input
–IN D	13	13	I	Inverting input
OUT A	1	1	O	Output
OUT B	7	7	O	Output
OUT C	8	8	O	Output
OUT D	14	14	O	Output
V+	4	4	—	Positive (highest) supply
V–	11	11	—	Negative (lowest) supply

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted. (1)

		MIN	MAX	UNIT
Supply voltage		±20		V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current	–10	10	mA
Output short circuit (2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information: TLV171

THERMAL METRIC (1)		TLV171			UNIT
		D (SO)	DBV (SOT23)	DRL (SOT553)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information: TLV2171

THERMAL METRIC (1)		TLV2171			UNIT
		D (SO)	DGK (MSOP)	DCU (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	195.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72.1	74.9	59.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	115.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	114.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information: TLV4171

THERMAL METRIC (1)		TLV4171		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.7 Electrical Characteristics

at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.75	±2.7	mV
Over temperature		T_A = –40°C to 125°C			±3.0	mV
Drift	dV_{OS}/dT	T_A = –40°C to 125°C		1		µV/°C
vs power supply	PSRR	V_S = 4 to 36 V, T_A = –40°C to 125°C	90	105		dB
INPUT BIAS CURRENT						
Input bias current	I_B			±10		pA
Input offset current	I_{OS}			±4		pA
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		3		μV_{PP}
Input voltage noise density	e_n	f = 100 Hz		25		$nV/\sqrt{Hz}$
		f = 1 kHz		18		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
Common-mode voltage range (1)	V_{CM}		(V–) – 0.1 V		(V+) – 2 V	V
Common-mode rejection ratio	CMRR	V_S = ±18V, (V–) – 0.1V < V_{CM} < (V+) – 2 V, T_A = –40°C to 125°C	94	105		dB
INPUT IMPEDANCE						
Differential				100 || 3		MΩ || pF
Common-mode				6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	V_S = 4 V to 36 V, (V–) + 0.35 V < V_O < (V+) – 0.35 V, T_A = –40°C to 125°C	94	130		dB
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/µs
Settling time	t_S	To 0.1%, V_S = ±18 V, G = +1, 10-V step		6		µs
		To 0.01% (12 bit), V_S = ±18V, G = +1, 10V step		10		µs
Overload recovery time		V_{IN} × Gain > V_S		2		µs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$		0.0002%		
OUTPUT						
Voltage output swing from rail	V_O	V_S = 5V, R_L = 10kΩ		30		mV
Over temperature		R_L = 10 kΩ, A_{OL} ≥ 110 dB, T_A = –40°C to 125°C	(V–) + 0.35		(V+) – 0.35	V
Short-circuit current	I_{SC}			+25/–35		mA
Capacitive load drive	C_{LOAD}			See *Typical Characteristics*		pF
Open-loop output resistance	R_O	f = 1MHz, I_O = 0A		150		Ω

(1) The input range can be extended beyond (V+) – 2V up to V+. See *Typical Characteristics* and *Application and Implementation* for additional information.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Specified voltage range	V_S		2.7		36	V
Quiescent current per amplifier	I_Q	I_O = 0 A, T_A = –40°C to 125°C		525	695	µA
TEMPERATURE						
Specified range			–40		125	°C
Operating range			–55		150	°C

7.8 Typical Characteristics

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 3
Input Bias Current vs Temperature	Figure 4
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 6
0.1-Hz to 10-Hz Noise	Figure 7
Input Voltage Noise Spectral Density vs Frequency	Figure 8
Quiescent Current vs Supply Voltage	Figure 9
Open-Loop Gain and Phase vs Frequency	Figure 10
Closed-Loop Gain vs Frequency	Figure 11
Open-Loop Output Impedance vs Frequency	Figure 12
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 13, Figure 14
No Phase Reversal	Figure 15
Small-Signal Step Response (100 mV)	Figure 16, Figure 17
Large-Signal Step Response	Figure 18, Figure 19
Large-Signal Settling Time (10-V Positive Step)	Figure 20
Large-Signal Settling Time (10-V Negative Step)	Figure 21
Short-Circuit Current vs Temperature	Figure 22
Maximum Output Voltage vs Frequency	Figure 23
Channel Separation vs Frequency	Figure 24

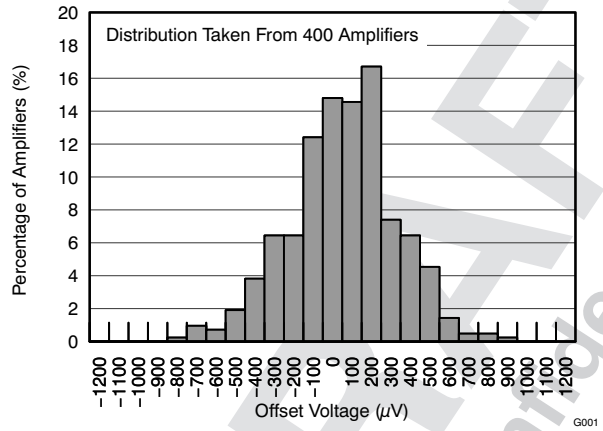


Figure 1. Offset Voltage Production Distribution

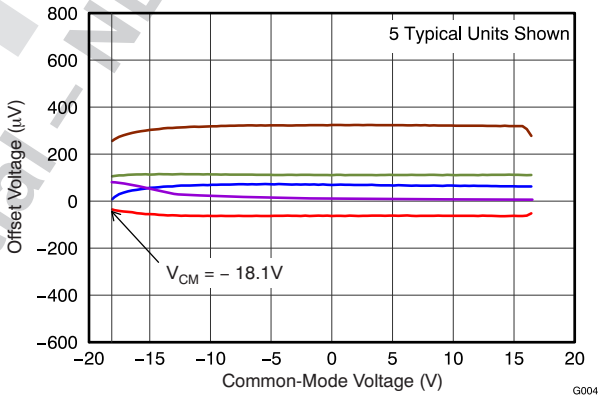


Figure 2. Offset Voltage vs Common-Mode Voltage

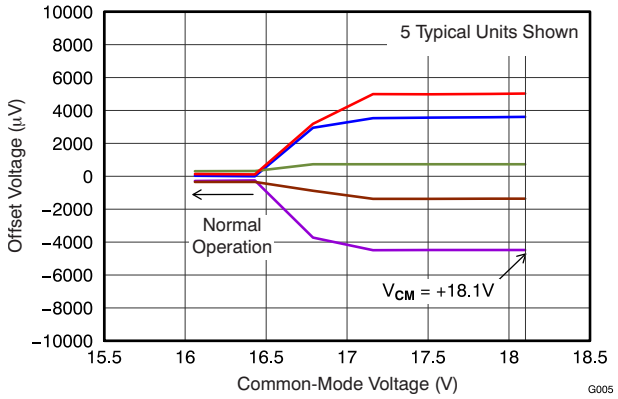


Figure 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

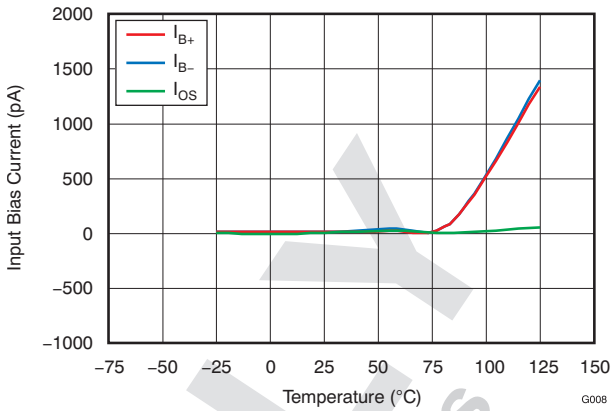


Figure 4. Input Bias Current vs Temperature

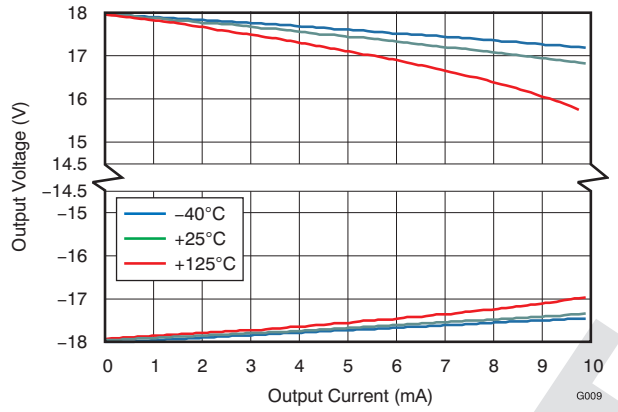


Figure 5. Output Voltage Swing vs Output Current (Maximum Supply)

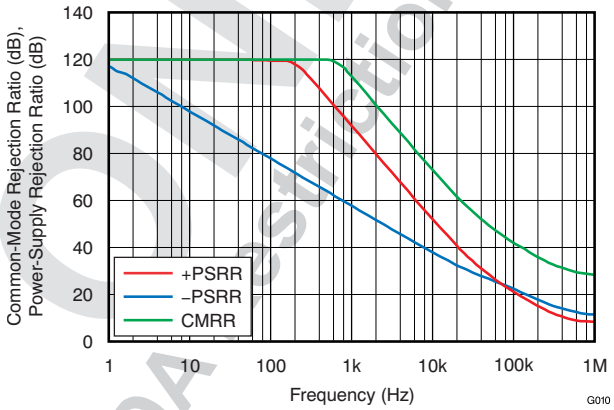


Figure 6. CMRR and PSRR vs Frequency (Referred-to Input)

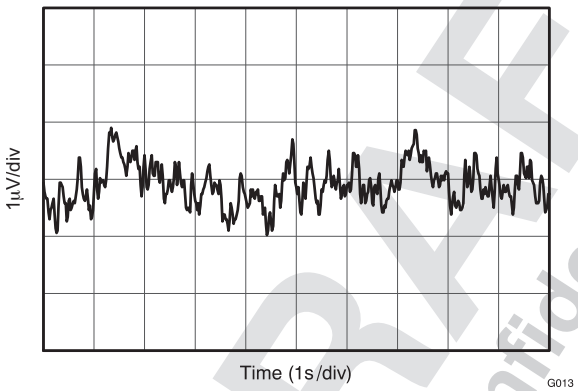


Figure 7. 0.1-Hz to 10-Hz Noise

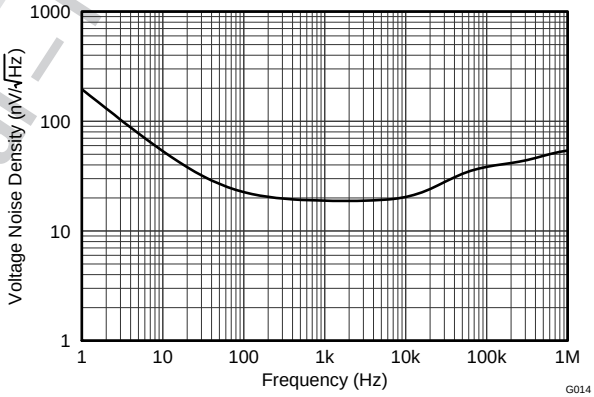


Figure 8. Input Voltage Noise Spectral Density vs Frequency

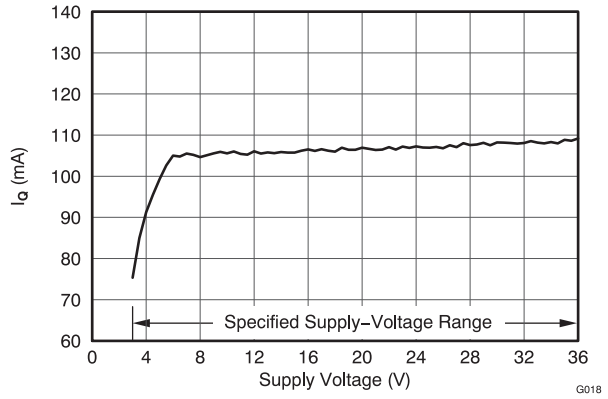


Figure 9. Quiescent Current vs Supply Voltage

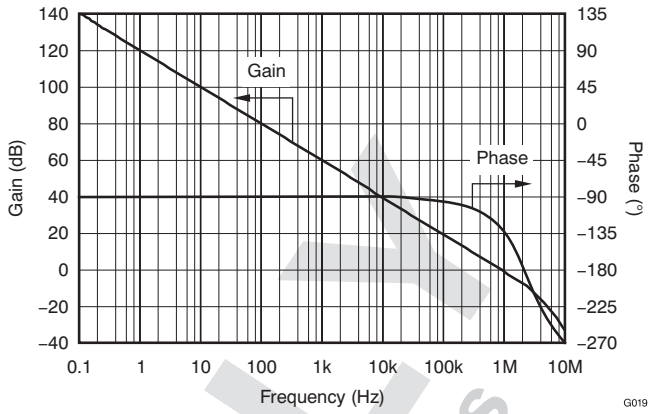


Figure 10. Open-Loop Gain and Phase vs Frequency

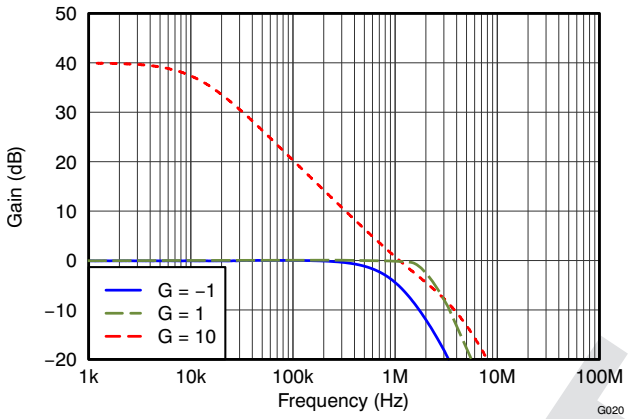


Figure 11. Closed-Loop Gain vs Frequency

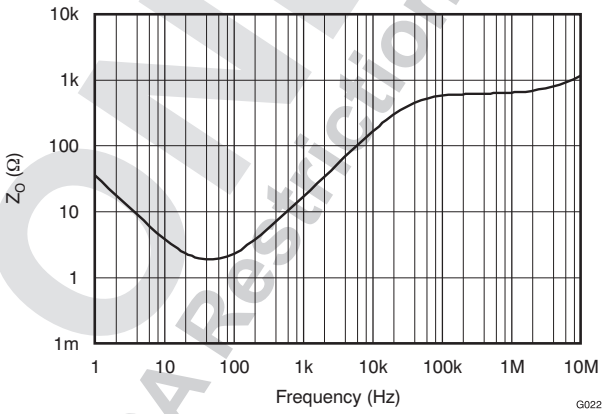


Figure 12. Open-Loop Output Impedance vs Frequency

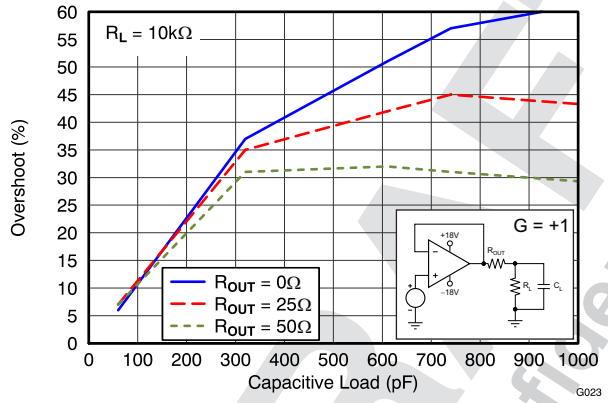


Figure 13. Small-Signal Overshoot vs Capacitive Load

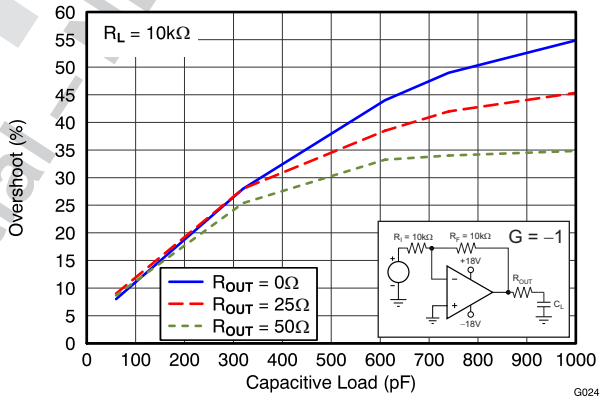


Figure 14. Small-Signal Overshoot vs Capacitive Load

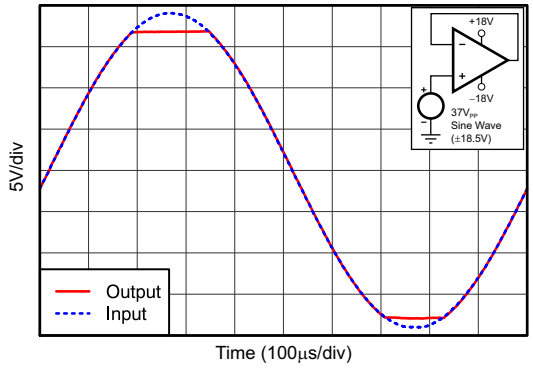


Figure 15. No Phase Reversal

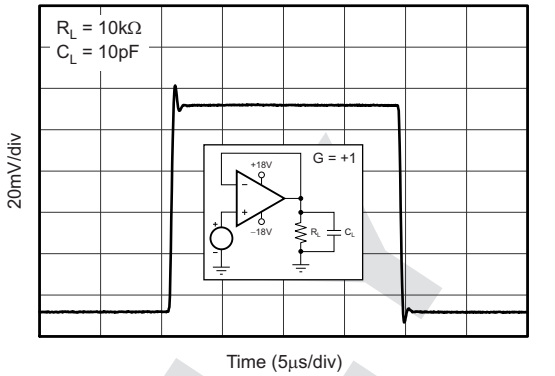


Figure 16. Small-Signal Step Response (100 mV)

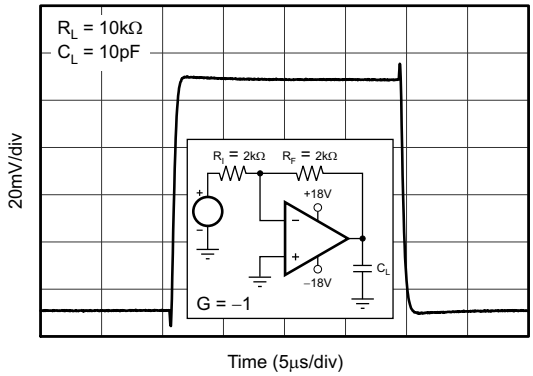


Figure 17. Small-Signal Step Response (100 mV)

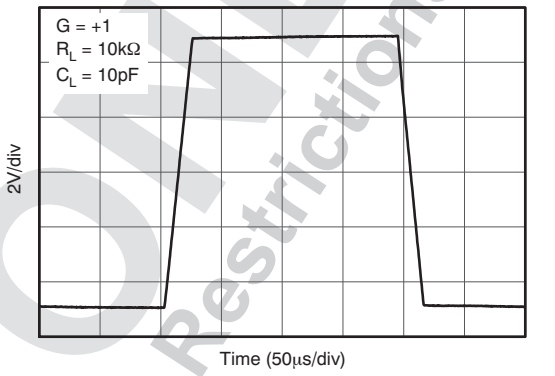


Figure 18. Large-Signal Step Response

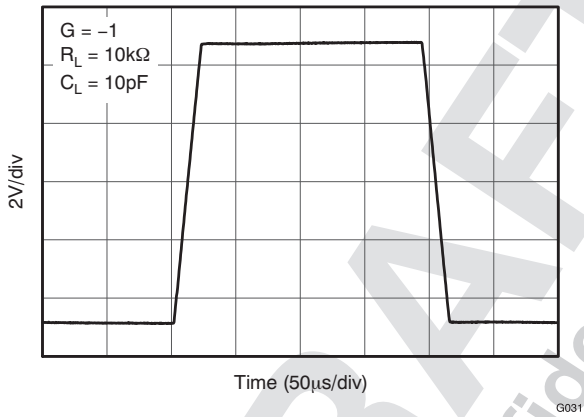
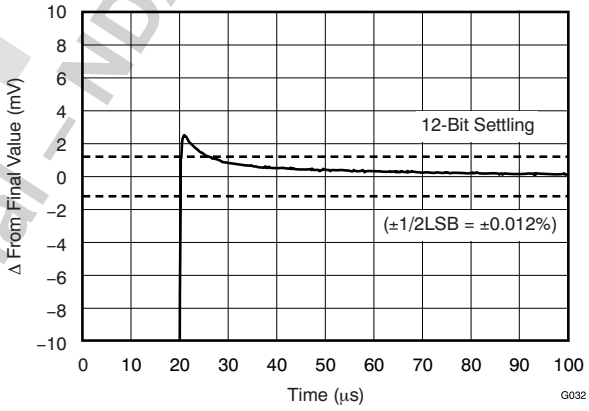
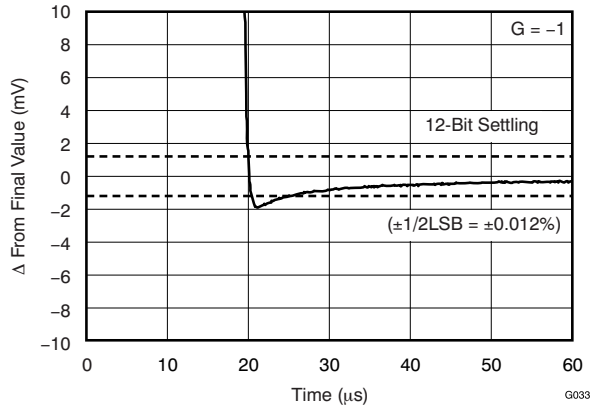


Figure 19. Large-Signal Step Response



10-V positive step

Figure 20. Large-Signal Settling Time



10-V negative step

Figure 21. Large-Signal Settling Time

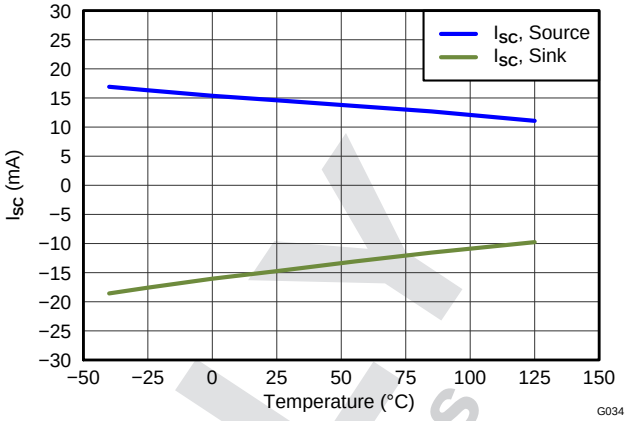


Figure 22. Short-Circuit Current vs Temperature

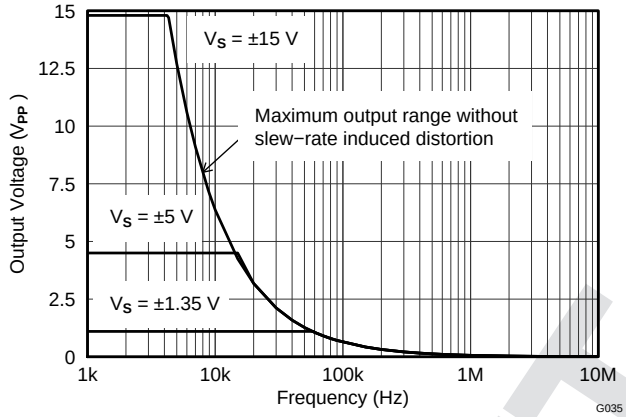


Figure 23. Maximum Output Voltage vs Frequency

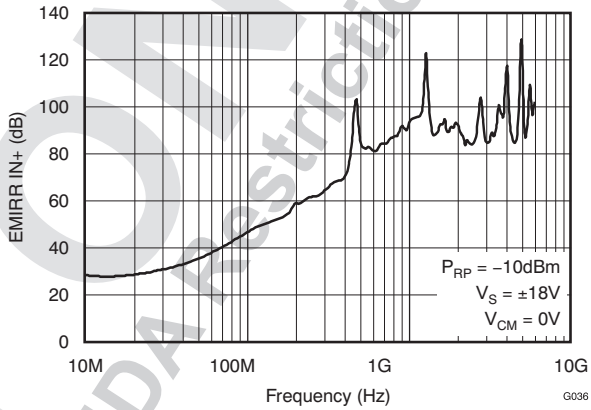


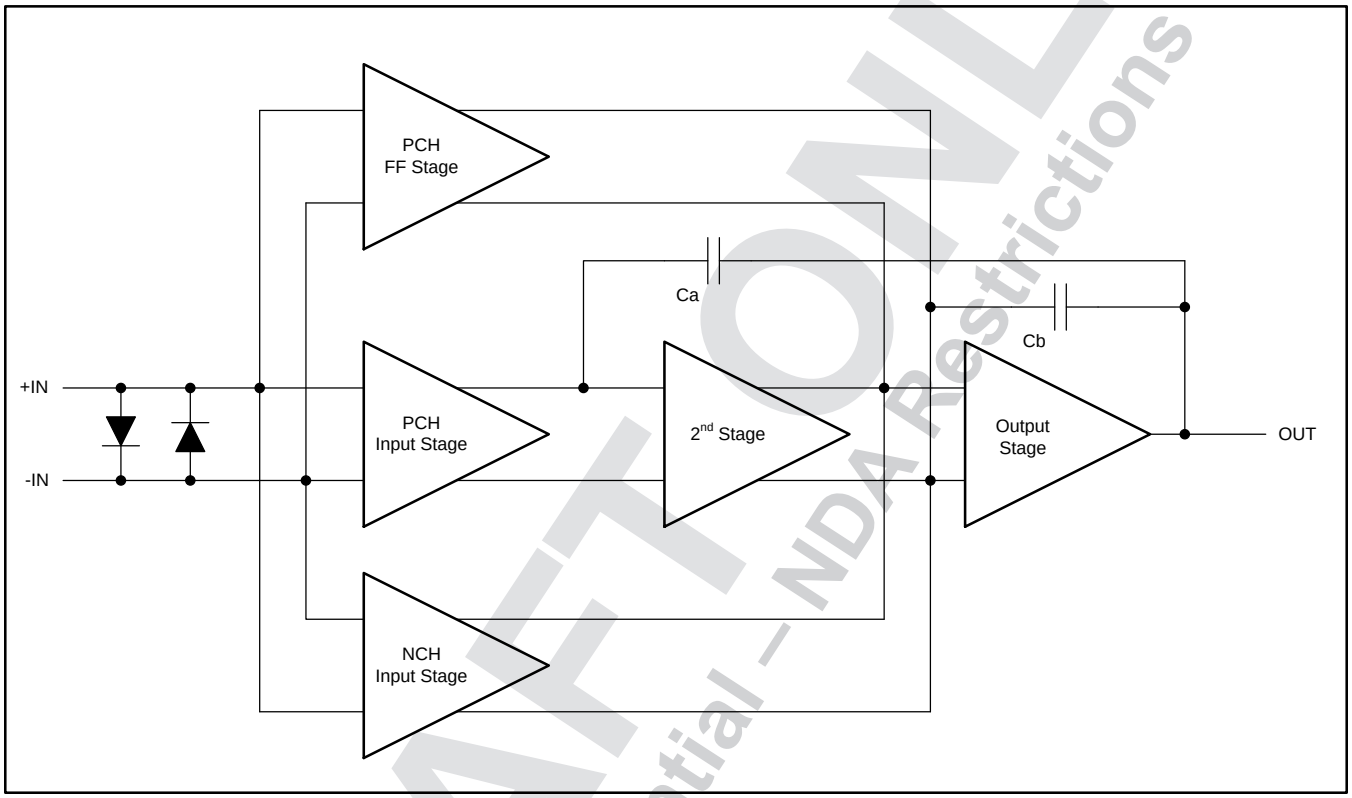
Figure 24. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The TLVx171 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The TLVx171 family of amplifiers is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics* .

8.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx171 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

Feature Description (continued)

8.3.3 Phase-Reversal Protection

The TLVx171 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 25.

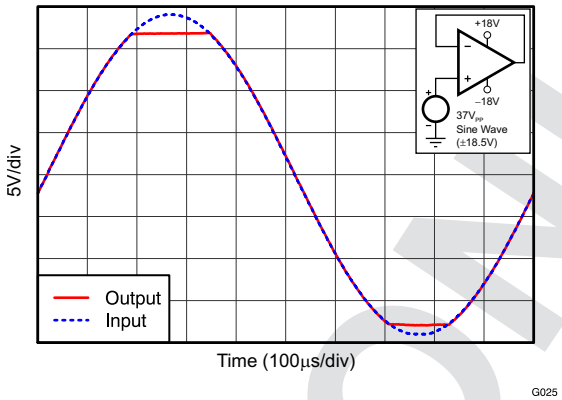


Figure 25. No Phase Reversal

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	**(V+) – 2**		**(V+) + 0.1**	**V**
Offset voltage		7		mV
vs Temperature		**12**		**µV/°C**
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/√Hz

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx171 family of devices have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 26 and Figure 27 show small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, for details of analysis techniques and application circuits, refer to the *Applications Bulletin AB-028* (SBOA015), available for download from TI.com.

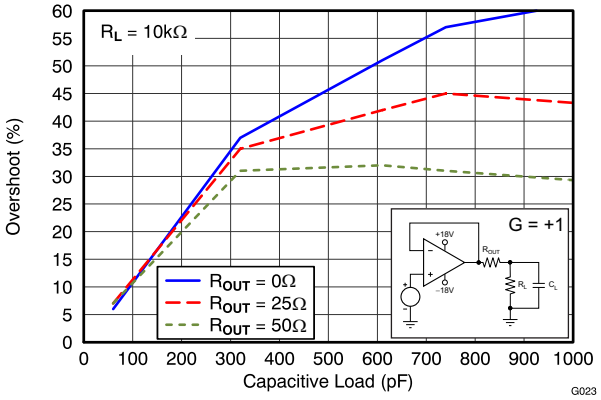


Figure 26. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

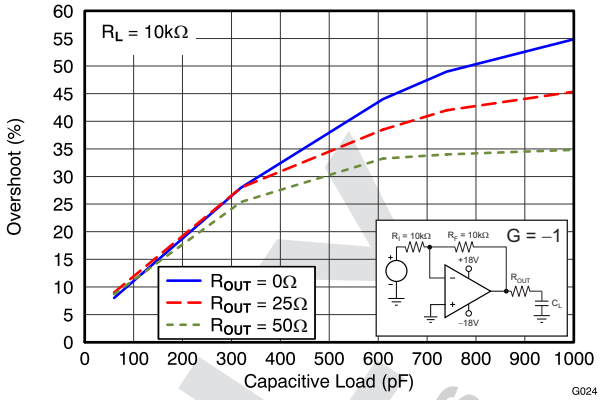


Figure 27. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx171 family of devices extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLVx171 operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very-good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

9.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins

or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the *Absolute Maximum Ratings* . Figure 28 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

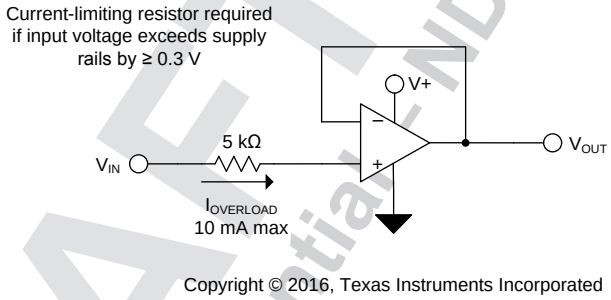


Figure 28. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

9.2 Typical Application

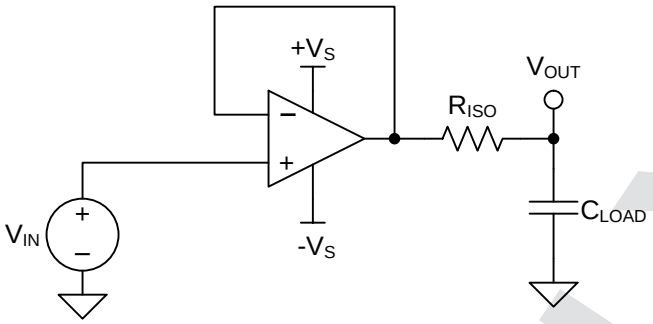


Figure 29. Unity-Gain Buffer With R_{ISO} Stability Compensation

9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

9.2.2 Detailed Design Procedure

Figure 30 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 30. Not shown in Figure 30 is the open-loop output resistance of the operational amplifier, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. Figure 30 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

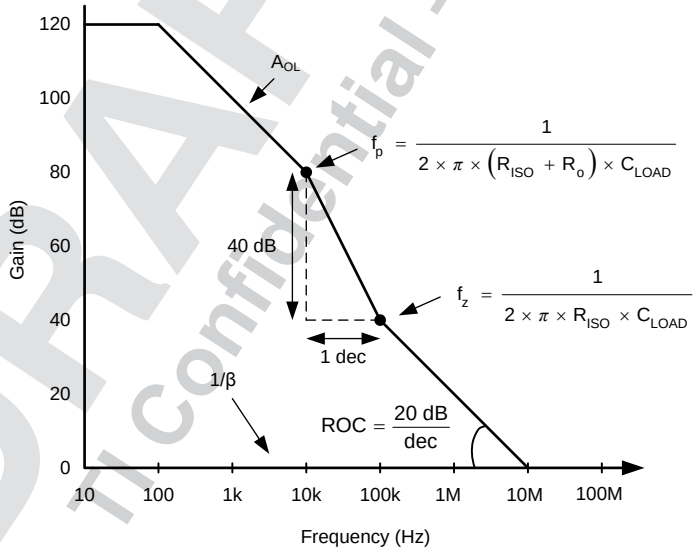


Figure 30. Unity-Gain Amplifier With R_{ISO} Compensation

Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.2.1 Capacitive Load and Stability

The dynamic characteristics of the TLVx171 have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 26 and Figure 27 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to *Applications Bulletin AB-028* (SBOA015), available for download from the TI website for details of analysis techniques and application circuits.

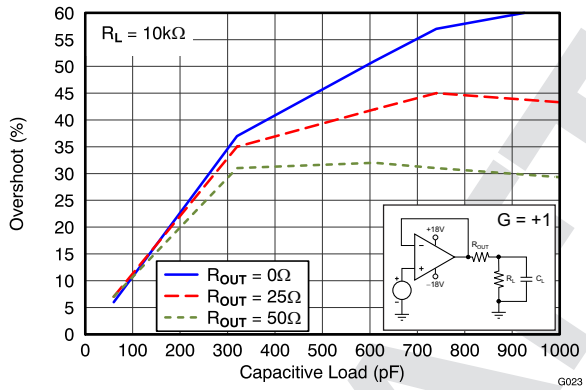


Figure 31. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

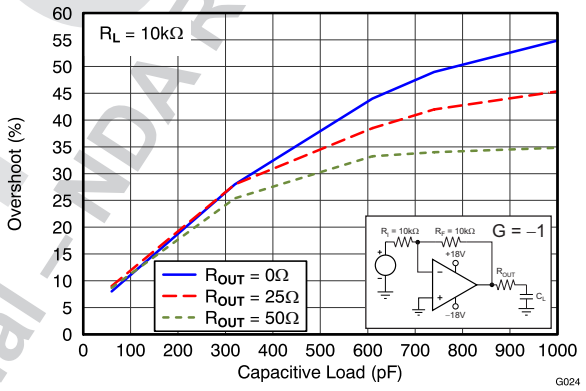


Figure 32. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

9.2.3 Application Curve

The TLV171 meets the supply voltage requirements of 30 V. The TLV171 is tested for various capacitive loads and RISO is adjusted to get an overshoot corresponding to Table 3. The results of the these tests are summarized in Figure 33.

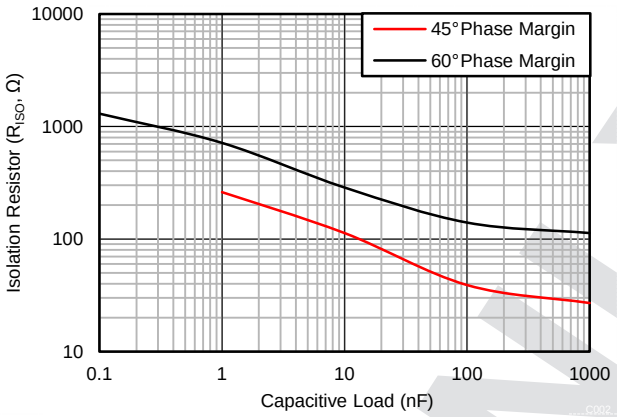


Figure 33. R_{ISO} vs C_{LOAD}

10 Power Supply Recommendations

The TLVx171 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Specifications* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, good printed--circuit board (PCB) layout practices are recommended. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

11.2 Layout Example

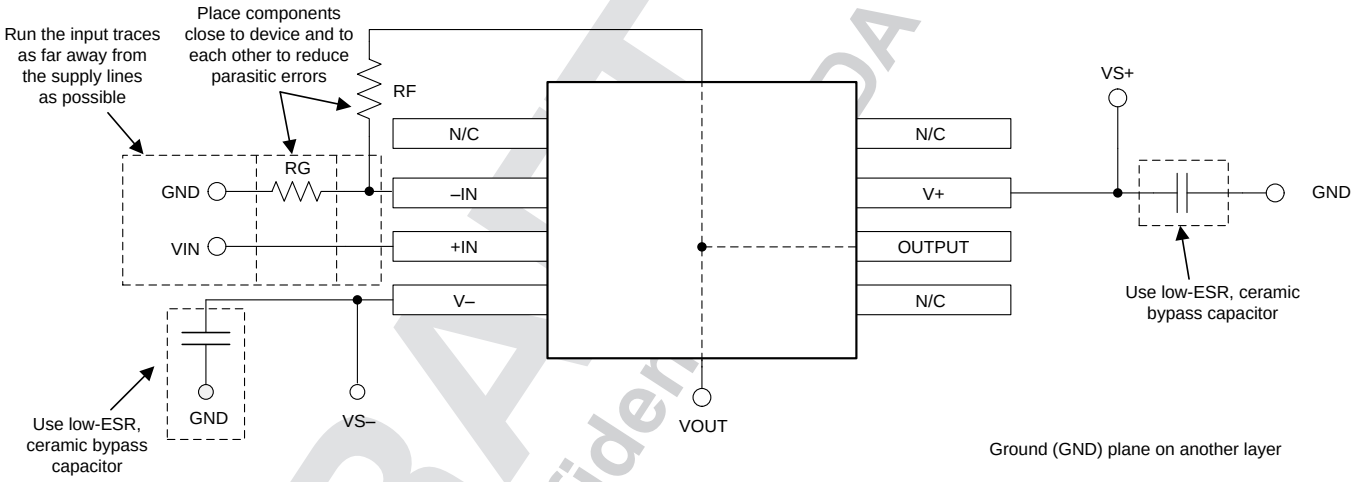


Figure 34. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV171	Click here	Click here	Click here	Click here	Click here
TLV2171	Click here	Click here	Click here	Click here	Click here
TLV4171	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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