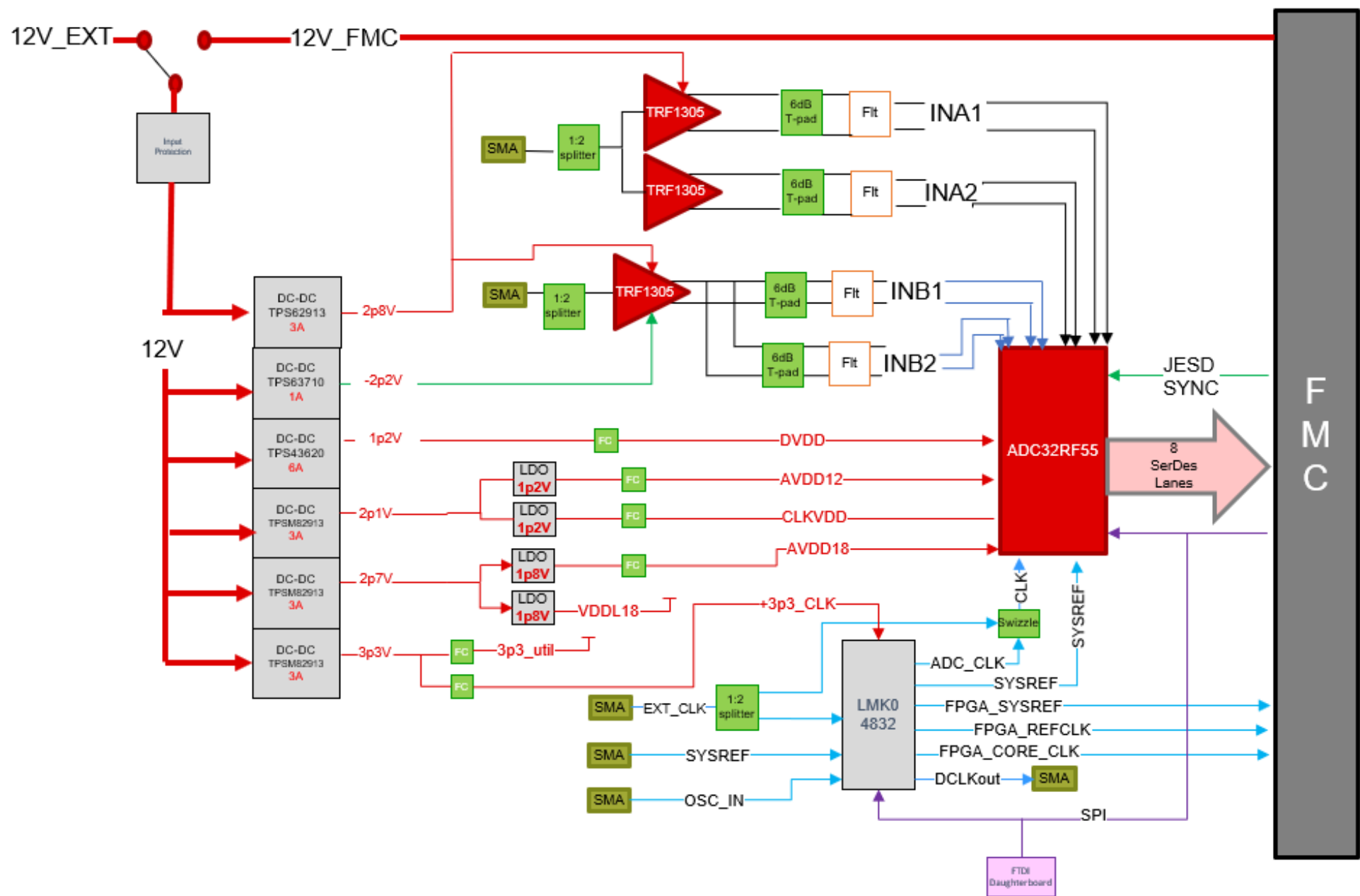
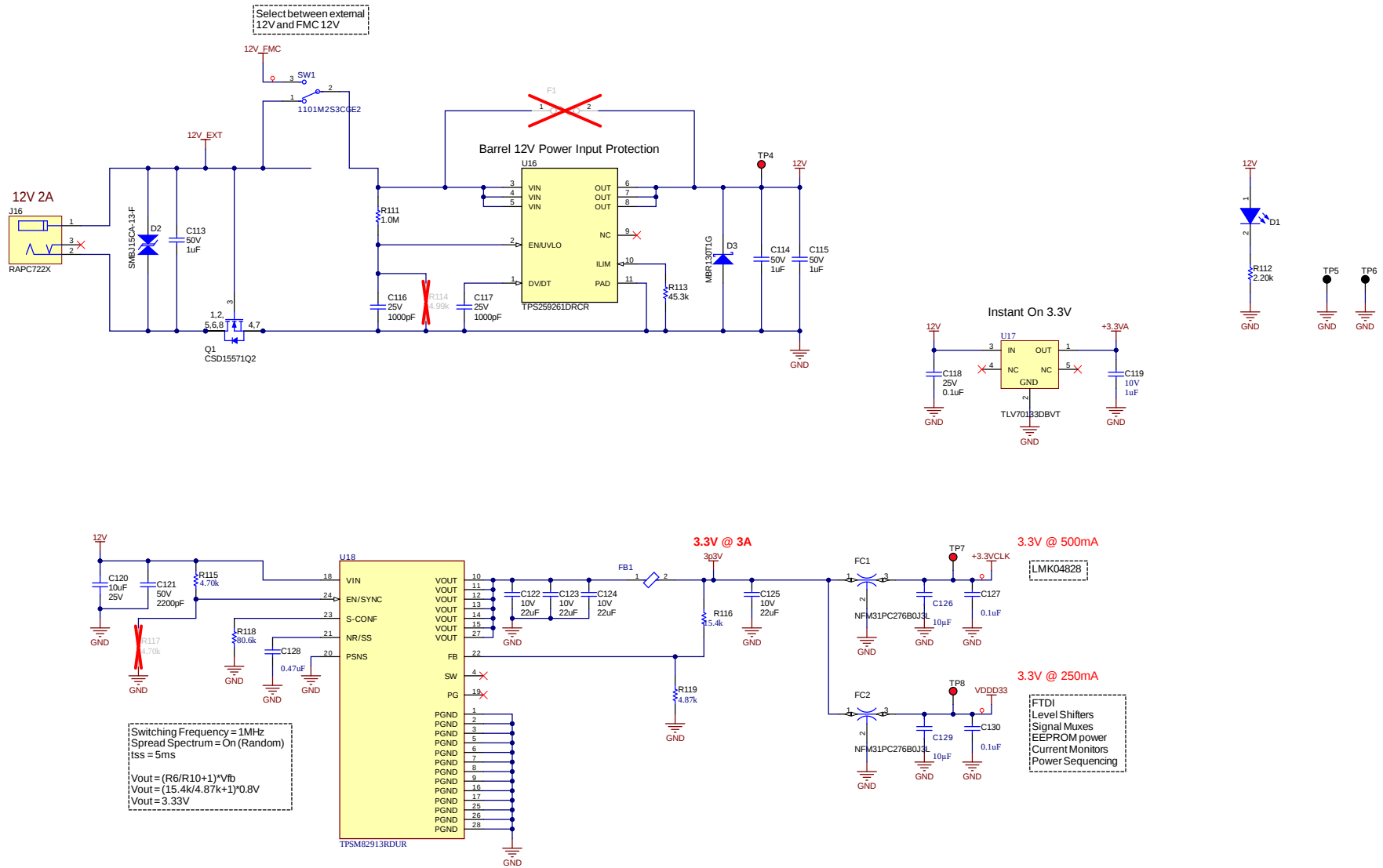




EVM Power 1

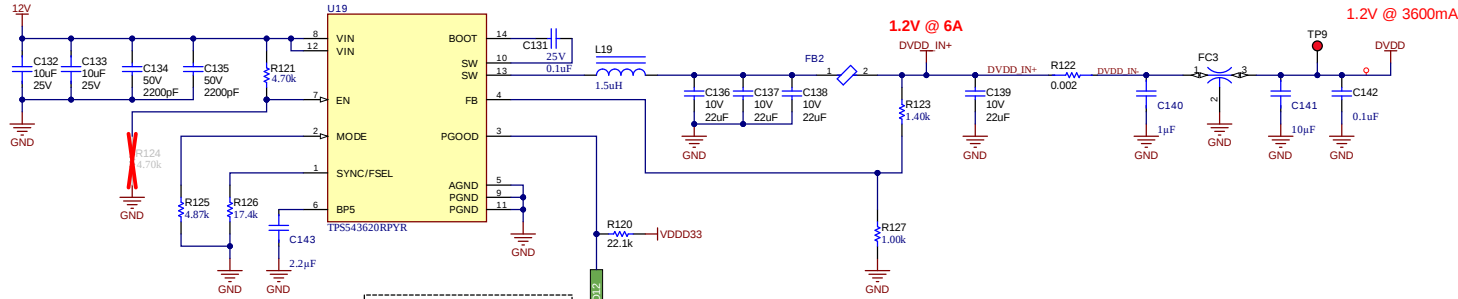


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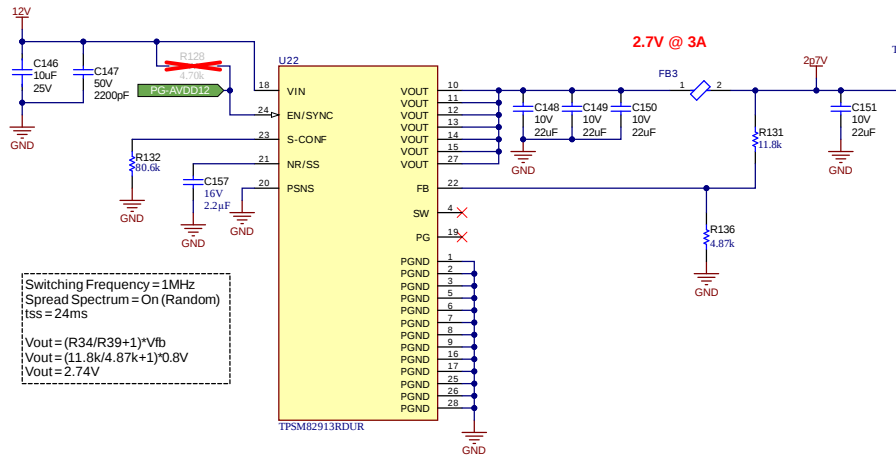
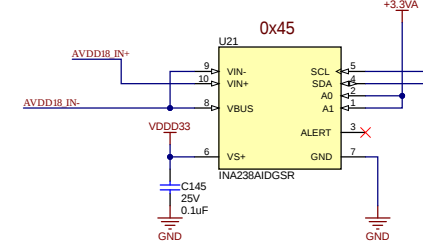
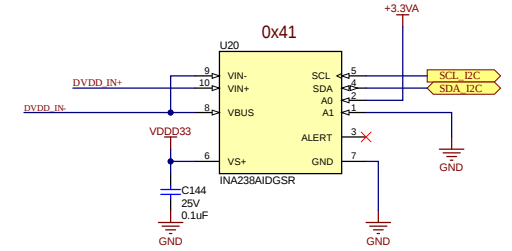
Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: EVM Power 1
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 2 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_Power1_RevA_SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	©Texas Instruments 2023



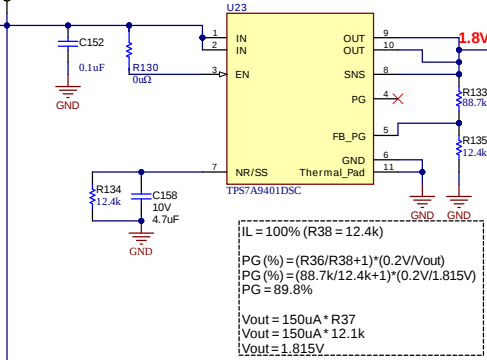
EVM Power 2



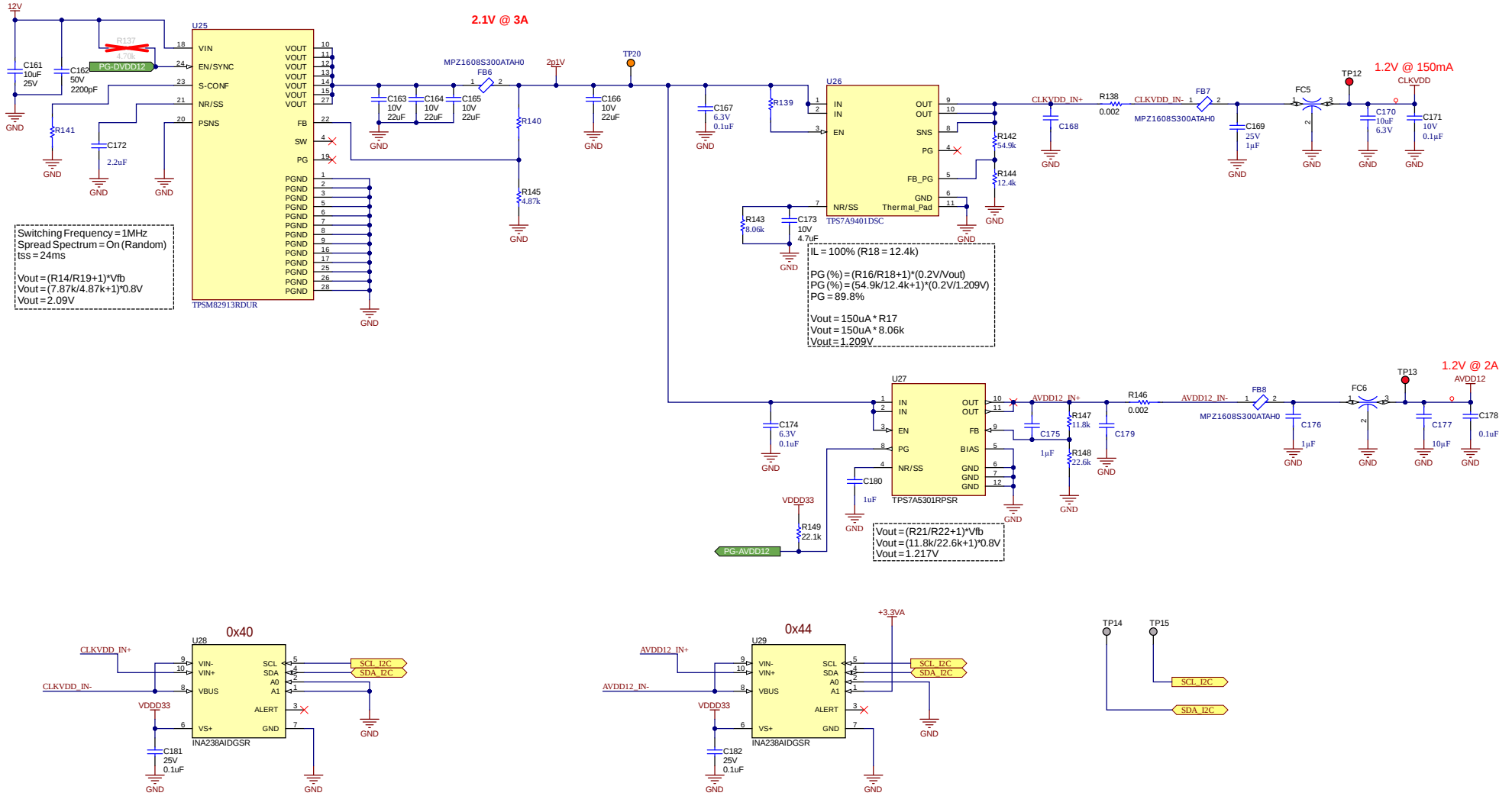
Switching Frequency = 750kHz
Current limit: High
tss = 1ms
 $V_{out} = (R27/R30+1) \cdot V_{fb}$
 $V_{out} = (1.4k/1k+1) \cdot 0.5V$
 $V_{out} = 1.21V$



Switching Frequency = 1MHz
Spread Spectrum = On (Random)
tss = 24ms
 $V_{out} = (R34/R39+1) \cdot V_{fb}$
 $V_{out} = (11.8k/4.87k+1) \cdot 0.8V$
 $V_{out} = 2.74V$



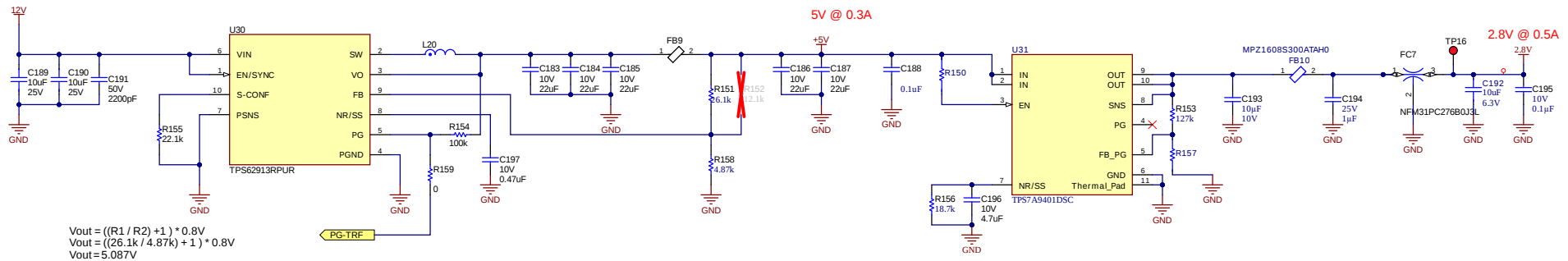
EVM Power 3



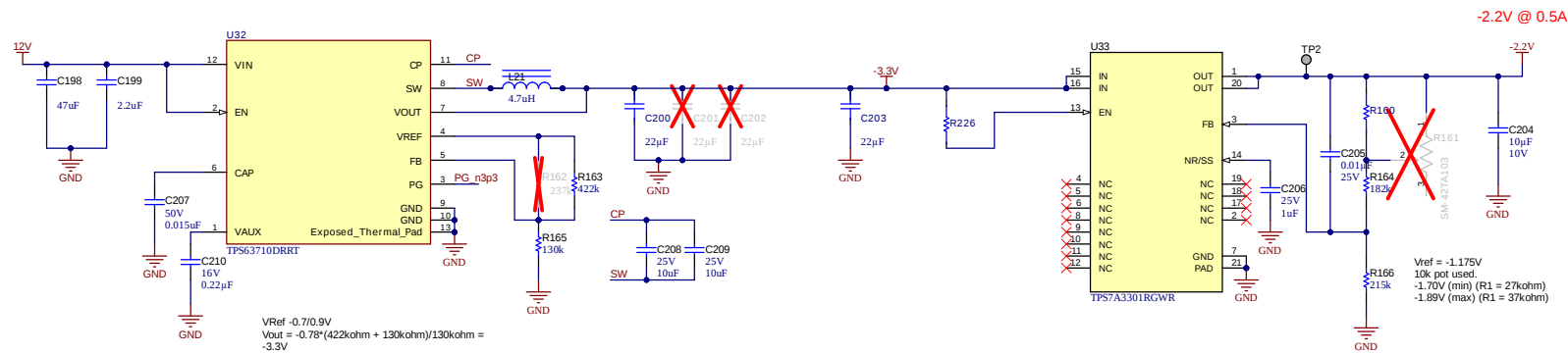
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Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: EVM Power 3
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 4 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_Power3_RevA_SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	

EVM Power 4



IL = 100% (R157 = 12.4k)

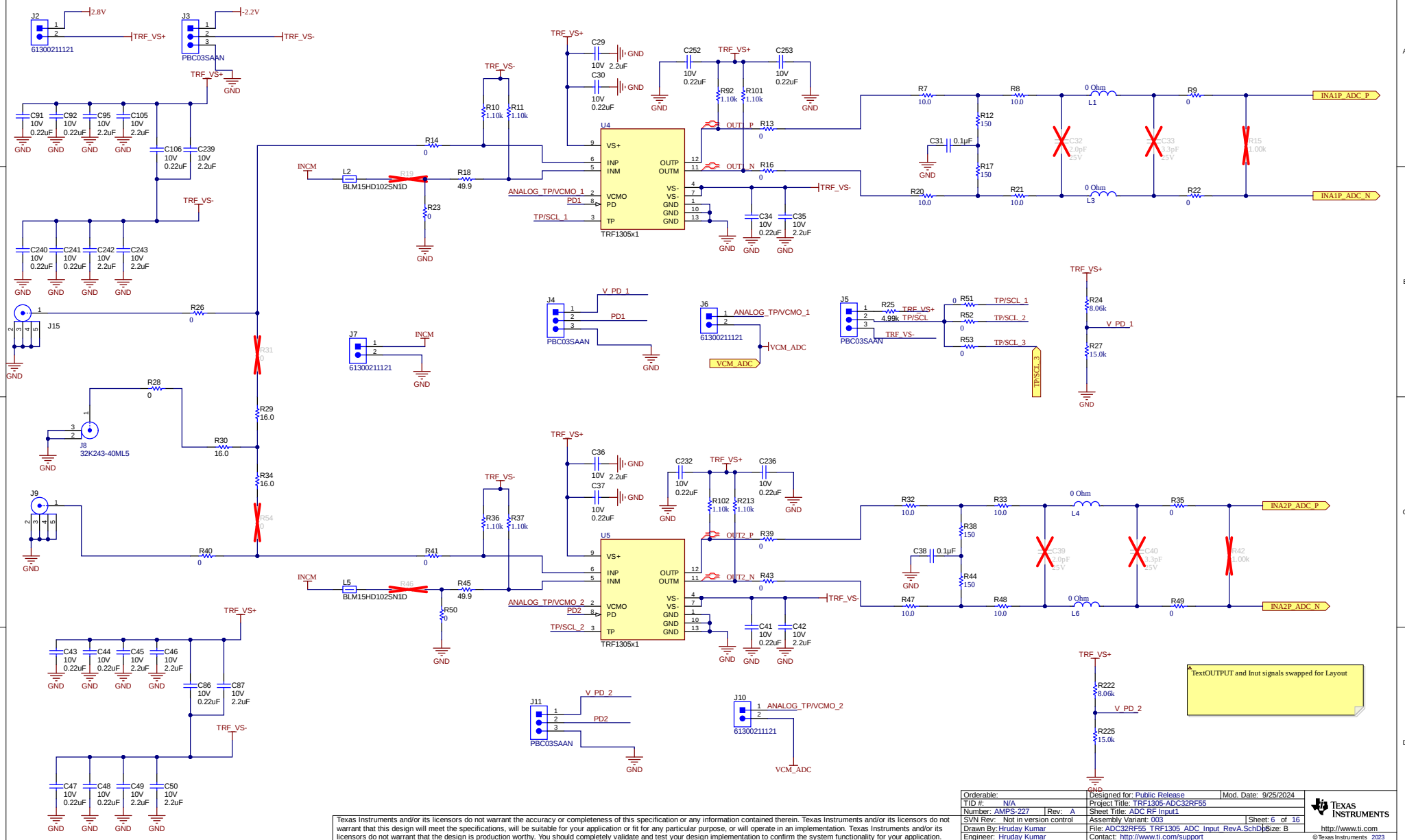
$$\begin{aligned} PG(\%) &= (R_{153}/R_{157}+1) \cdot (0.2V/V_{out}) \\ PG(\%) &= (127k/12.4k+1) \cdot (0.2V/2.80V) \\ PG &= 80\% \end{aligned}$$
$$\begin{aligned} V_{out} &= 150\mu A * R_{17} \\ V_{out} &= 150\mu A * 18.7K \\ V_{out} &= 2.805V \end{aligned}$$

$$V_{out} = -0.78 \cdot (422\text{k}\Omega + 130\text{k}\Omega) / 130\text{k}\Omega = -3.3\text{V}$$

Vref = -1.175V
10k pot used.
-1.70V (min) (R1 = 27kohm)
-1.89V (max) (R1 = 37kohm)

Orderable:		Designed for: <u>Public Release</u>		Mod. Date: 8/9/2024	
TID #: <u>N/A</u>		Project Title: <u>TRF1305-ADC32RF55</u>			
Num: <u>AMPS-227</u> Rev: <u>A</u>		Sheet Title: <u>EVMT Power 4</u>			
SVN Rev: <u>N/A</u> Not in version control		Assembly Variant: <u>003</u>		Sheet: <u>5</u> of <u>16</u>	
Drawn By: <u>Hruday Kumar</u>		File: <u>ADC32RF55-TRF1305_Power4_RevA_SchDoc</u>		Size: <u>B</u>	
Engineer: <u>Hruday Kumar</u>		Contact: <u>http://www.ti.com/support</u>		http://www.ti.com  © Texas Instruments 2023	

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ADC RF Input1

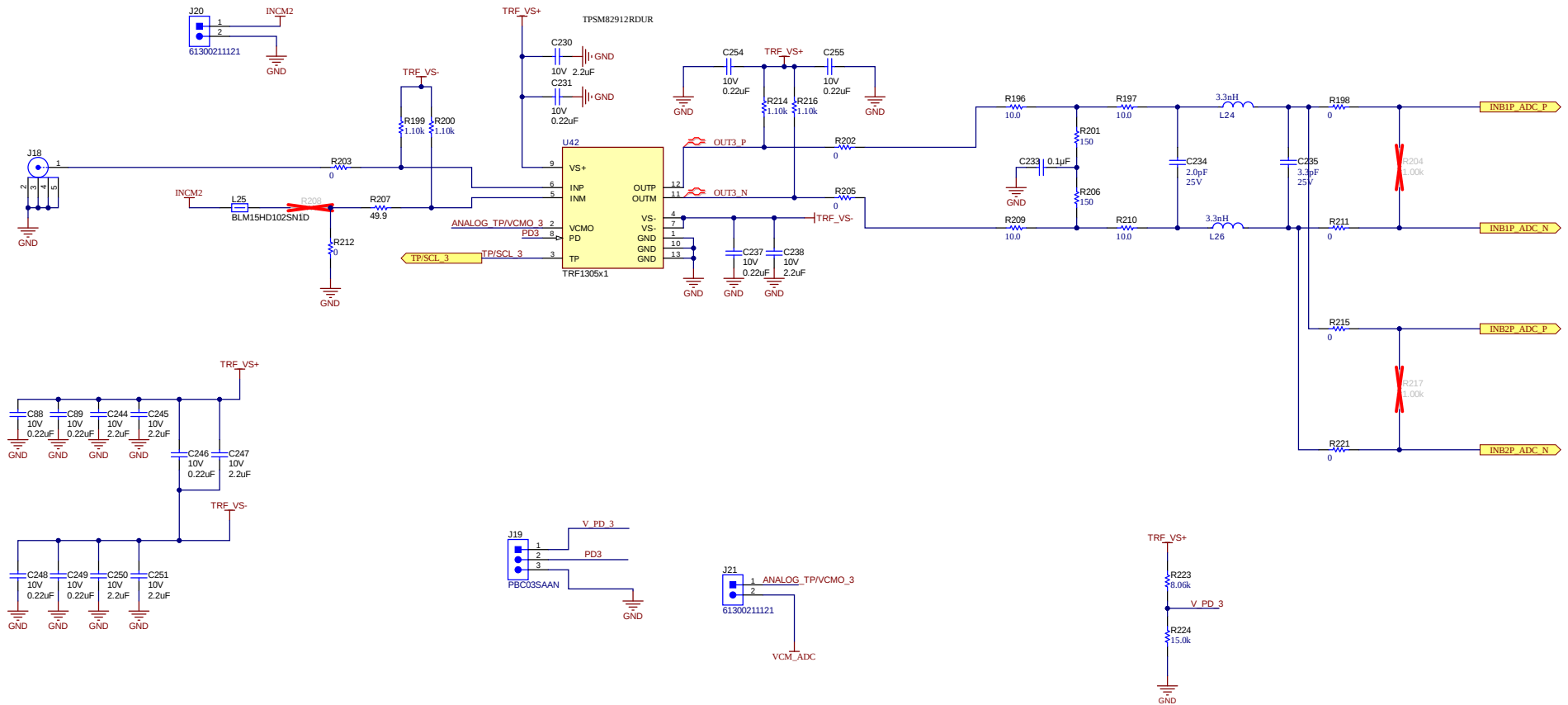


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Orderable:	Designed for: Public Release	Mod. Date: 9/25/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: ADC RF Input1
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 6 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_ADC_Input_RevA_SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	



ADC RF Input2



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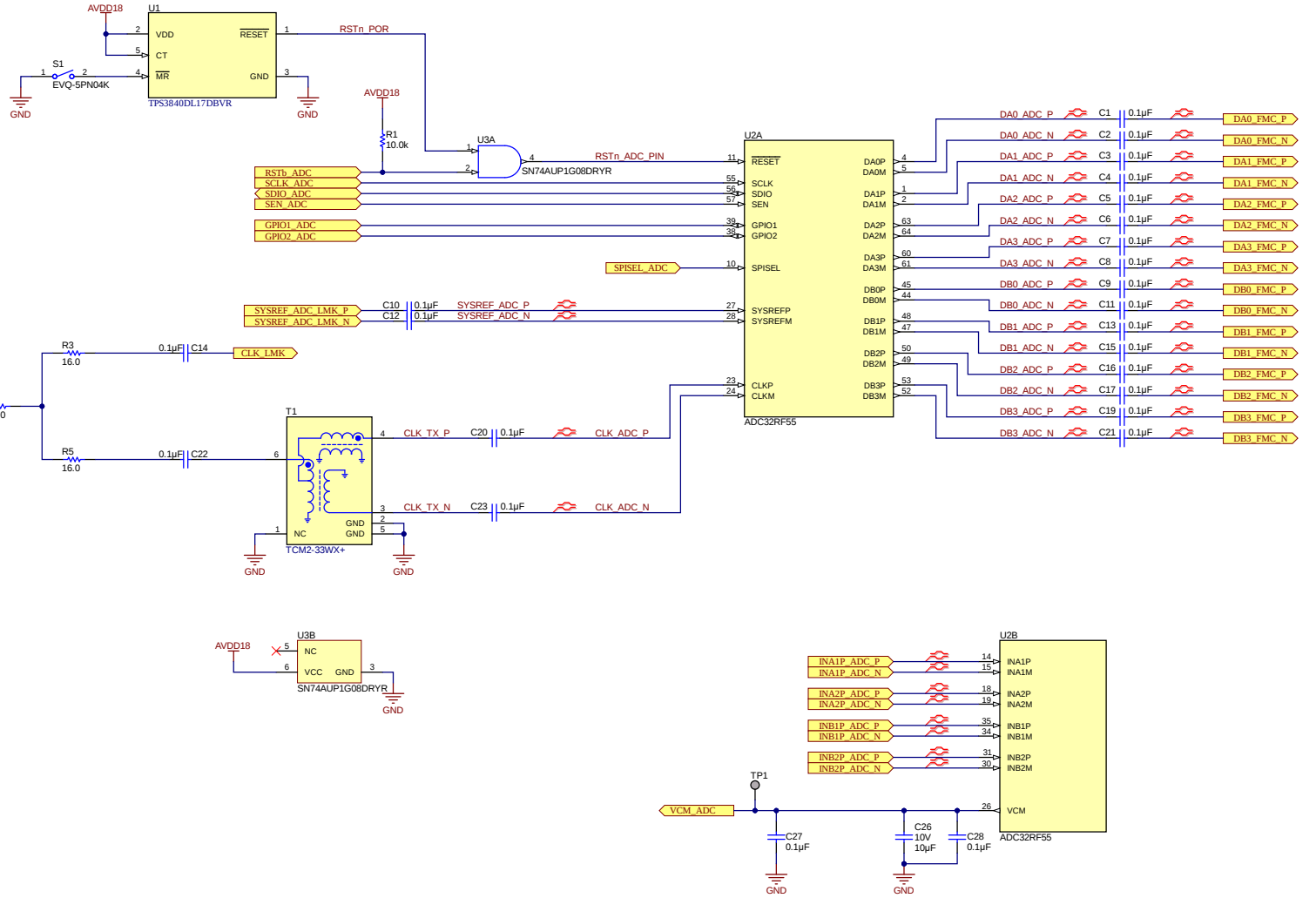
Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: ADC RF Input2
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 7 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_ADC_Input2_RevA_Sch	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	



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ADC Input, SERDES and Digital Pins

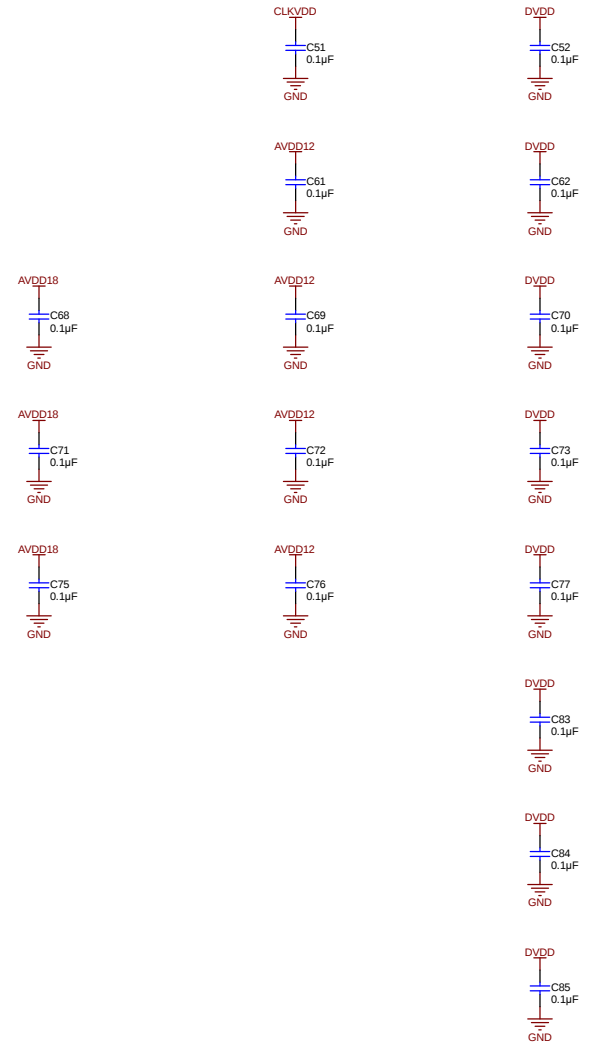
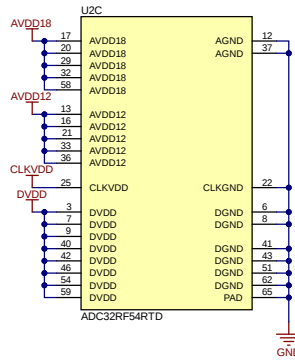
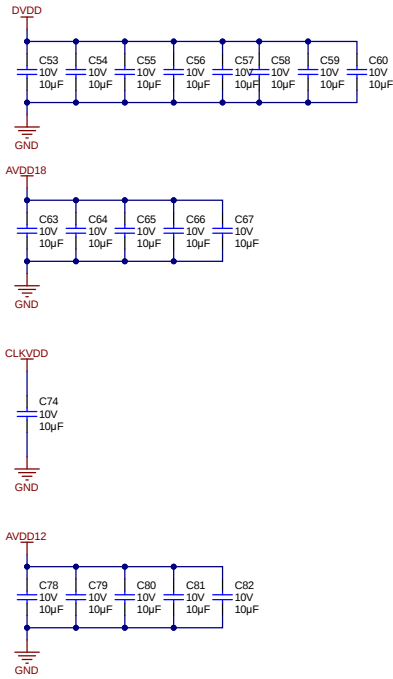
EXTCLK



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Orderable:	Designed for: Public Release	Mod. Date: 8/23/2024
TID #:	Project Title: TRF1305-ADC32RF55	
Number: AMPS-227	Rev: A	Sheet Title: ADC Input, SERDES and Digital Pins
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 8 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_ADC_Dig_RevA.SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	

ADC Power



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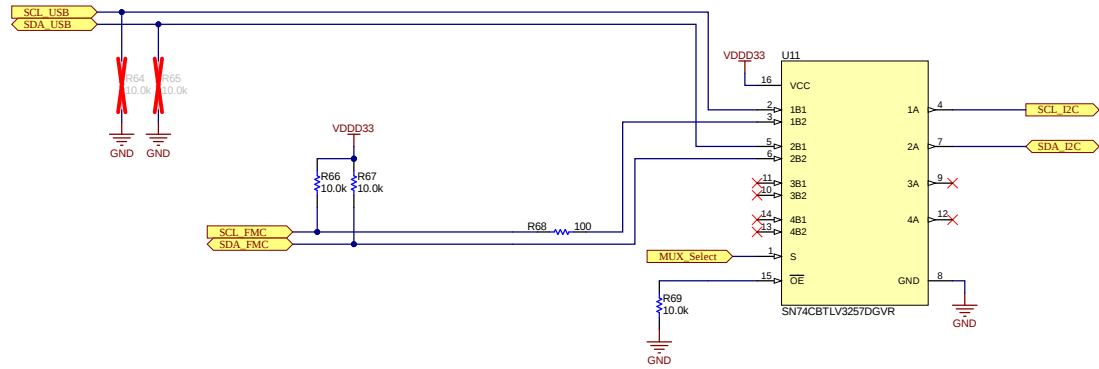
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TID #:	Project Title: TRF1305-ADC32RF55	
Number: AMPS-227	Rev: A	Sheet Title: ADC Power
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 9 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_ADC_Power_RevA.Sch	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	



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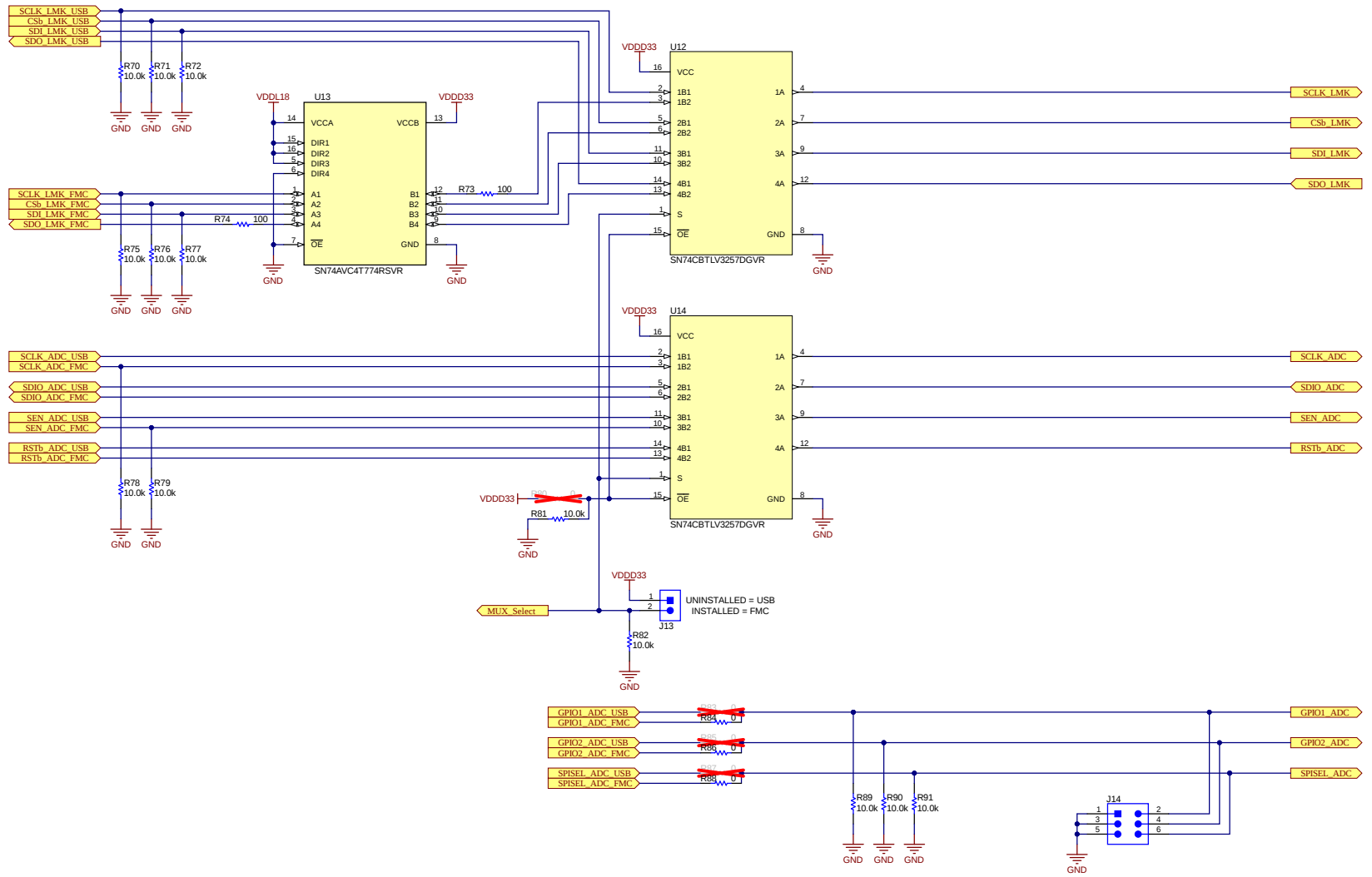
GPIO MUX



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Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: GPIO MUX
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 11 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_GPIO_MUX_RevA_Sch01	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	

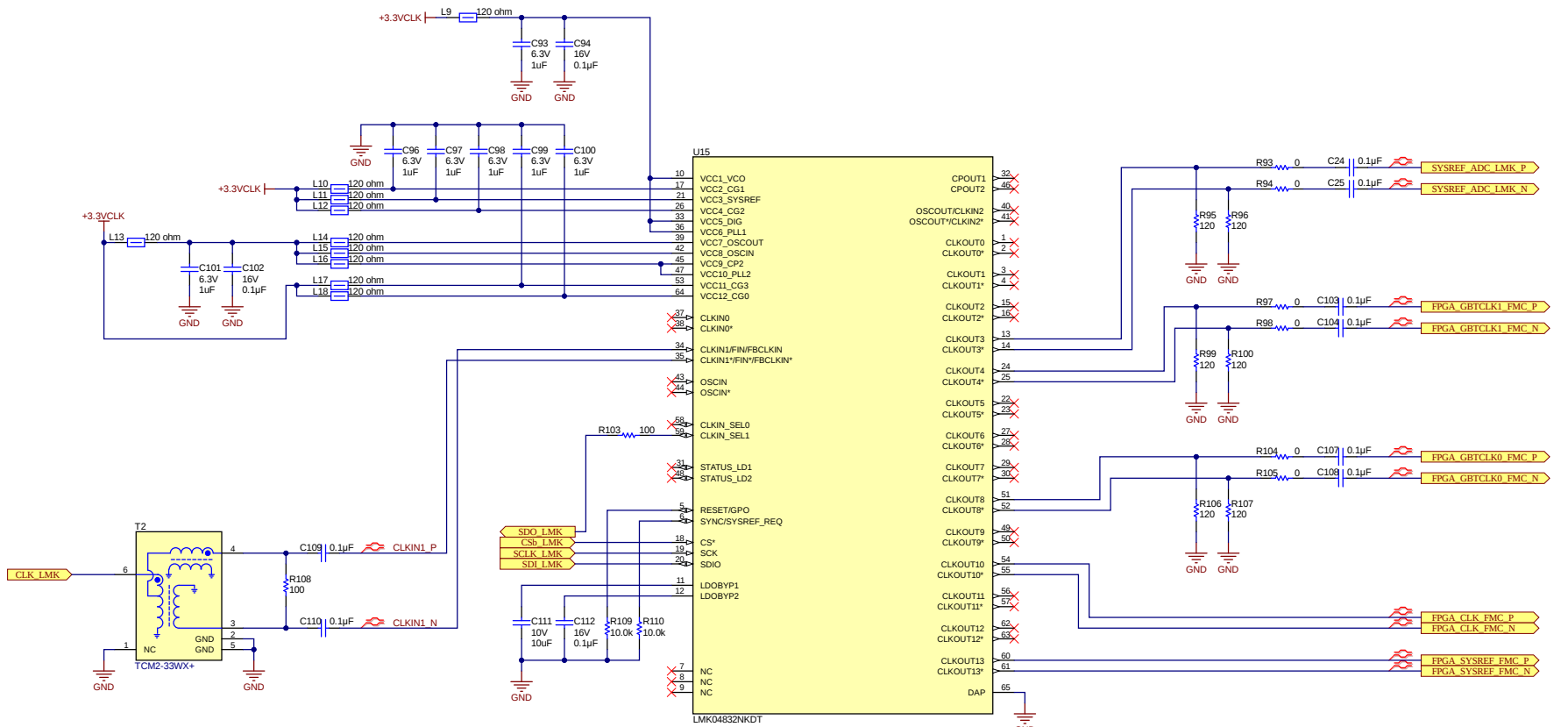
GPIO MUX Cont.



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Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: GPIO MUX Cont.
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 12 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_GPIO_MUX2_RevA_Sch	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	

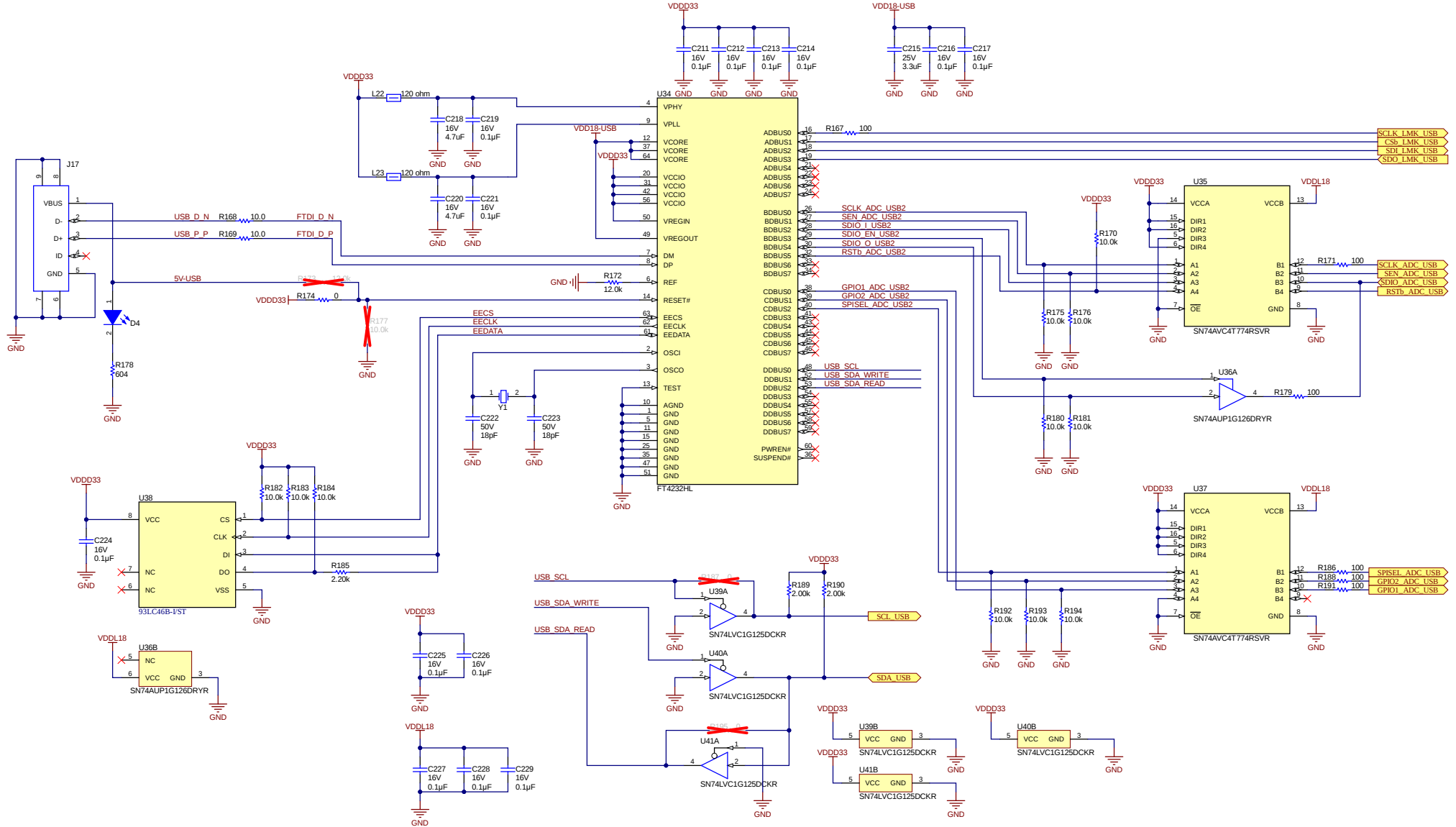
LMK04832 Clock Fanout



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Orderable:	Designed for: Public Release	Mod. Date: 3/7/2024
TID #: N/A	Project Title: TRF1305-ADC32RF55	
Number: AMP5-227	Rev: A	Sheet Title: LMK04832 Clock Fanout
SVN Rev: Not in version control	Assembly Variant: 003	Sheet 13 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_LMK_RevA_SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	

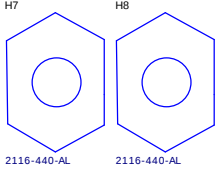
USB Interface



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Orderable:	Designed for: Public Release	Mod. Date: 8/9/2024
TID #:	N/A	Project Title: TRF1305-ADC32RF55
Number: AMPS-227	Rev: A	Sheet Title: USB Interface
SVN Rev: Not in version control	Assembly Variant: 003	Sheet: 14 of 16
Drawn By: Hruday Kumar	File: ADC32RF55_TRF1305_USB_RevA_SchDoc	Size: B
Engineer: Hruday Kumar	Contact: http://www.ti.com/support	http://www.ti.com

D



PCB
LOGO
WEEE logo

Variant/Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

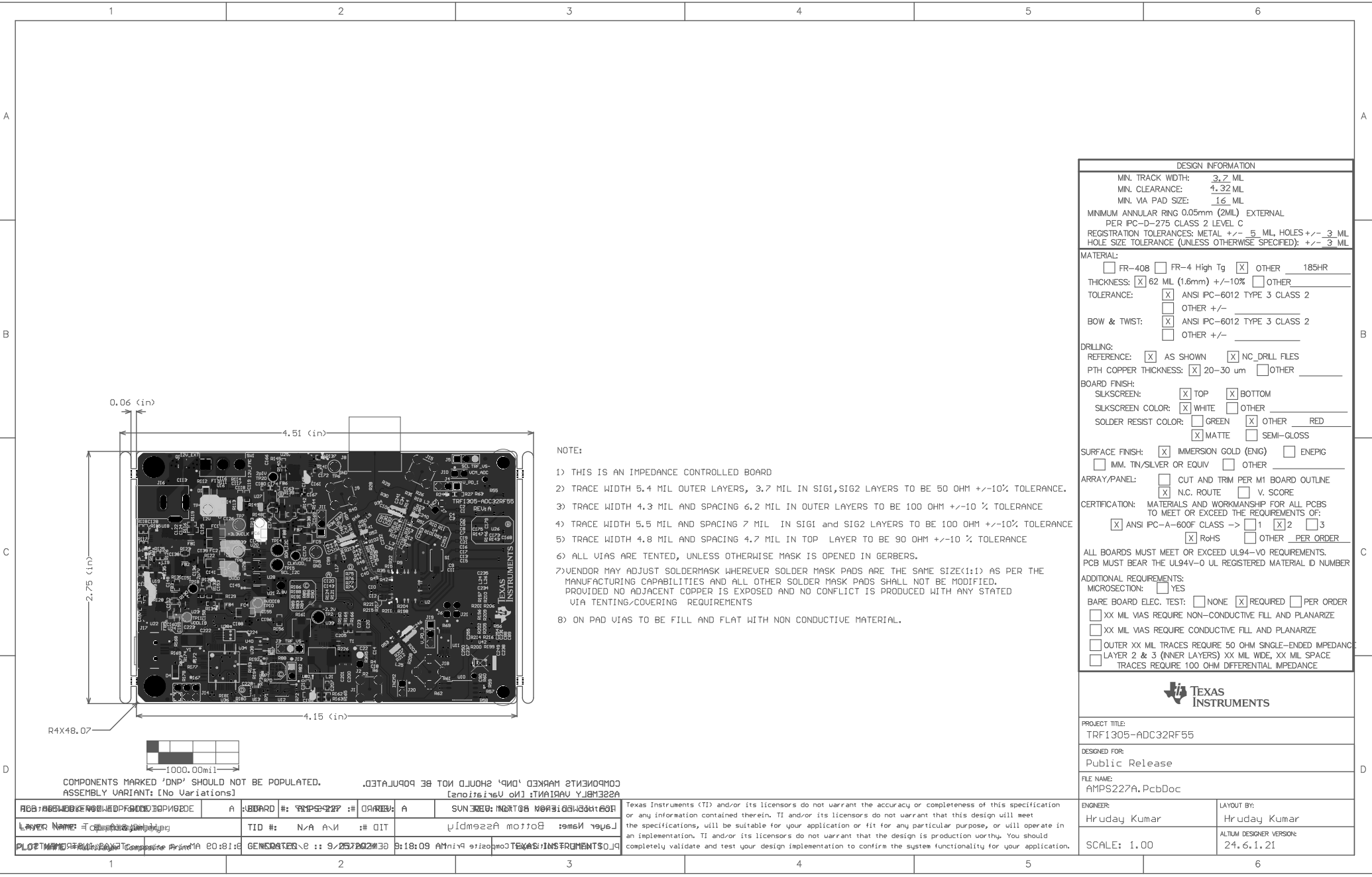
You should delete this note too.

1		2		3		4		5		6									
Rev History & Variants																			
A	Revision History <table><thead><tr><th>Rev</th><th>Release Date</th><th>Notes</th></tr></thead><tbody><tr><td>A</td><td>DD-MMM-YYYY</td><td>Initial Release</td></tr></tbody></table>											Rev	Release Date	Notes	A	DD-MMM-YYYY	Initial Release		
	Rev	Release Date	Notes																
	A	DD-MMM-YYYY	Initial Release																
	B	Variant(s) <table><thead><tr><th>Variant</th><th>Notes</th></tr></thead><tbody><tr><td>001</td><td> •Original DNI components •Used for production build </td></tr><tr><td>002</td><td> • LMK Routed as CLK input option **Changes from 001** DNI : C20,C23 Install : C41,C42 </td></tr><tr><td>003</td><td> • OSC Routed as CLK input option **Changes from 001** DNI : R25 Install : R26 </td></tr></tbody></table>											Variant	Notes	001	•Original DNI components •Used for production build	002	• LMK Routed as CLK input option **Changes from 001** DNI : C20,C23 Install : C41,C42	003
Variant		Notes																	
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003	• OSC Routed as CLK input option **Changes from 001** DNI : R25 Install : R26																		
C																			
D																			

Orderable:		Designed for: Public Release		Mod. Date: 1/26/2024	
TID #:		N/A		Project Title: TRF1305-ADC32RF55	
Number: AMPS-227		Rev: A		Sheet Title: Rev History & Variants	
SVN Rev: Not in version control		Assembly Variant: 003		Sheet: 16 of 16	
Drawn By: Hruday Kumar		File: ADC32RF55_TRF1305_Revision History_RevA.tss		Sheet: B	
Engineer: Hruday Kumar		Contact: http://www.ti.com/support			

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1	2	3	4	5	6
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- NOTE:
- 1) THIS IS AN IMPEDANCE CONTROLLED BOARD
 - 2) TRACE WIDTH 5.4 MIL OUTER LAYERS, 3.7 MIL IN SIG1, SIG2 LAYERS TO BE 50 OHM +/-10% TOLERANCE.
 - 3) TRACE WIDTH 4.3 MIL AND SPACING 6.2 MIL IN OUTER LAYERS TO BE 100 OHM +/-10 % TOLERANCE
 - 4) TRACE WIDTH 5.5 MIL AND SPACING 7 MIL IN SIG1 and SIG2 LAYERS TO BE 100 OHM +/-10% TOLERANCE
 - 5) TRACE WIDTH 4.8 MIL AND SPACING 4.7 MIL IN TOP LAYER TO BE 90 OHM +/-10 % TOLERANCE
 - 6) ALL VIAS ARE TENTED, UNLESS OTHERWISE MASK IS OPENED IN GERBERS.
 - 7) VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDER MASK PADS ARE THE SAME SIZE(1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED. PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED VIA TENTING/COVERING REQUIREMENTS
 - 8) ON PAD VIAS TO BE FILL AND FLAT WITH NON CONDUCTIVE MATERIAL.

DESIGN INFORMATION	
MIN. TRACK WIDTH: 3.7 MIL MIN. CLEARANCE: 4.32 MIL MIN. VIA PAD SIZE: 16 MIL MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL: ☐ FR-408 ☐ FR-4 High Tg ☒ OTHER 185HR THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/- BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/-	
DRILLING: REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER	
BOARD FINISH: SILKSCREEN: ☒ TOP ☒ BOTTOM SILKSCREEN COLOR: ☒ WHITE ☐ OTHER SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED ☒ MATTIE ☐ SEMI-GLOSS	
SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENEPIG ☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER	
ARRAY/PANEL: ☐ CUT AND TRM PER M1 BOARD OUTLINE ☒ N.C. ROUTE ☐ V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF: ☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3 ☒ RoHS ☐ OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL D NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: ☐ YES BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER ☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE ☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE ☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	
PROJECT TITLE: TRF1305-ADC32RF55	
DESIGNED FOR: Public Release	
FILE NAME: AMP5227A.PcbDoc	
ENGINEER: Hruday Kumar	LAYOUT BY: Hruday Kumar
SCALE: 1.00	
ALTUM DESIGNER VERSION: 24.6.1.21	