

CB-4062-0

ZR0

AI3-3B40Z

H930xxxx

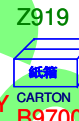
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Schematic Page Description **Page**

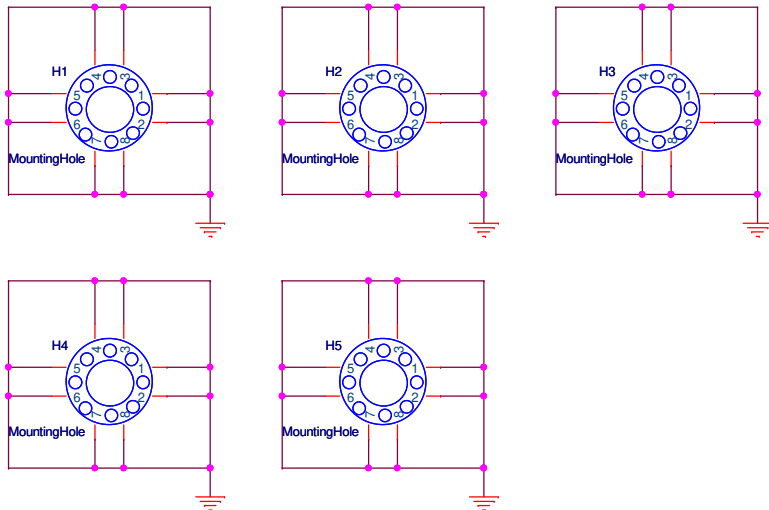
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**<-注意:
數量需改0**



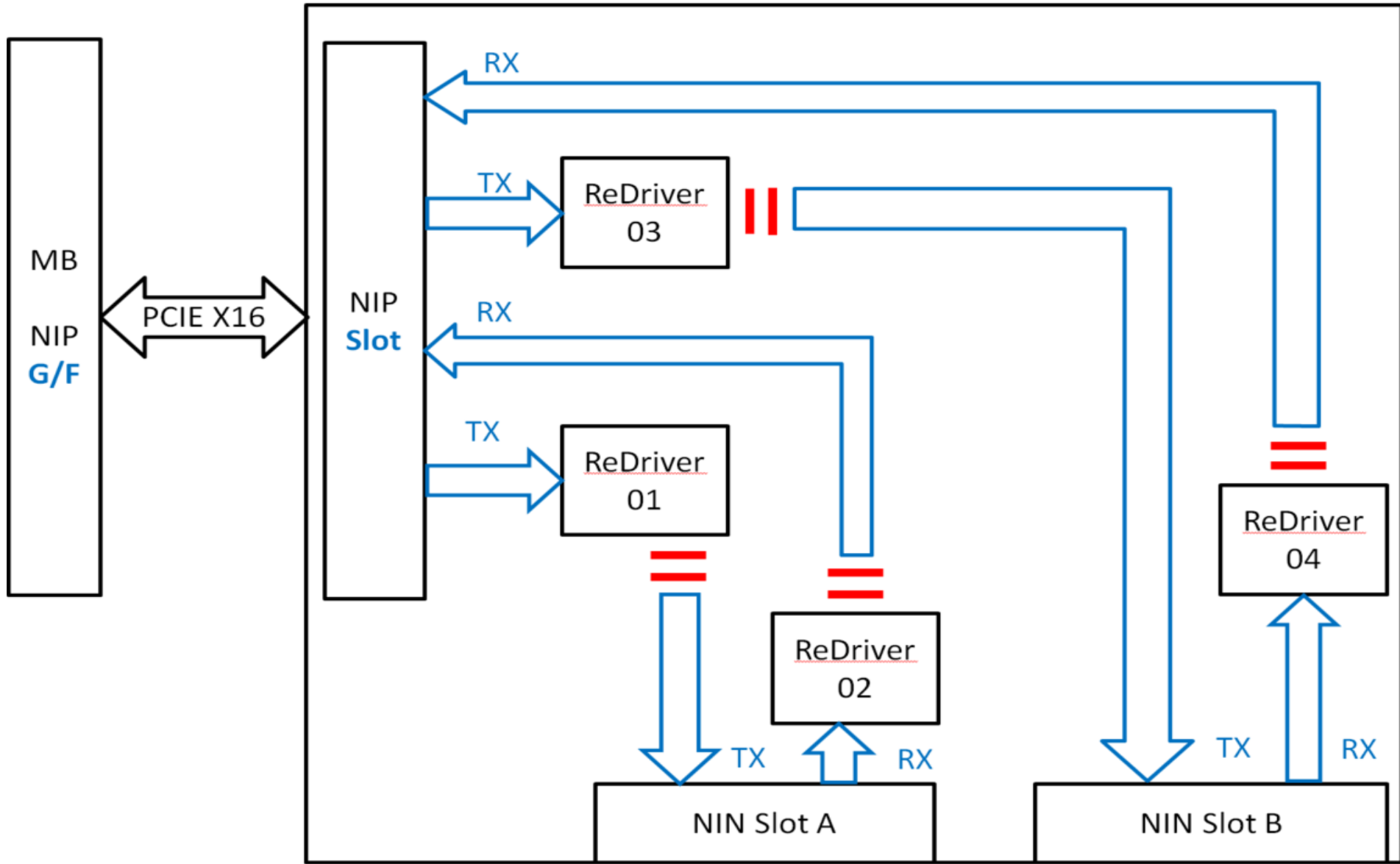
**<-注意:
數量需修改0.05**



<Variant Name>

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Complete Your Network		
Page Description		
COVER PAGE		
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P02 Block Diagram

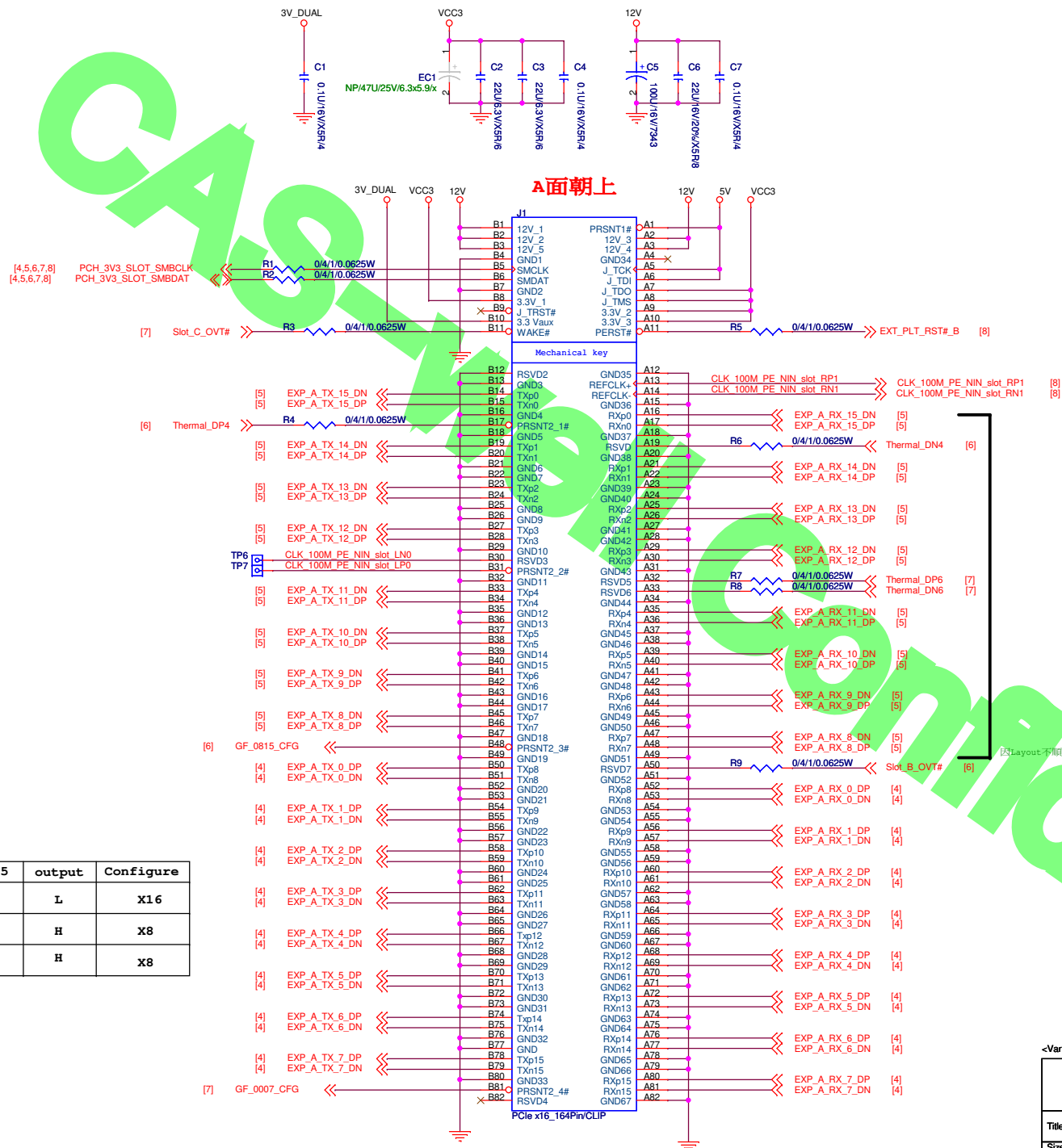


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P03_PCIe X16 NIP Slot



A面朝上

Pin.B48

0-7	8-15	output	Configure
H	H	L	X16
L	x	H	X8
x	L	H	X8

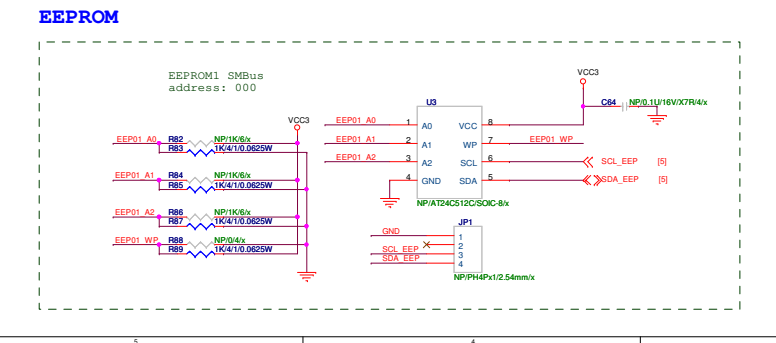
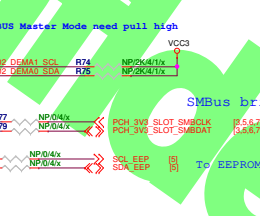
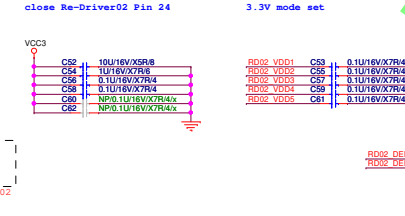
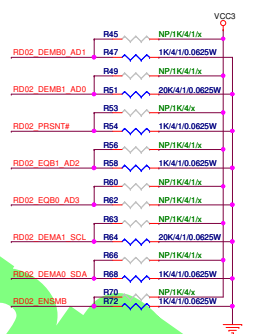
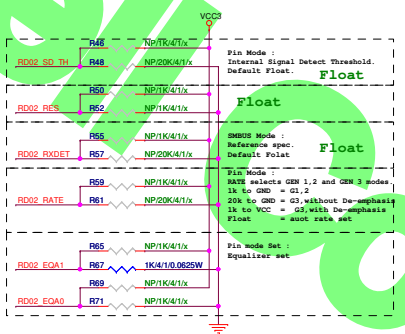
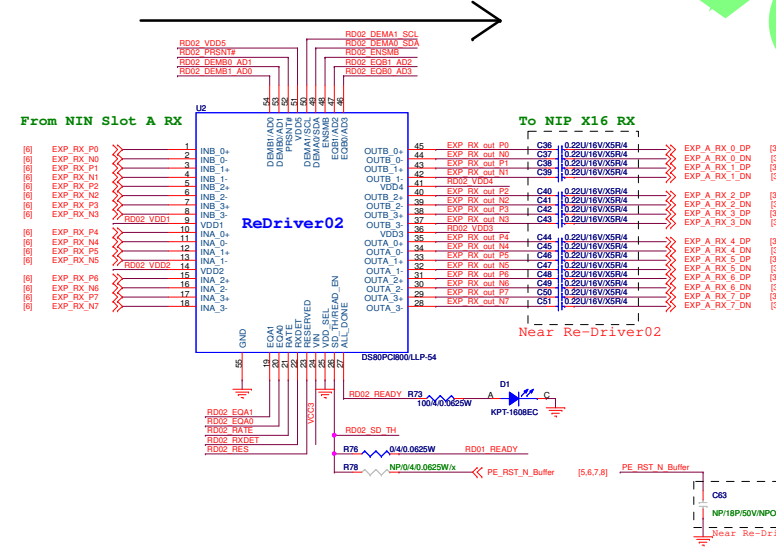
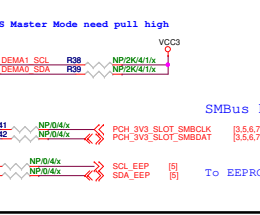
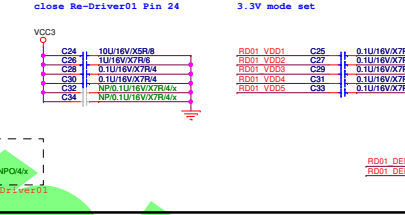
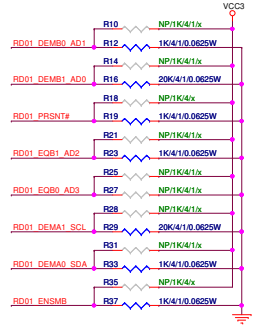
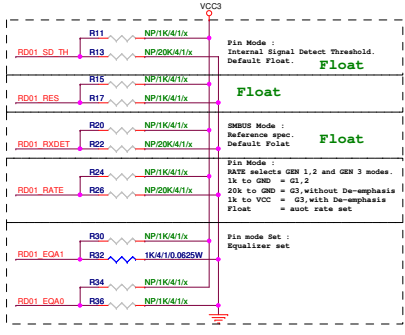
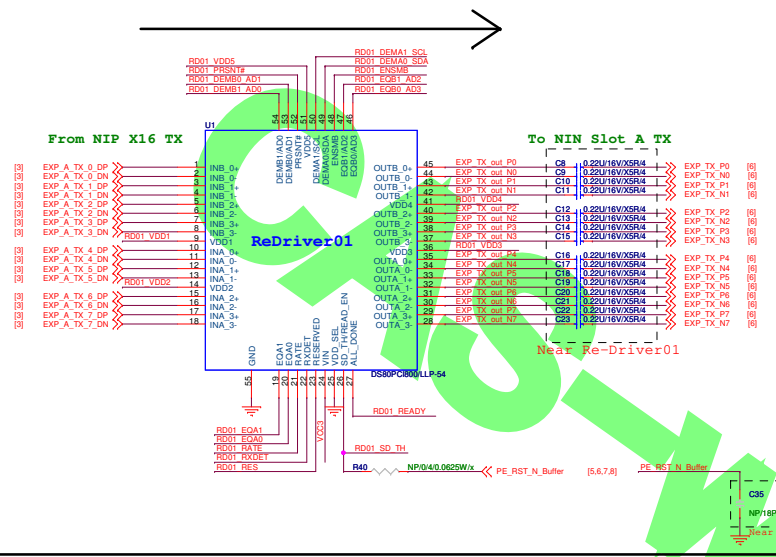
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<Variant Name>

PCIe X16 NIP Slot

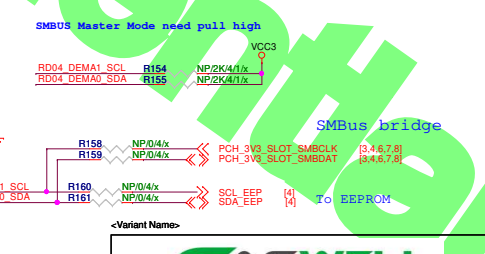
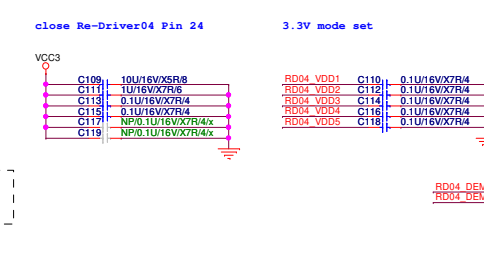
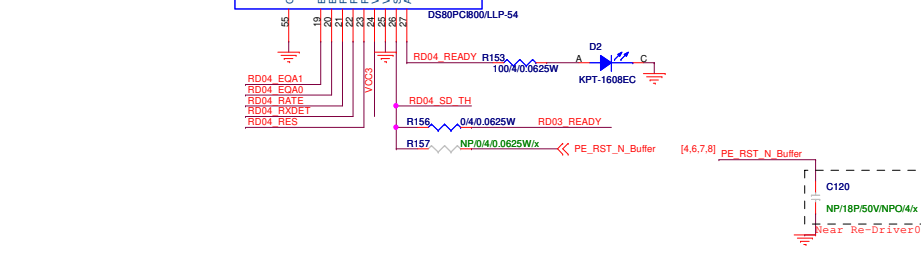
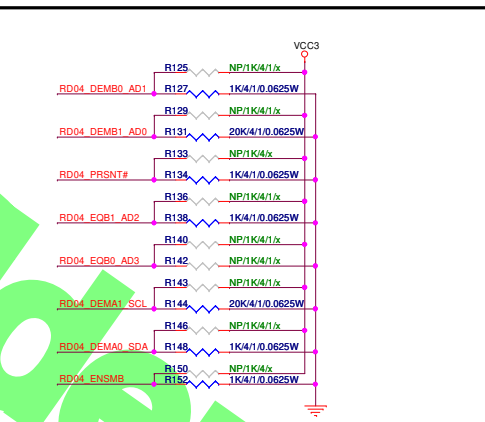
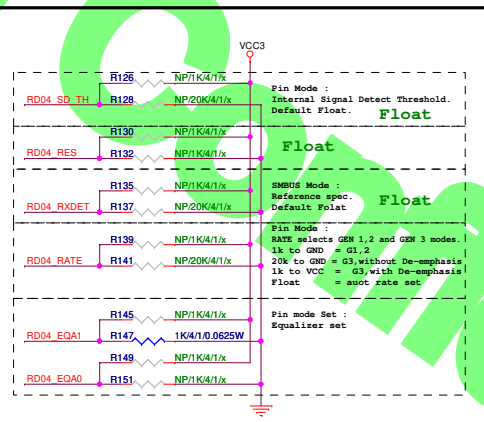
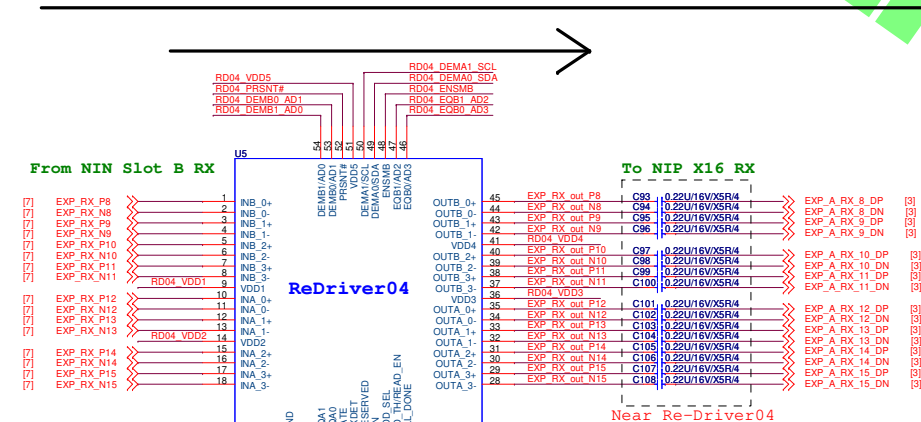
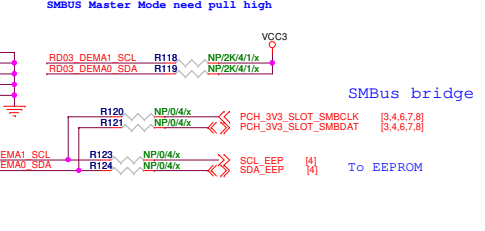
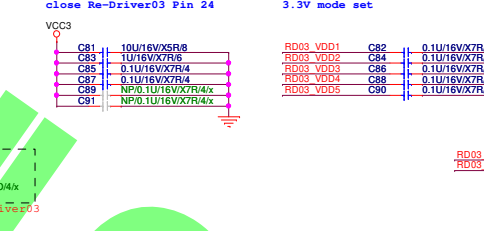
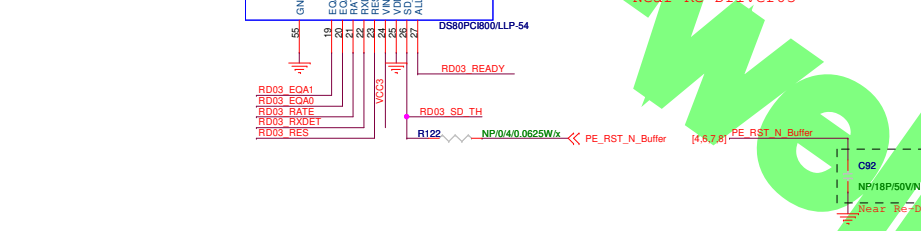
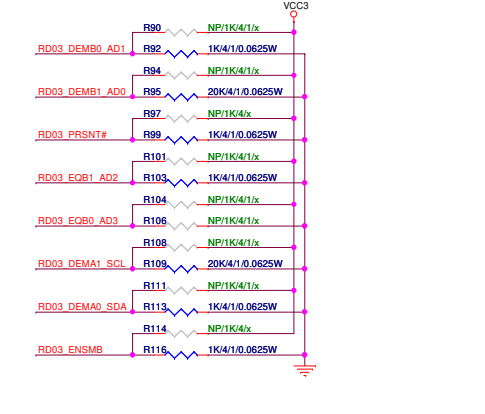
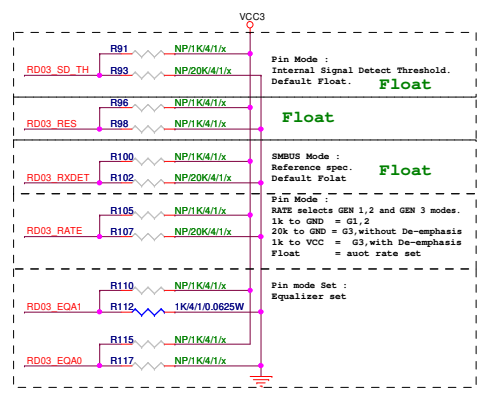
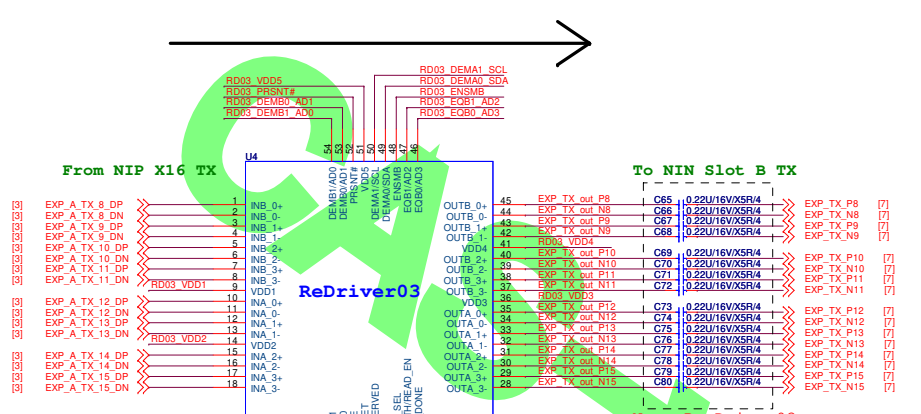
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P04_PCIE_0-7_Re-Driver (Slot A)



Variant Name:		CASWELL Complete Your Solution	
Title	PCIE_0-7_Re-Driver (Slot A)		
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P05_PCIE_8-15_Re-Driver (Slot B)



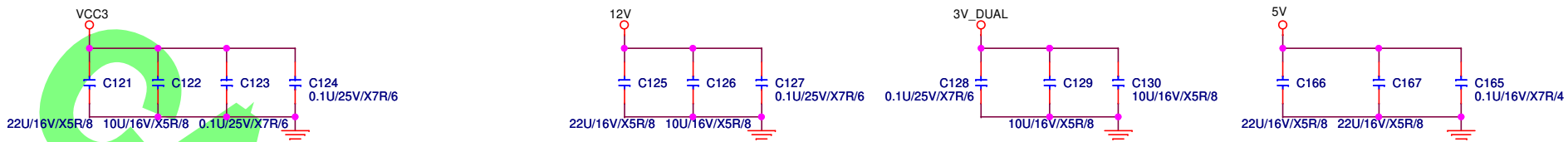
CASWELL Complete Your Solution

Title: PCIE_15-8_Re-Driver (Slot B)

Size: Custom Document Number: CB-4062-0 Rev: ZR0

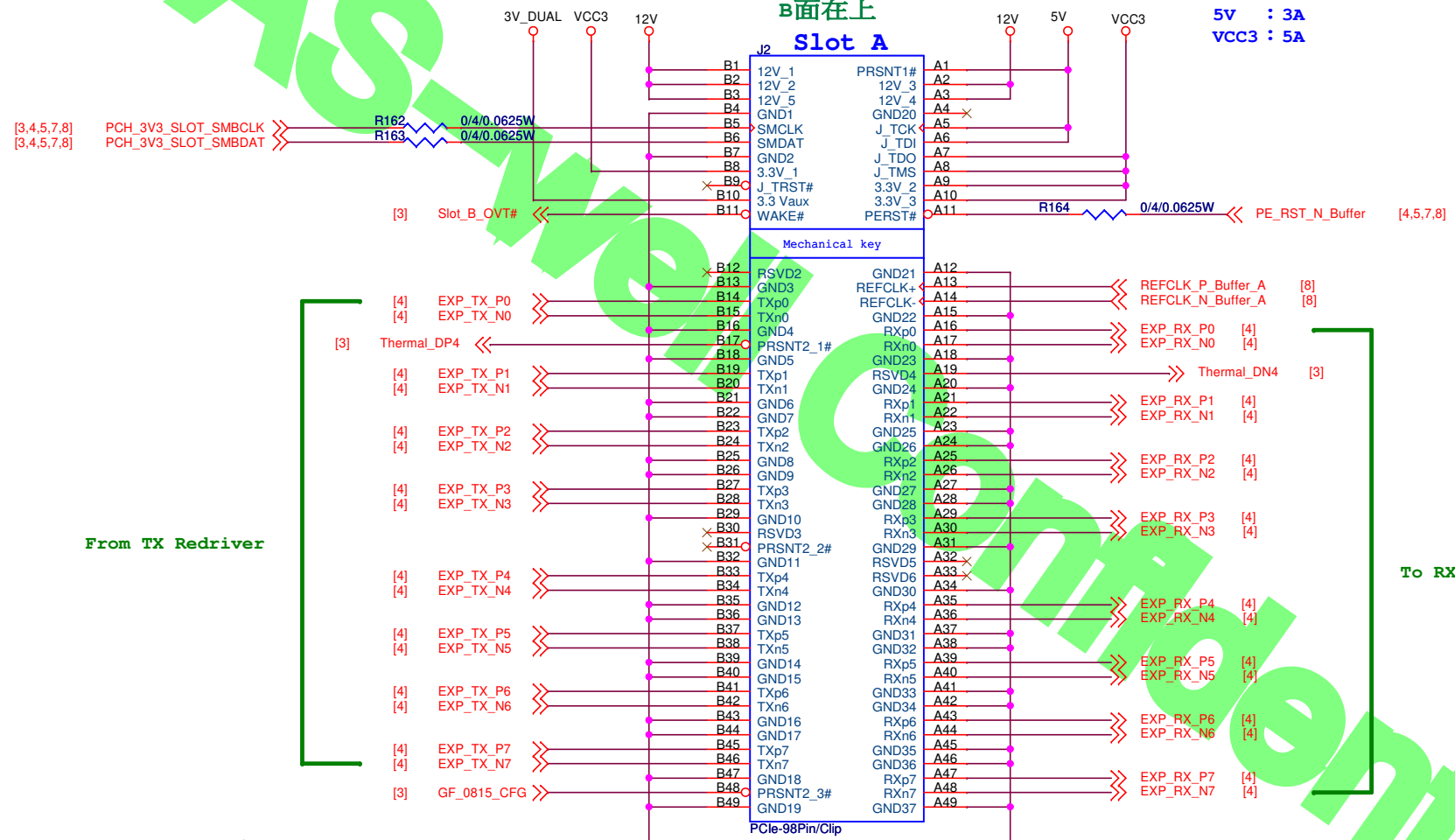
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P06 PCIe X8 NIN Slot A



12V : 5A
5V : 3A
VCC3 : 5A

B面在上
Slot A



From TX Redriver

To RX Redriver

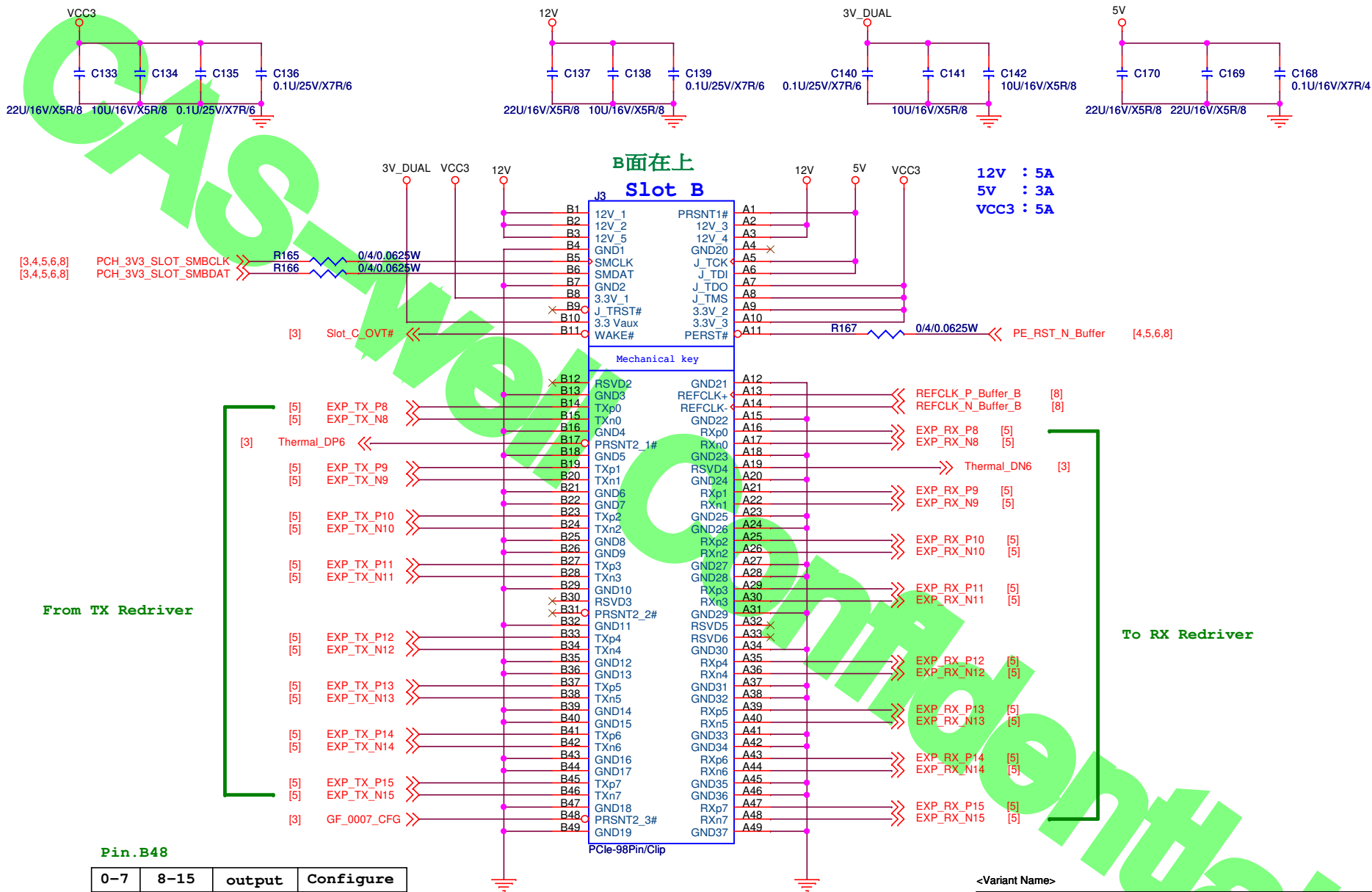
Pin. B48

0-7	8-15	output	Configure
H	H	L	X16
L	x	H	X8
x	L	H	X8

<Variant Name>

Title: PCIe X8 NIN Slot A		
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P07 PCIe X8 NIN Slot B



Pin.B48

0-7	8-15	output	Configure
H	H	L	X16
L	x	H	X8
x	L	H	X8

<Variant Name>

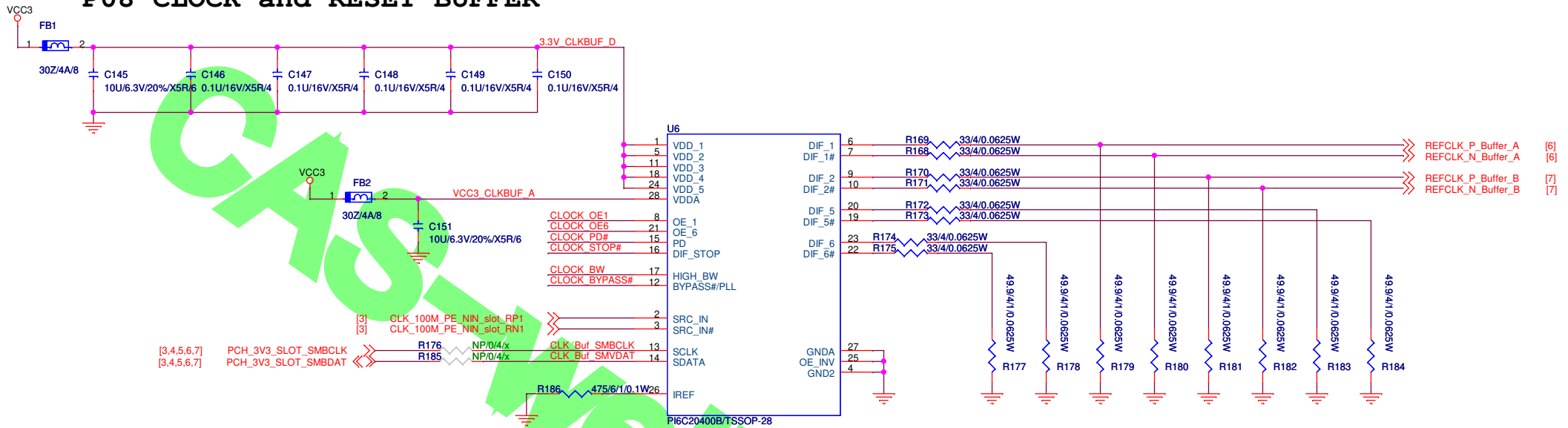


Title: PCIe X8 NIN Slot B

Size: Custom	Document Number: CB-4062-0	Rev: ZR0
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P08 CLOCK and RESET BUFFER



[3,4,5,6,7]

PCH_3V3_SLOT_SMBCLK
PCH_3V3_SLOT_SMBDAT

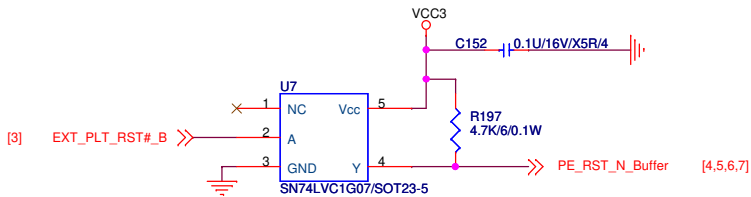
[3] CLK_100M_PE_NIN_slot_RP1
CLK_100M_PE_NIN_slot_RN1

CLOCK_OE1
CLOCK_OE6
CLOCK_PD#
CLOCK_STOP#
CLOCK_BW
CLOCK_BYPASS#

CLK_Buf SMBCLK
CLK_Buf SMVDAT

R186 475/6/1/0.1W26

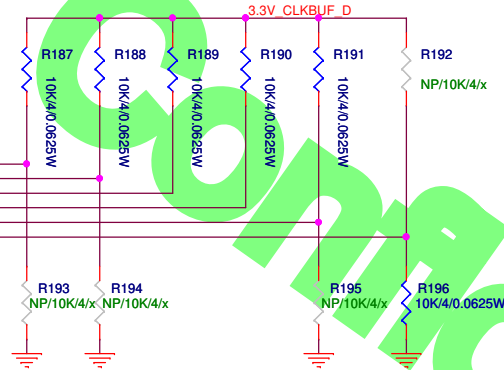
RESET BUFFER



[3]

SN74LVC1G07/SOT23-5

[4,5,6,7]



HW Strapping When OE_NIV=0		
CLOCK_OE1	0	Tri-stage outputs
	1	Enable output 1 and 2
CLOCK_OE6	0	Tri-stage outputs
	1	Enable output 5 and 6
CLOCK_PD#	0	Power down device
	1	None Power down device
CLOCK_STOP#	0	Stop differential clock output
	1	Enable differential clock output
CLOCK_BW	0	High PLL band width
	1	Low PLL band width
CLOCK_PLL	0	Bypass mode
	1	PLL mode

<Variant Name>		
CASWELL Complete Your Solution		
Title: CLOCK and RESET BUFFER		
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