Application Division (Continued)

- Keep traces connecting R_f separated and as short as possible
- **Capacitive Loads**
- Place a small resistor (20-50Ω) between the output and C_L
- **Long traces and/or lead lengths between R_f and the CLC5523**
- Keep these traces as short as possible
- **Long traces between CLC5523 and 0.1µF bypass capacitors**
- Keep these traces less than 0.2 inches (5mm)
- For the devices in the PDIP package, an additional 1000pF monolithic capacitor should be placed less than 0.1" (3mm) from the pin
- **Extra capacitance between the R_g pin and ground (C_g)**
- See the Printed Circuit Board Layout sub-section below for suggestions on reducing C_G
- Increase R_f if peaking is still observed after reducing C_g
- **Non-inverting input pin connected directly to ground**
- Place a 50 to 200Ω resistor between the non-inverting pin and ground

Adjusting Offsets and DC Level Shifting

Offsets can be broken into two parts: an input-referred term and an output-referred term. These errors can be trimmed using the circuit in *Figure 4*. First set V_g to OV and adjust the trim pot R4 to null the offset voltage at the output. This will eliminate the output stage offsets. Next set V_g to 2V and adjust the trim pot R1 to null the offset voltage at the output. This will eliminate the input stage offsets.

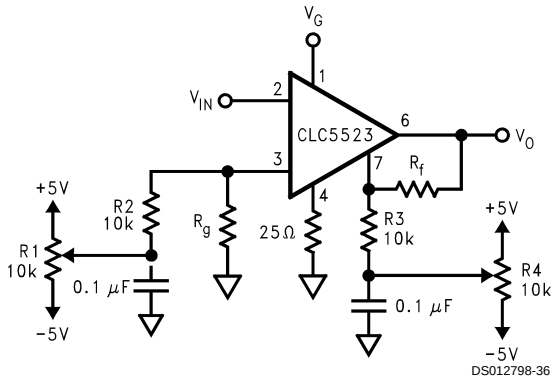

FIGURE 4. Offset Adjust Circuit

Printed Circuit Board Layout

High frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass each power supply pin with these capacitors:
- a high-quality 0.1µF ceramic capacitor placed less than 0.2" (5mm) from the pin
- a 6.8µF tantalum capacitor less than 2" (50mm) from the pin
- for the plastic DIP package, a high-quality 1000pF ceramic capacitor placed less than 0.1" (3mm) from the pin

Capacitively bypassing power pins to a good ground plane with a minimum of trace length (inductance) is necessary for any high speed device, but it is particularly important for the CLC5523.

- Establish wide, low impedance, power supply traces
- For the plastic DIP package, a 25Ω resistor should be connected from pin 4 to ground with a minimum length trace
- Minimize or eliminate source of capacitance between the R_f pin and the output pin. Avoid adjacent feedthrough vias between the R_f and output leads since such a geometry may give rise to a significant source of capacitance.
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane 0.1" (3mm) from all input/output pads
- For prototyping, use flush-mounted printed circuit board pins; **never use high profile DIP sockets**

To minimize high frequency distortion, other layout issues need be addressed.

- Short, equal length, low impedance power supply return paths from the load to the supplies
- avoid returning output ground currents near the input stage

Evaluation Boards

Evaluation boards are available for both the 8-pin DIP and small outline package types. Free evaluation boards are shipped when a device sample request is placed with National Semiconductor. The 8-pin DIP evaluation kit part number is CLC730065. The 8-pin small outline evaluation kit part number is CLC730066.

The DIP evaluation kit has been designed to utilize axial lead components. The small outline evaluation kit has been designed to utilize surface mount components.

The circuit diagram shown in *Figure 5*, applies to both the DIP and the small outline evaluation boards.

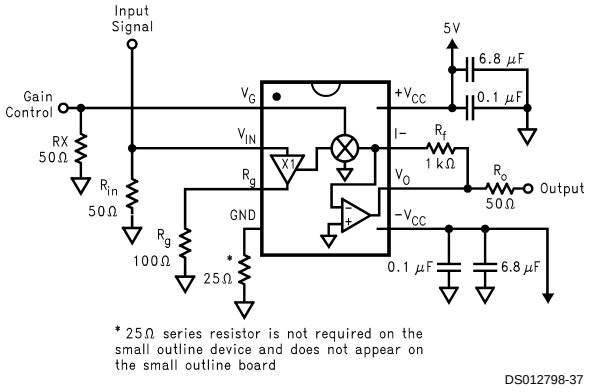

FIGURE 5. Evaluation Board Schematic

Application Division (Continued)

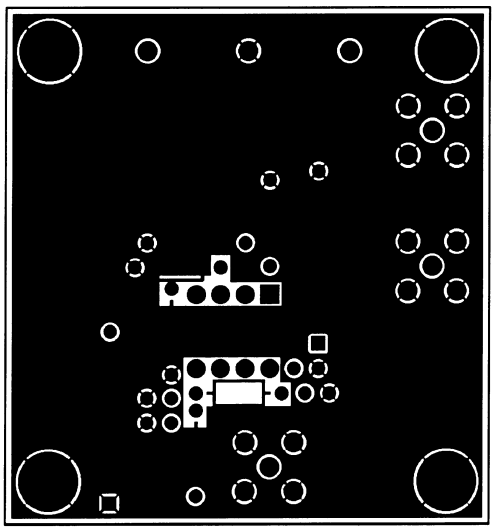

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FIGURE 6. DIP Evaluation Board (Top Layer)

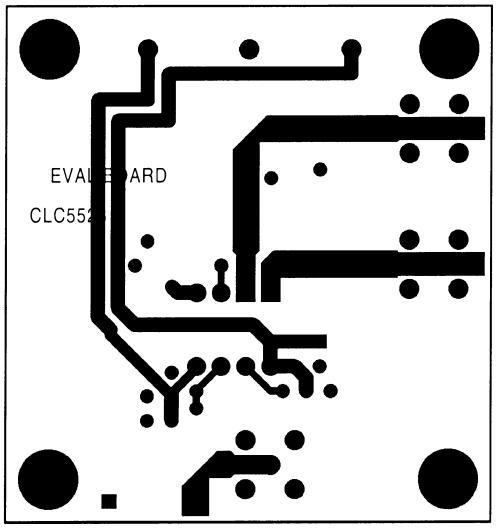

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FIGURE 7. DIP Evaluation Board (Bottom Layer)

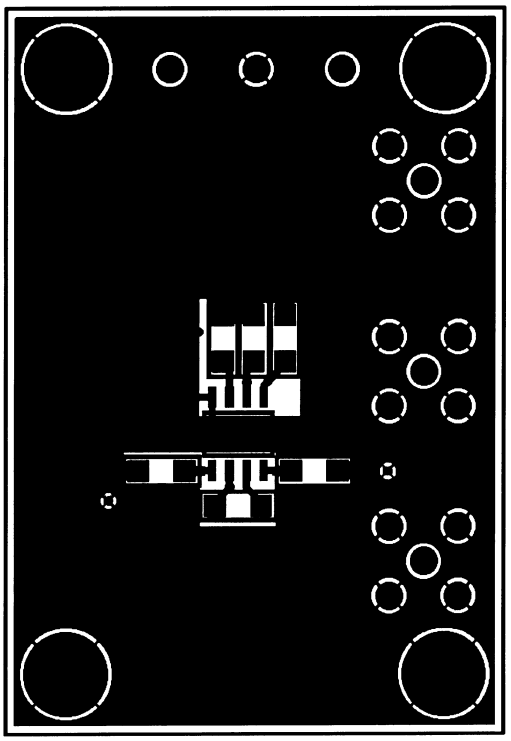

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FIGURE 8. Small Outline Evaluation Board (Top Layer)

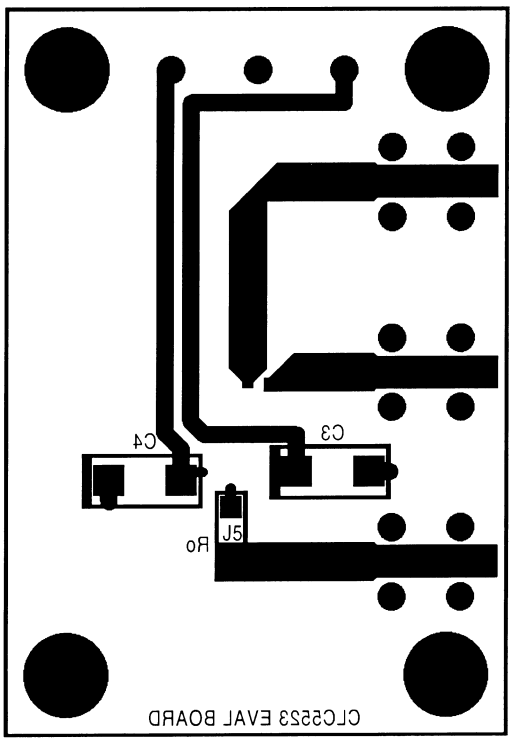

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FIGURE 9. Small Outline Evaluation Board (Bottom Layer)