The Signal Sped Up (Part 4): DC Precision Considerations for High Speed Current Feedback and Fully Differential Amplifiers

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Abstract: Current Feedback Amplifiers (CFA) provide the highest Large Signal BandWidth (LSBW), but relatively poor DC precision. The elements creating that poor DC precision will be detailed here. Of particular interest is the CMRR error in the CFA design. That low CMRR arises from the input buffer gain being <1.0. The more recent Fully Differential Amplifiers (FDA) offer both CFA and VFA versions. The CFA based versions will also have poor DC accuracy while more recent "precision" VFA based FDA's can provide much improved DC accuracy. Those VFA based FDA's do come with some added DC error sources beyond the typical op amp terms that will be described here.

DC accuracy for Current Feedback Amplifier's (CFA's)

The CFA found its true calling in low gain video line driving and differential xDSL line drivers (ref.1), where DC precision is a minor consideration in what are often AC coupled output designs. The architecture does not lend itself well to low nominal output DC errors, nor drift. Once an amplifier starts to deliver reasonably low nominal 25°C DC errors, the next layer to consider are their drift terms. All CFA's are constructed with a unity gain buffer from the V+ input to the V- input. That buffer will show these DC errors -

1. Input offset voltage and drift
2. Non-inverting bias current and drift
3. Inverting bias current and drift
4. CMRR (which arises from the buffer gain being <1.00000).

Even with considerable effort (ref. 2), the best reported input offset voltage drift is a nominal 1µV/°C with a 5µV/°C max. - where very few CFA's even specify a max. offset voltage drift. The two input bias currents for a CFA are essentially the difference between base currents arising from mismatched NPN and PNP β's. The mechanisms are completely different at the detail level for the two input bias currents, hence they are unmatched both nominally at 25°C and in their temperature drifts. The output DC error drift is often dominated by the inverting bias current drift times the feedback resistor (R_f). Even one of the most recent single channel CFA devices, the THS3491 (ref. 3), specifies only a nominal I_{b-} drift of -116nA/°C (with no min/max – but with the first ever CFA drift histograms, page17, ref. 3). CFA devices require a narrow range of feedback resistor values (R_f) for stability. Using the THS3491 recommended 576Ω for the QFN package (Av=+5V/V) translates to 576*(-116nA/°C) = -67uV/°C at the output – hardly a DC precision device. And, since the two input bias currents are not matched in either 25°C nominal nor drift terms, bias current cancellation techniques are not applicable (ref. 4).

Going one more step, the reported CMRR for a CFA device arises from the buffer gain being slightly <1.0000 (ref. 5, page 36). In the 4-equal resistor, differential to signal ended configuration, it is this slight gain loss across the input stage that gives rise to an output signal when the two inputs are driven from a common mode source. Most CFA input buffers are open loop where a typical buffer gain of 0.996 would create a CMRR spec of 48dB via equation 1 (with α≡buffer gain in V/V).

$$CMRR = -20\log(1-\alpha)$$ Eq. 1

Stand alone, open loop buffers specify a DC gain that is very load dependent due to their finite DC output impedance (Ref. 6). The input buffers used in both CFAs, and very high slew rate VFAs (Table 3, Ref. 7), see a no-load condition since the overall loop in both cases drives their output (error) current(s) to zero. The buffer output at the inverting CFA pin cascodes the error current to the current mirrors, while also forcing the inverting node voltage to follow the +V input. Being part of the overall CFA feedback loop means the error current in this buffer output is driven to zero by the high DC loop gain – identical to saying the buffer sees a no-load condition. This loop gain induced no load condition holds the buffer DC gain very constant vs. external resistor settings at just below 1.000.

This "CMRR" effect in the CFA will "contract" the gain from ideal. This is easy to see in a simple non-inverting unity gain buffer application where the input stage buffer gain reduces the gain from V+ to V- slightly below 1.0000 while the LG/(LG+1) gain compression reduces it slightly more to the output voltage. The 4 equal resistor differential to single configuration can be used more generally to probe the polarity and magnitude of the error signal across the input stage due to a common mode input voltage swing. This test case produces a very small output voltage swing reducing the input referred error due to that small V_{out} divided by the Loop Gain (LG) to an inconsequential level relative to the input error produced by the CMRR effect. That CMRR error should produce a +/-μV/V_{cm} input error voltage that then gets gained up by the Noise Gain (NG) to add to the output error (ref. 8).

The test of Figure 1 is driving a 1Hz input square wave into the 4 equal resistor circuit and looking for the polarity and magnitude of the square wave at the input error voltage sensing output. This positive first input signal will generate a negative first error signal (including the -1 in the dependent source) if the CMRR effect is a -μV/V_{cm} (or contracting gain) effect – as it is for all CFA devices. This error voltage square wave is sitting on top of the static DC error terms for the low power OPA684 (ref. 9) used in Fig.1. This 1.615mV_{pp} input error swing for a 1Vpp V_{cm} test signal (at the V+ input pin) gives

-20*log(1.615mV/1) = 55.8dB CMRR. This relatively higher CMRR for the OPA684 CFA (vs. a more typical 48dB CMRR) comes from the closed loop input buffer design and approximately agrees with the datasheet specifications. Solving eq. 1 for the buffer gain shows that the OPA684 model is delivering a nominal α=0.9984V/V.

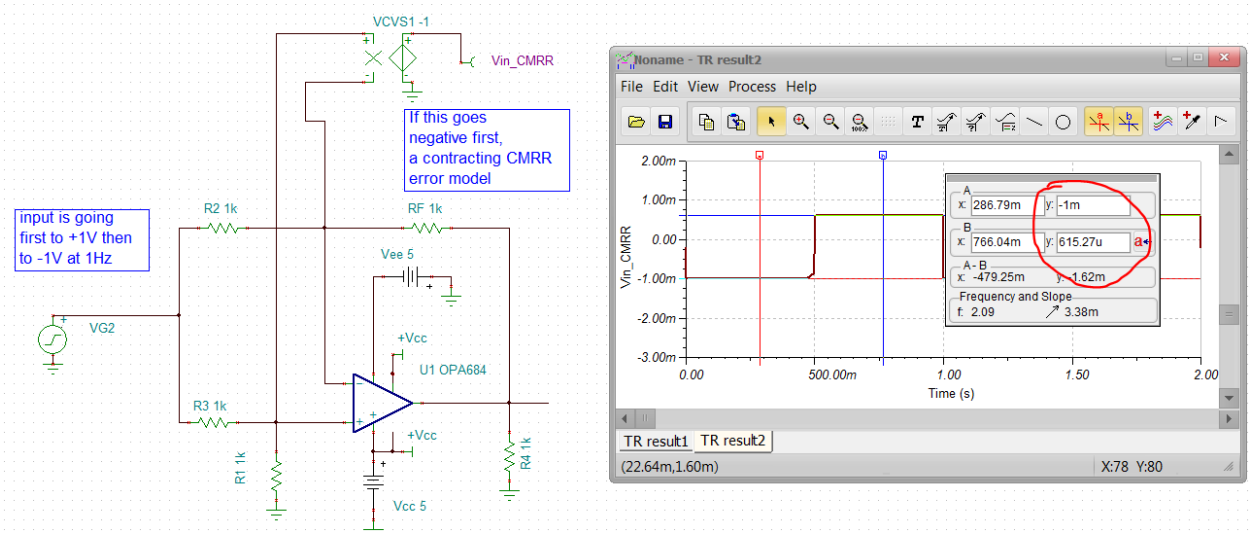

Figure 1. Input error voltage due to CMRR effects in the OP684 CFA simulation model.

While there are no true "precision" CFA op amps, there are better and worse devices. Making a simple sort on maximum 25°C input offset voltage, recognizing very few devices specify a max. offset drift (and many devices physically show an output DC drift dominated by the inverting bias current drift), will yield the rough sort of Table 1. In this range of max. offsets from 2mV to 5mV max, a secondary sort in each offset value ranked them in ascending max. 25°C supply current. In each max. input offset value, this ascending supply current roughly sorts the devices in descending input voltage noise and ascending slew rate. To get newer devices, this table also screened out –

1. Max. input Vos > +/-5mV
2. Output Headroom >2.0V
3. If both disable and not- disable versions, only disable version shown.
4. Obsolete devices

Table 1. Single channel CFA sorted by ascending max. input offset voltage.

		Operating total Vs range				Sorted in ascending Vos, then ascending Icc max								
Supplier	Device	Vs (min V)	Vs (max V)	SSBW @ Av=1 (MHz)	Slew Rate (V/µsec)	Icc Max/Ch (mA)	Vn_flatband (nV/√Hz)	Vos Max (mV)	Ib Max (V+pin) µA	Io (mA) (=min. linear)	R-R In	R-R Out	Output Headroom (V)	Part Description
TI	THS3491	14.0	32.0	900.0	8000	17.3	1.7	2.000	7	420	No	No	1.500	900MHz, 500mA high power output current feedback amplifier
TI	OPA691	4.0	12.0	280.0	2100	5.3	1.7	2.500	35	160	No	No	1.200	Wideband Current Feedback Operational Amplifier with Disable
NSM	LMH6723	4.5	12.0	370.0	600	1.2	4.3	3.000	4	48	No	No	0.900	370 MHz 1 mA Current Feedback Op Amp
TI	OPA694	7.0	12.6	1500.0	1700	6.0	2.1	3.000	20	60	No	No	1.000	WideBand, Low-Power, Current Feedback Amplifier
TI	THS3095	9.0	32.0	235.0	5000	10.5	2.0	3.000	15	200	No	No	1.800	High-Voltage, Low Distortion, Current-Feedback Operational Amplifier with Power
TI	OPA695	5.0	12.0	1700.0	2900	13.3	1.8	3.000	30	90	No	No	1.000	Ultra-Wideband, Current-Feedback Operational Amplifier with Disable
TI	OPA683	2.8	12.0	200.0	400	1.0	4.4	3.500	4	100	No	No	1.000	Very Low Power Current Feedback Amplifier with Disable
TI	OPA684	2.8	12.0	210.0	820	1.8	3.7	3.500	10	110	No	No	1.000	Low-Power, Current Feedback Operational Amplifier With Disable
TI	THS3061	9.0	32.0	300.0	5700	10.0	2.6	3.500	25	140	No	No	1.300	High-Voltage, High Slew-Rate Current Feedback Amplifier
ADI	AD8007	5.0	12.0	650.0	1000	10.2	2.7	4.000	8	65	No	No	1.100	Ultra Low Distortion, High Speed, Current Feedback Amplifier
NSM	LMH6702	10.0	12.0	1700.0	3100	16.1	1.8	4.500	15	50	No	No	1.500	1.7 GHz Ultra Low Distortion Wideband Op Amp
ISIL	EL5160	5.0	10.0	200.0	1700	0.9	4.0	5.000	4	40	No	No	1.000	Single, Low-Power, 200MHz Current Feedback Amplifier with Enable
ADI	AD8014	4.5	12.0	480.0	4600	1.3	3.5	5.000	15	50	No	No	1.200	400 MHz, Low Power, High Performance Current Feedback Amplifier
ADI	AD8011	3.0	12.0	400.0	3500	1.3	2.0	5.000	15	30	No	No	0.900	300 MHz, Low Supply Current, Current Feedback Amplifier
ISIL	EL5162	5.0	12.0	500.0	4000	2.0	3.0	5.000	8	60	No	No	1.100	Single, 500MHz Current Feedback Amplifier with Enable
ISIL	EL5164	5.0	12.0	600.0	4700	4.2	2.1	5.000	10	100	No	No	0.900	Single, 600MHz Current Feedback Amplifier with Enable
ISIL	HFA1105	9.0	11.0	270.0	2100	6.1	3.5	5.000	15	50	No	No	1.600	Single, 330MHz (@ G=2), Low Distortion, Current Feedback Video Amplifier
ISIL	HFA1135	9.0	11.0	660.0	2300	7.3	3.5	5.000	15	50	No	No	1.600	Single, 360MHz (@ G=2), Low Power, Current Feedback Amplifier (Video Amplifier)
ISIL	EL5166	5.0	12.0	1400.0	6000	9.3	1.7	5.000	25	110	No	No	1.000	Single, 1.4GHz Current Feedback Amplifier with Enable
ADI	AD8009	5.0	12.0	1000.0	5500	16.0	1.9	5.000	150	175	No	No	1.200	1 GHz, 5,500 V/µs, Low Distortion, Current Feedback Amplifier

Turning back to the very high slew rate VFA devices using two open loop input buffers (table 3, ref. 7), it might be reasonable to expect those to also show a very slight gain compression ($-\mu V/V_{cm}$) in their simulation models due to the CMRR effect. The transistor based AD8057 (ref. 10) model available in the TINA library (ref. 11) does indeed contract as shown in Fig. 2. Many of the more "macromodel" based

devices (in Table 3, ref. 7) show a positive +µV/ V_{cm} effect in this same simulation test. This simulated input error voltage swing of 0.31mV_{pp} for a 1V_{pp} V_{cm} input swing in fig. 2 solves to a 70dB CMRR. This result closely matches the AD8057 CMRR plot (fig. 30, ref. 10) but not the 60dB specification.

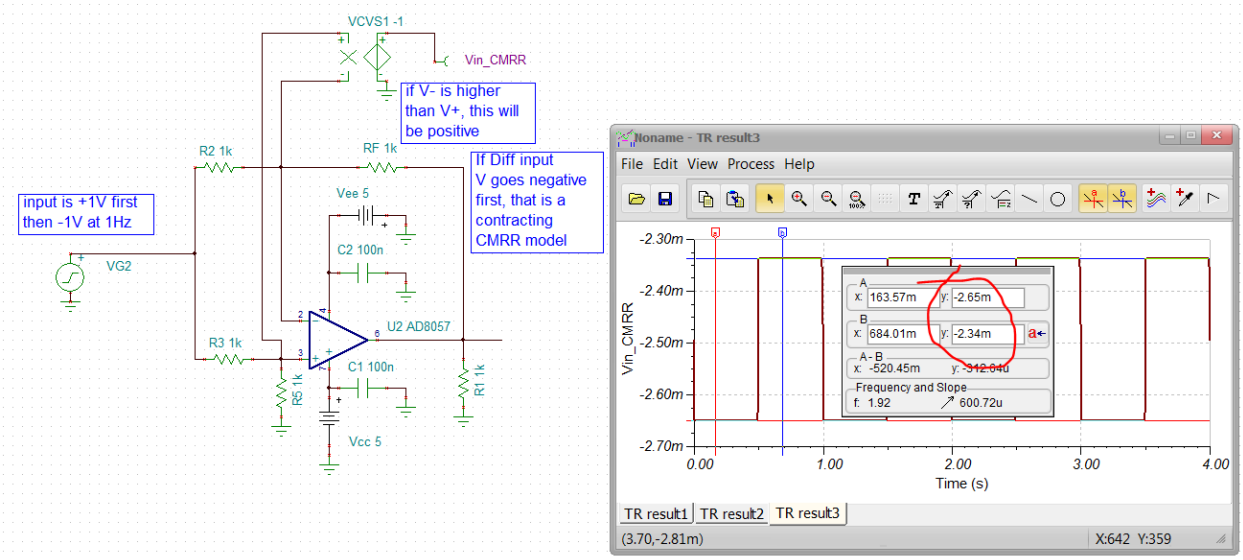

Figure 2. Input error voltage due to CMRR effect in a very high slew rate AD8037 VFA simulation model.

Looking at the other types of high speed VFA devices (ref. 7), it is unclear if they should show a + or – µV/V_{cm} error term and their models seem to essentially give random polarities (where some models have reversed polarities from their original to more recently updated versions). Some sources (slide 9, ref. 12) suggest this CMRR error should be a bipolar Gaussian distribution centered on 0µV/V. But that implies an average CMRR of infinite dB? There is possibly more modelling work that could be done on this CMRR error term in the wider range of VFA op amps.

DC Accuracy for High Speed Fully Differential Amplifier's (FDA's)

These FDA's come in both CFA and VFA types. The CFA based versions will have phenomenal slew rates but relatively poor DC precision terms. For the wide range of AC coupled signal path application using CFA based FDA solutions, this poor DC precision will not matter. The most troublesome term would be the input offset current drift specification – typically a missing spec. for these types of devices. Table 2 shows a thorough DC error specification (ref. 13) that is notably silent on I_{os} drift – likely pretty poor looking at the range on 25°C Input Offset Current.

Table 2. Example DC error specification for the very wideband, CFA based, FDA (the ADA4927, ref. 13)

INPUT CHARACTERISTICS					
Offset Voltage	$V_{IP} = V_{IN} = V_{OCM} = 0$ V	−1.3	+0.3	+1.3	mV
	t_{MIN} to t_{MAX} variation		±1.5		µV/°C
Input Bias Current		−15	+0.5	+15	µA
	t_{MIN} to t_{MAX} variation		±0.1		µA/°C
Input Offset Current		−10.5	−0.6	+10.5	µA
Input Resistance	Differential		14		Ω
	Common mode		120		kΩ
Input Capacitance	Differential		0.5		pF

Turning now to the more “precision” VFA based FDA devices (Table 3 below), these have the usual input offset voltage (V_{os}) and current offset (I_{os}) errors along with a range of other errors arising from the two feedback networks not being exactly matched - and due to the common mode control loop that is acting to hit a desired output average voltage. Only considering DC issues here, first assume the two feedback resistors and divider ratio’s to the inputs are exactly matched – as shown in the example of Figure 3 using the precision RRO, NRI THS4551 (ref. 14) with 4 equal 10kΩ resistors and a grounded V_{ocm} input on +/-2.5V supplies. Centered gaussian DC errors (like V_{os} and I_{os}) are often specified as +/- 1δ for the typical value. That bipolar value, is then assigned a polarity to include in the nominal simulation model. The full bipolar min/max error range and drifts are available in the datasheets (ref. 14). Figure 3 shows a simple DC setup with measurement probes before the DC simulation in Figure 4 where those numbers will mask the circuit underneath.

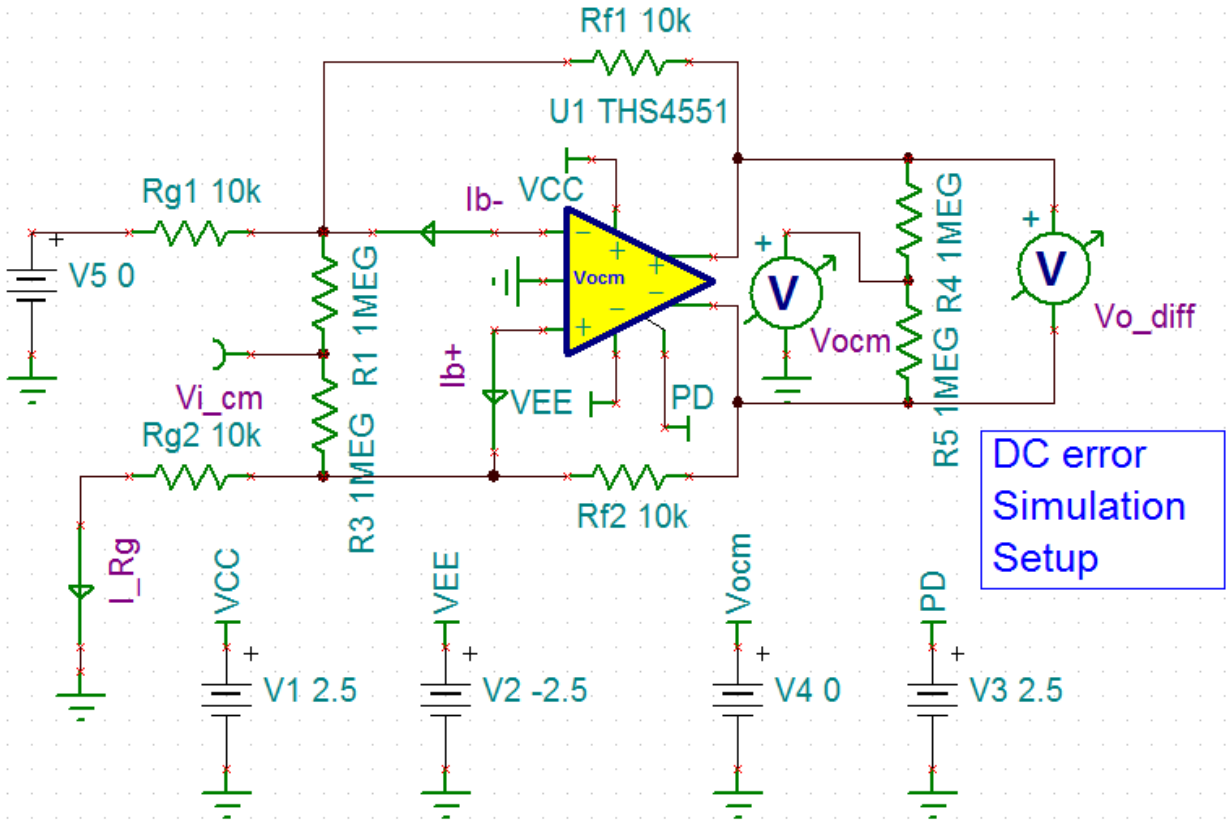

Figure 3. Equal R, THS4551 FDA nominal DC error test simulation.

And then running the DC operating point simulation shows these error terms built into the nominal model (ref. 15).

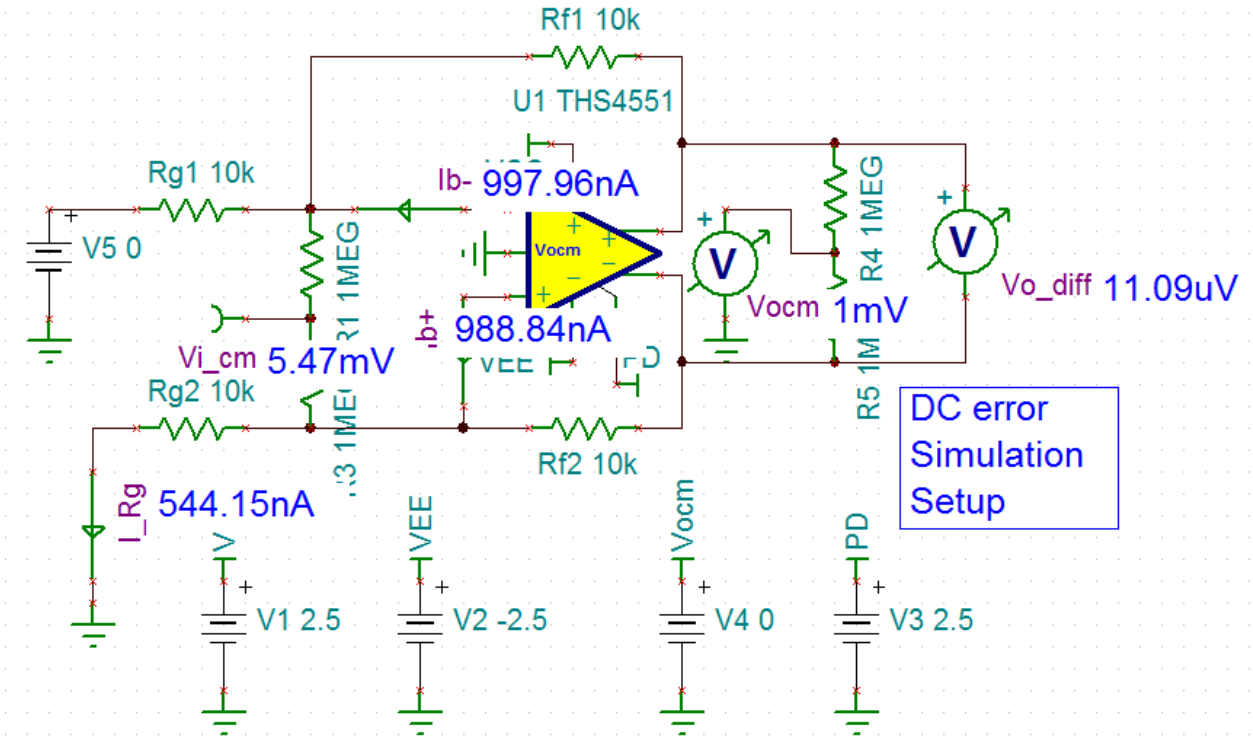

Figure 4. DC operating point errors for the precision THS4551 FDA.

Starting with the common mode voltages, the output common mode shows a +1mV positive offset from the 0V input at the V_{ocm} pin. This matches the magnitude of the typical specification of +/-1mV (ref. 14, page 9). This device is typical in that the common mode control offset error is lower with the input control pin driven vs. when it is floating. The floating input V_{ocm} offset (from mid-supply) is typically +/-2mV on this device. This output CM offset is usually of negligible concern in driving ADC's that show some tolerance on their input common mode voltage range (when specified) far exceeding these <+/-20mV output V_{ocm} errors.

This NRI, PNP input stage device, will have input bias currents that flow out of the input pins. That average value in Fig. 4 of 0.9934µA closely matches the typical 1µA in the data sheet (ref. 14, page7). This input bias current specification is uni-polar out of the input pins for this NRI device. One new aspect to the FDA is that this common mode input bias current shifts the "input" common mode voltage from the output common mode that is being controlled by the common mode control loop. The 5.47mV input common mode voltage shown in Fig. 4 has shifted up from the 1mV output common mode and correctly splits the available .993µA common mode current into the R_{g2} path to ground, and then the R_{f2} path back to the output 1mV common mode voltage. This input V_{cm} level shift is approximately the output V_{cm} voltage + the input I_{bcm} current times the $R_f||R_g$ impedance looking out the two input nodes.

The differential output offset is a combination of the input offset voltage and the effect of mismatched input bias currents (I_{os}). The nominal +50µV input offset voltage is gained up by the NG = 1 +R_f/R_g to the output while the differential offset current (I_{os}) adds an $I_{os}*R_f$ term to that. Since this I_{os} is differential,

the output common mode control loop does not come into play and the typical differential input virtual ground is used to pass this term to the output times just the R_f value.

The THS4551 model (ref. 15) sets the typical V_{os} polarity to be a 50uV rise from V+ to V-. This will produce an output of +100uV for V_{o_diff} (Using the (Vo+) – (Vo-) voltmeter in fig. 4). This simulated output offset is then reduced superimposing the nominal model polarity of the I_{os} term. There, the 9nA I_{os} is higher on the non-inverting input pin than the inverting, approximately reducing the 100µV output due to V_{os} by the 9nA*10kΩ ≈ -90uV yielding close to the simulated value of +11µV. Again, the model assigns nominal values and polarities while the full range shown in the datasheet (ref. 14) should be used for output differential offset min/max analysis.

Temperature drifts on the input bias current average value will simply shift the input common mode voltage. Temp. drift on the V_{ocm} offset voltage will show up directly as output V_{ocm} drift. Temp. drift on the V_{os} and I_{os} terms will have the same gain as the static values, the NG for V_{os} and R_f for I_{os}.

The input stage CMRR is usually high enough to be a minor error contribution in these precision FDA's. The simple test of Figure 5 drives a +/-2V input to matched 1kohm R_f=R_g resistors. This will divide down to a +/-1V input CM swing which produces the very small 3.56µV input error voltage due to CMRR. This error swing calculates out to 115dB CMRR matching the plot (Fig. 41, ref. 14) but not the typical 110dB CMRR specification. This small positive +uV/Vcm effect then gets to the output times the NG.

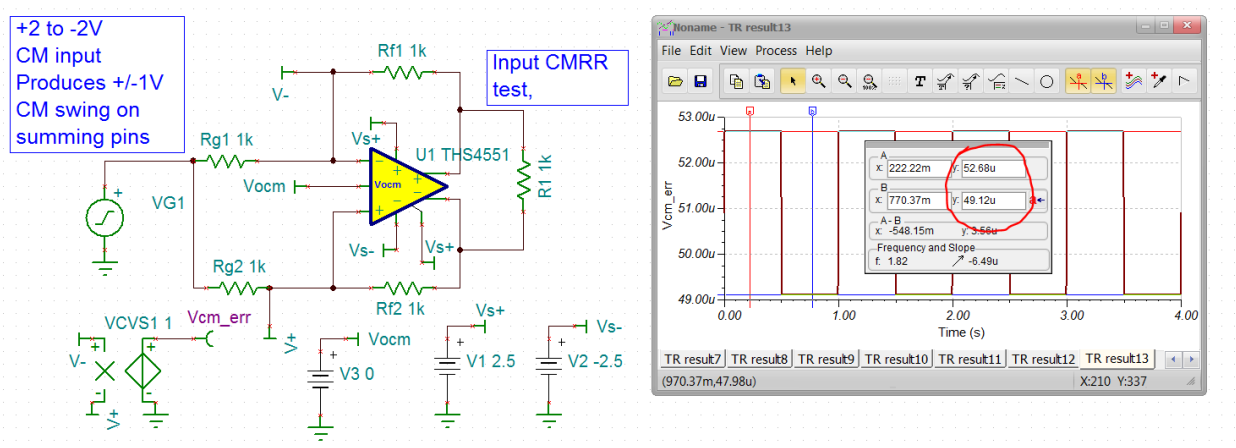

Figure 5. Input stage CMRR test circuit using the THS4551 model.

The effect of mismatched R's around the FDA on DC precision

Mismatched resistors around the FDA will add more output DC error terms beyond the simple ones considered thus far. The first to consider is simply the effect of equal standard value feedback R_f's, but with some tolerance on their values. Setting up a DC simulation with +/-1% mismatched R_f values at a NG of 1, will give the typical output error of Figure 6. Here, the NG = 1 so the output starts with the +50µV V_{os} offset. The 200ohm mismatch in the feedback R_f values gives a differential gain to the I_{bcm} term - a negative going 1µA *200Ω adding -200µV offset producing the final -150µV shown in Fig. 6. The model input offset voltage is shown by (V-) – (V+) probes to equal 50uV. Again, this is simply a nominal

value for modeling purposes where the full +/-175µV 25°C max. tested V_{os} range and +/-50nA I_{os} range should be used in output DC error band analysis (ref. 14).

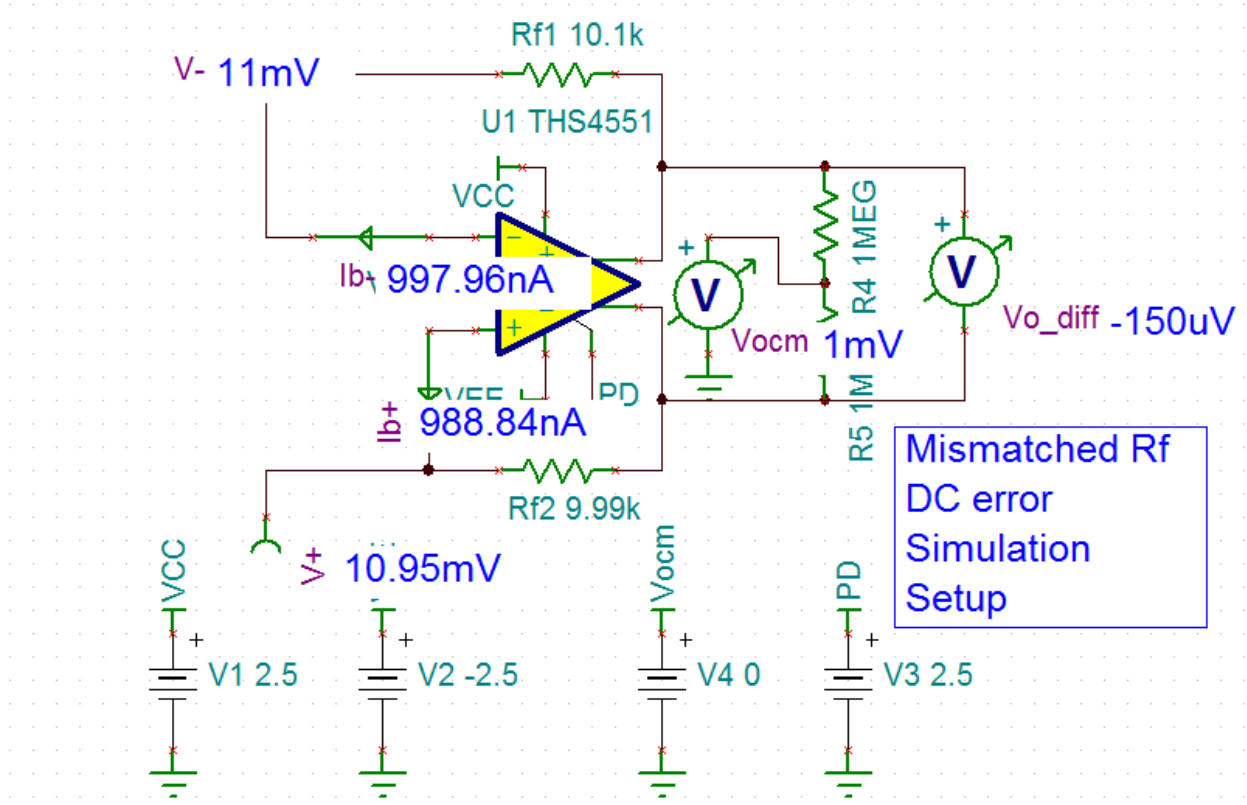

Figure 6. Mismatched Rf test showing output V_{o_diff} shift.

Moving on to imbalance the feedback divider ratios brings in a range of common mode to differential conversion errors. The conversion gain from any output CM term to the output differential error is shown in Eq. 2. Here, $G_1 \equiv R_{f1}/R_{g1}$ and $G_2 \equiv R_{f2}/R_{g2}$ in Fig. 7 (Eq. 2 is algebraically equivalent to the more convoluted expression in ref. 17, page 26)

$$V_{od} = \frac{V_{ocm} * (G_1 - G_2)}{1 + \frac{G_1 + G_2}{2}} \qquad \text{Eq. 2}$$

The test case of Figure 7 can be used to validate this error. Here, a +/-50mV 1Hz square wave is applied to the V_{ocm} input where, with equal feedback R's, the G terms are imbalanced with +1% higher ratio the upper path and -1% lower gain on the lower feedback path. Putting those into Eq. 2 shows a +0.01 gain for the input V_{ocm} signal – as shown in the output waveform of Fig. 7. This $100mV_{pp}$ input on V_{ocm} appears as a $1mV_{pp}$ differential error at the output due the feedback ratio mismatch.

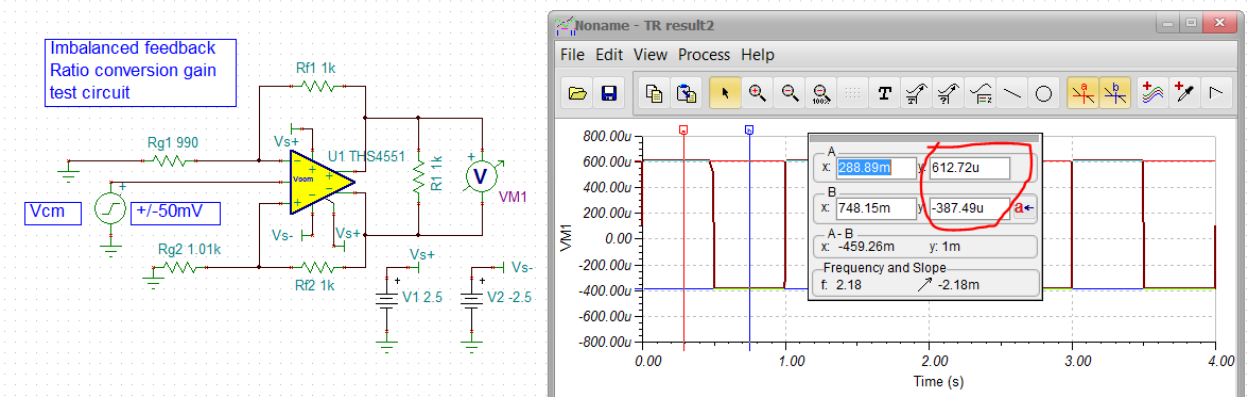

Figure 7. Conversion gain from V_{ocm} variation to output differential voltage due to gain mismatch

This CM to DM conversion gain applies to –

1. The FDA V_{ocm} input voltage and drift
2. The signal sources' V_{icm} voltage and drift

A very common way to generate a poor output static DC differential offset is to imbalance the gain networks when designing for a single supply, single to differential, 50ohm input matched application. Figure 8 shows this typical design using the gain of 1V/V, active impedance solution for a 50Ω match to a 50Ω signal source (Table 2, ref. 14). Here, the gain mismatch is relatively low, but multiplying that by the 2.5V V_{ocm} input voltage on this single +5V supply design predicts a differential output error due to this output offset term of -1.59mV – far exceeding all other initial 25°C differential output offset error terms. The simulation in figure 8 shows this slightly reduced by the other differential offset terms in the FDA itself. A simple improvement to this built in error is to match the nominal resistor network on the R_{g2} side as seen on the signal input side. Often, this relatively large initial differential output offset can be calibrated out where then the more important terms are the drift effects for each output differential offset contribution.

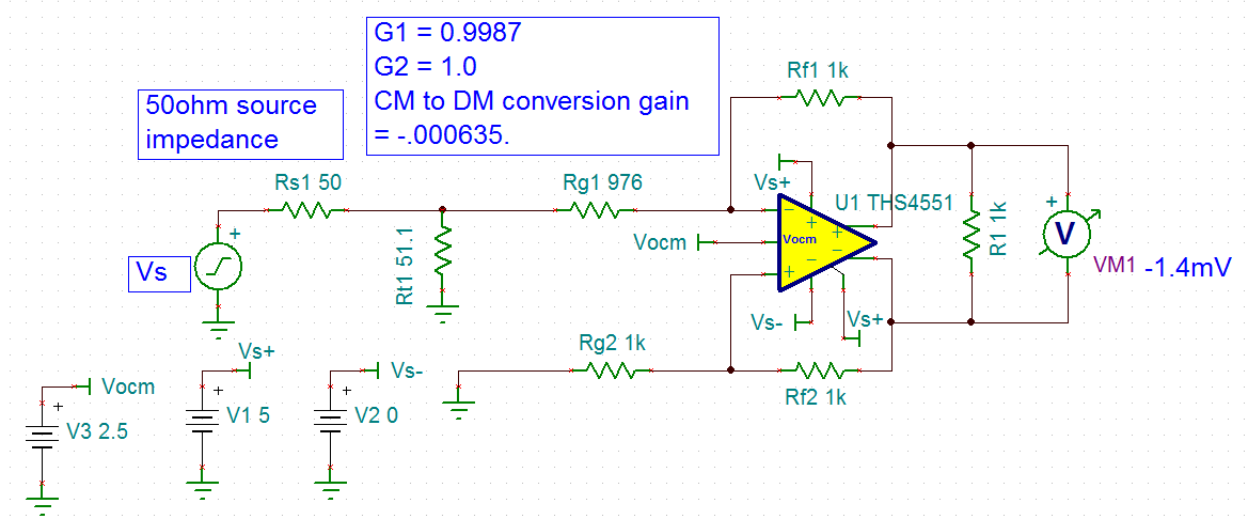

Figure 8. Output differential offset due to gain imbalance and input V_{ocm} voltage.

This CM to DM conversion gain can have both a static error due to standard value selections, and then a spread due to resistor tolerancing, and a spread plus drift due to the V_{ocm} input tolerance and drift through to the output CM voltage. Often, this V_{ocm} based output differential offset "drift" term will be negligible relative to the input offset voltage drift term times the noise gain. Using the maximum +/- 10µV/°C CM offset drift for the THS4551 (ref. 14), and the conversion gain of Figure 8, only gives an output differential drift of .0063µV/°C. While the nominal output differential offset can often be dominated by this V_{ocm} input times the gain imbalance conversion gain, its drift contribution can often be neglected where the input offset voltage drift times the noise gain normally dominates the output differential offset drift.

The effect of input common mode bias current (I_{bcm}), combined with resistor imbalances, is a new error source in all VFA based FDA's. Briefly, the I_{bcm} term will first generate an added output differential offset due to mismatched R_f values. Also, this I_{bcm} times the average impedance looking out of each input ($R_f||R_g$) will generate a shift in the input common mode voltage (the output CM control loop pushes this error to the input pin CM voltages). That voltage will then generate an output differential error times the (G_1-G_2) terms described earlier. These same gains will apply to the I_{bcm} drift error term.

Recent FDA introductions have vastly improved on the input stage DC error terms. Table 3 shows a range of these solutions sorted in ascending 25°C maximum input offset voltage. To limit these single channel selections, the following were also screened out –

1. Max 25°C input offset voltage >1.5mV
2. 1k MSRP > $4.00
3. Obsolete devices

Note there are a few G_{min}>1 devices indicating a de-compensated design where lower input voltage noise with higher slew rate is usually the intent. A G_{min} = 1V/V in this FDA case would be a DC NG=2. This sometimes means a low phase margin condition can be experienced with simple bandlimiting feedback capacitors - taking the NG to 1V/V at higher frequencies (ref. 16).

Table 3. Single Channel, Precision, VFA based FDA devices

		Operating total Vs range						Sorted in ascending Vos							
Supplier	Device	Vs (min V)	Vs (max V)	SSBW @ Gmin (MHz)	Gmin (V/V)	Slew Rate (V/µsec)	Icc Max/Ch (mA)	Vn_flatband (nV/√Hz)	Vos Max (mV)	Ib Max (V+pin) nA	Io (mA) (=min. linear)	R-R In	R-R Out	Output Headroom (V)	Part Description
LTC	LTC6363	2.8	11.0	35.0	1	75	1.9	2.9	0.100	1.00E+02	18	-Vs	Yes	0.150	Precision, Low Power Differential Amplifier
TI	THS4551	2.7	5.4	150.0	1	220	1.4	3.3	0.175	1.50E+03	45	-Vs	Yes	0.200	Low Noise, Precision, 150MHz Fully Differential Amplifier
TI	THS4561	2.9	12.6	70.0	1	130	0.9	5.0	0.200	6.00E+02	27	-Vs	Yes	0.200	Low Power, High Supply Range, 70Mhz fully differential amplifier
LTC	LTC6362	2.8	5.5	34.0	1	45	1.1	3.9	0.200	3.50E+02	10	Yes	Yes	0.080	Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver
ADI	ADA4940-1	3.0	7.0	260.0	1	95	1.4	3.9	0.350	1.60E+03	46	-Vs	Yes	0.070	Ultralow Power, Low Distortion, Fully Differential ADC Driver
TI	THS4531A	2.5	5.5	36.0	1	250	0.4	10.0	0.400	2.10E+02	25	-Vs	Yes	0.100	Ultra Low-Power, RRO, NRI, Fully Differential Amplifier with improved offset
TI	THS4541	2.7	5.4	620.0	1	1500	10.5	2.2	0.450	1.30E+04	35	-Vs	Yes	0.200	NRI, RRO Precision 850Mhz Fully Differential Amplifier
ADI	AD8139	4.5	12.0	240.0	2	800	25.5	2.3	0.500	8.00E+03	100	No	Yes	0.200	Low Noise, Rail-to-Rail, Differential ADC Driver
NSM	LME49724	5.0	36.0	50.0	1	18	15.0	2.1	1.000	2.00E+02	40	No	No	1.750	High Performance, High Fidelity, Fully Differential Audio Amp
ISIL	ISL55210	3.0	4.2	2200.0	4	5600	37.0	0.9	1.400	1.20E+05	40	No	No	0.900	Wideband, Low Power, Ultra-High Dynamic Range Differential Amplifier

DC Error Considerations for High Speed CFA and FDA Devices

CFA's (and CFA based FDA devices) will not be able to provide good DC precision. Beyond the dominant error terms from relatively high input offset voltage drift and mismatched input bias current terms, the CFA will have a CMRR effect that will look like a negative µV/V_{cm} input error for a non-inverting gain configuration. This will act to compress the non-inverting gain from ideal (with a similar effect likely in the very high slew rate VFA topology using two open loop input buffers).

VFA based FDA's start out with the usual input offset voltage and offset current errors, but then add a myriad of static and drift errors due to mismatched resistor networks on the two sides. Often, that mismatch will deliver the dominant static error through the desired V_{ocm} voltage, but rarely a meaningful drift term. Some recent permutations to the LTC6363 FDA (ref. 17) have added precision on chip resistors to reduce these resistor mismatch errors in fixed gain alternatives. Next up – high speed amplifier stability issues!! More commonly known as the full employment program for high speed amplifier application engineers!!

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