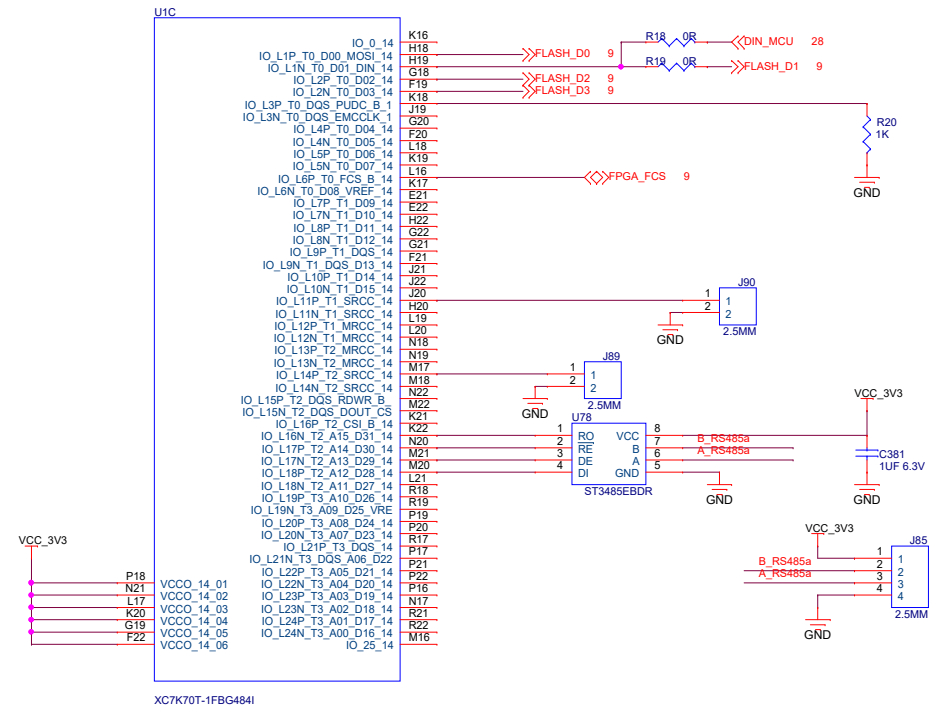
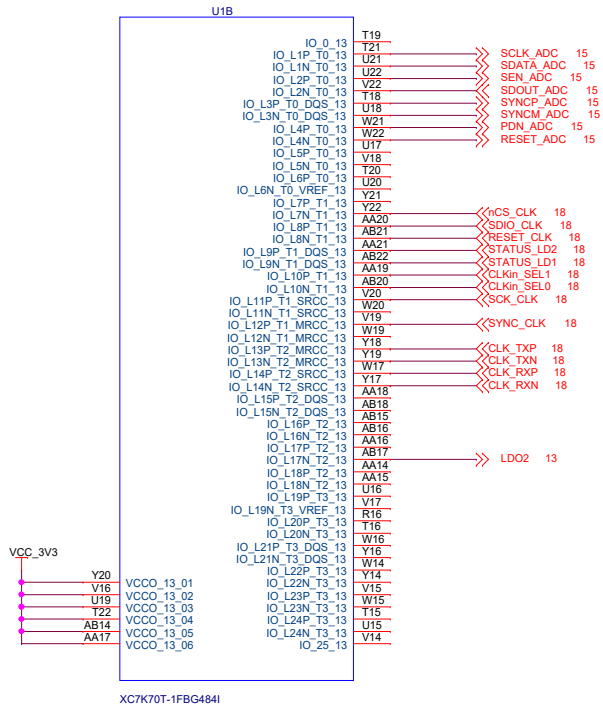
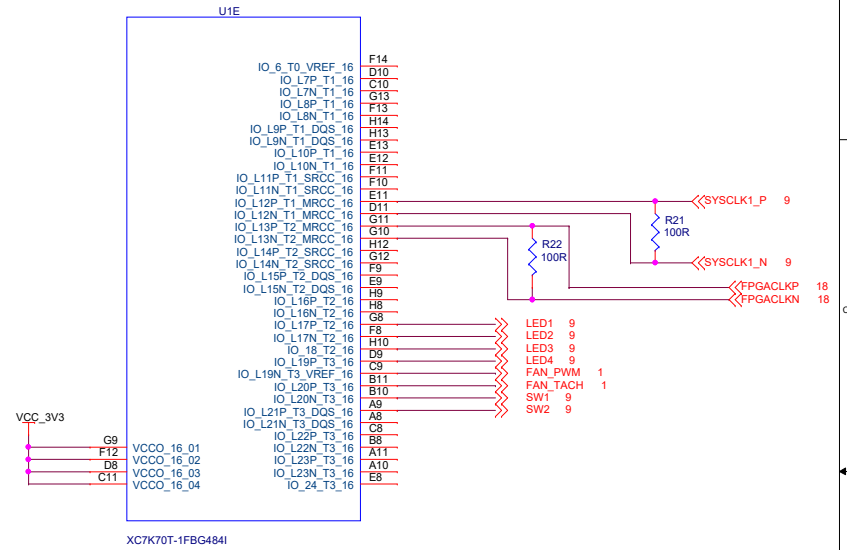
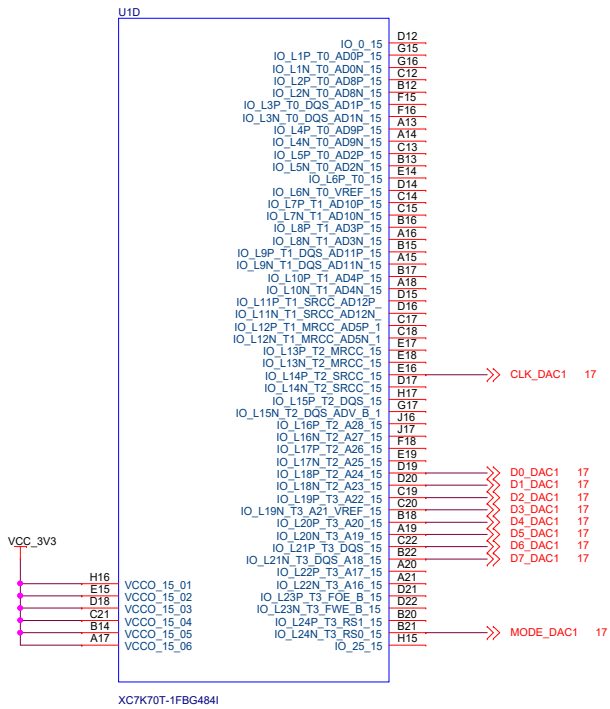


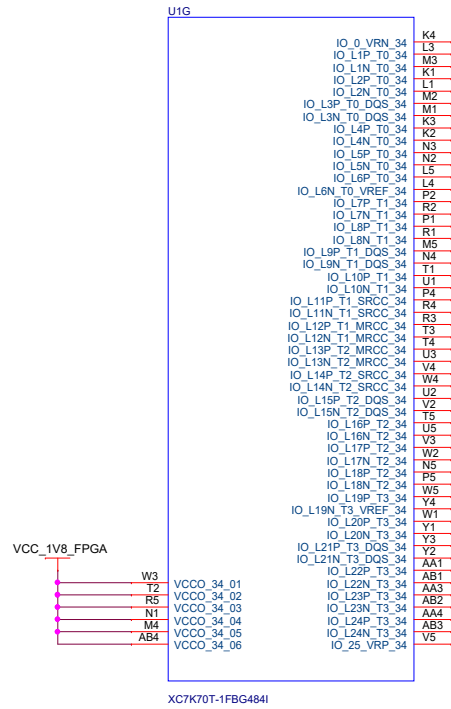
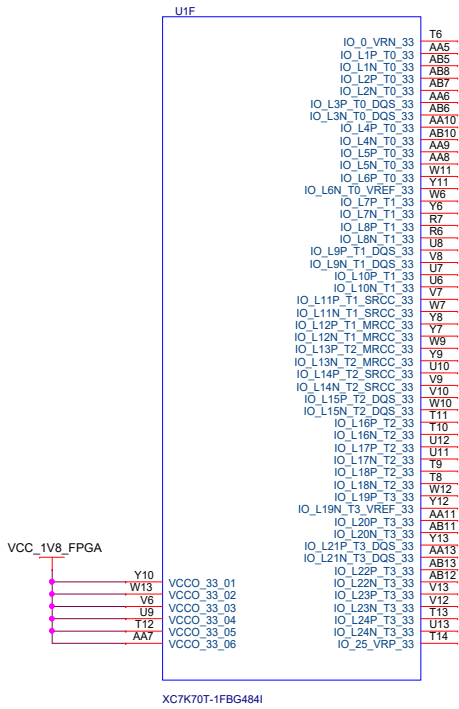
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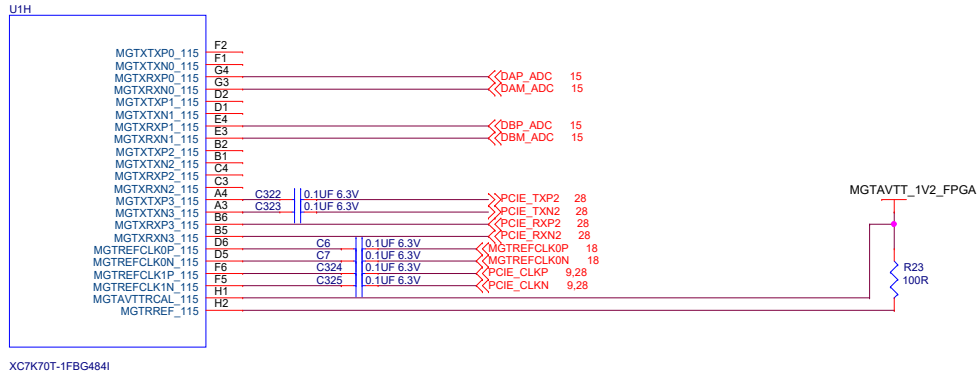
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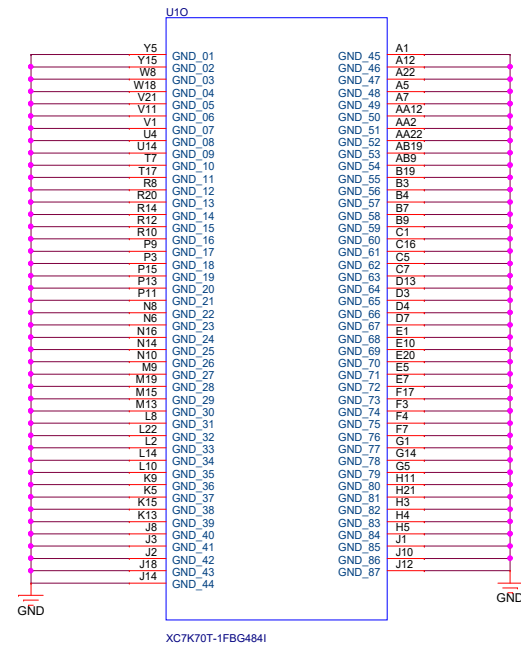
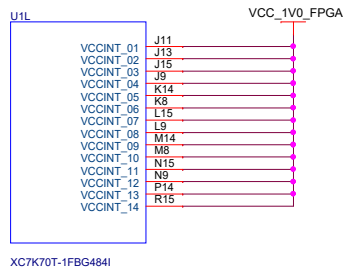
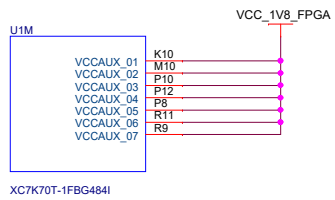
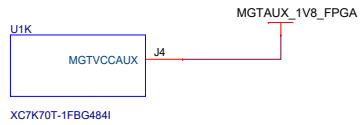
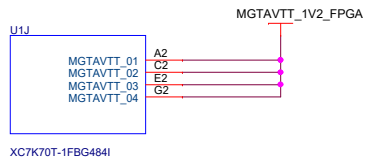
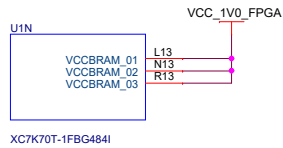
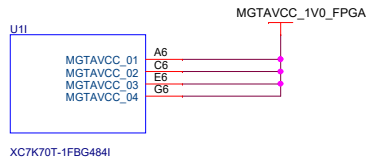
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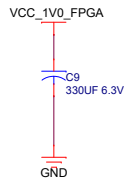
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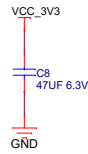
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BYPASS CAPACITORS

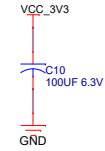
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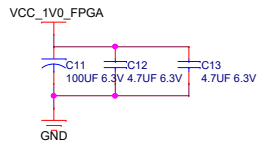
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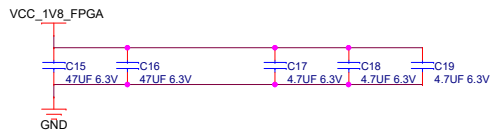
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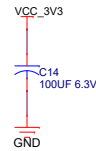
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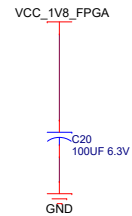
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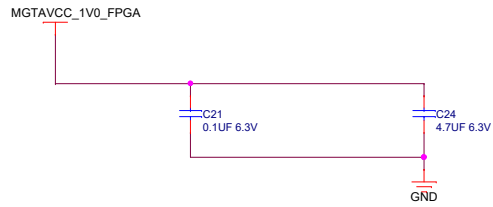
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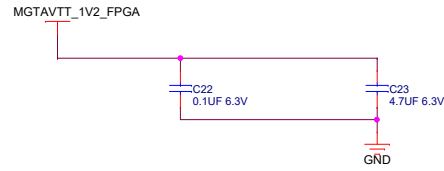
FPGA Bypass Capacitors

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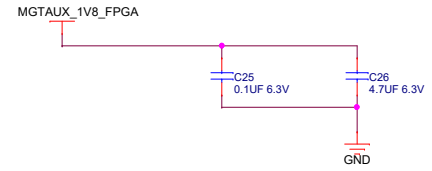
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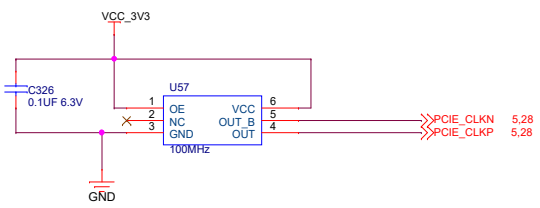
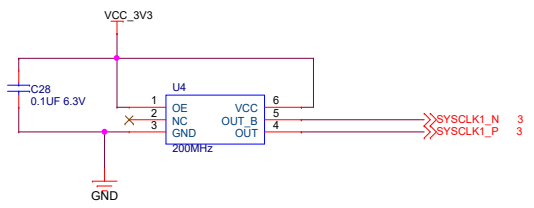


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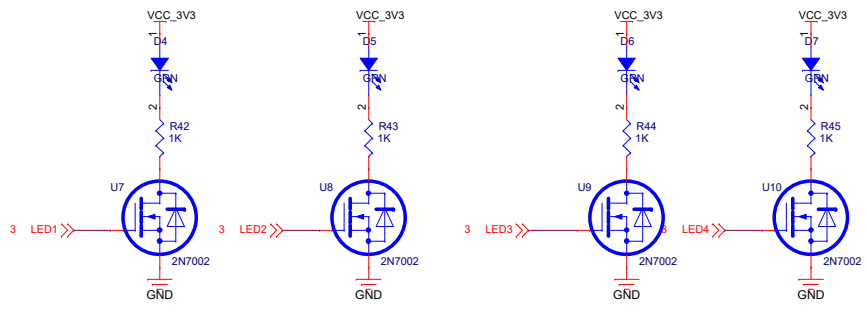
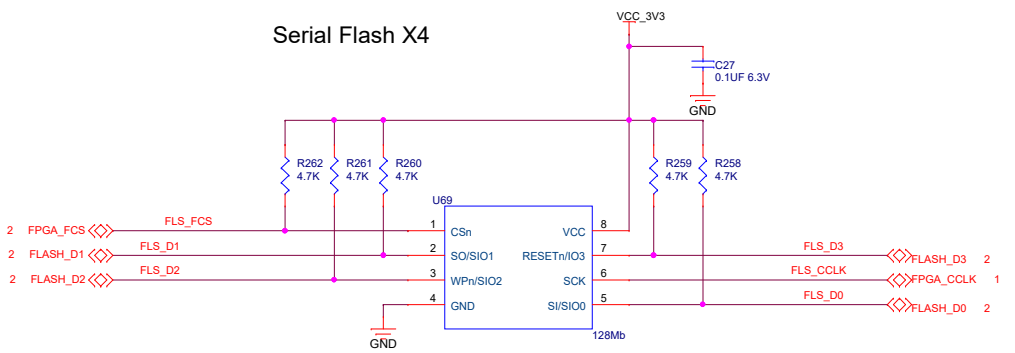


FPGA MGT Bypass Capacitors

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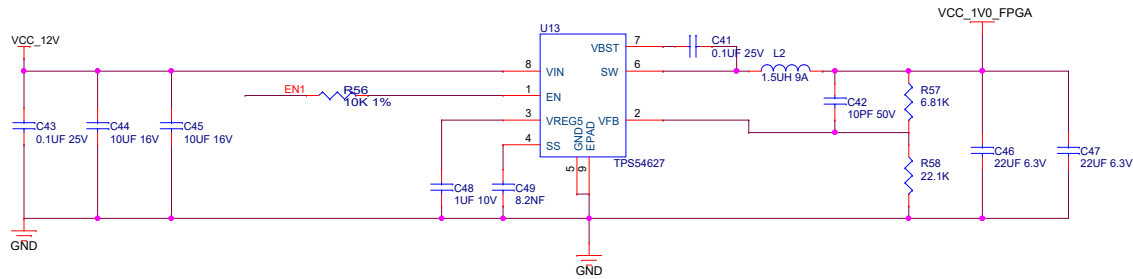
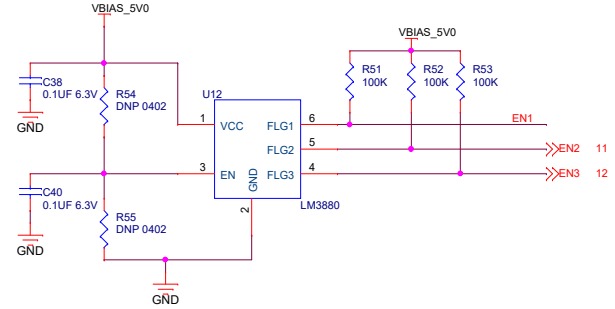
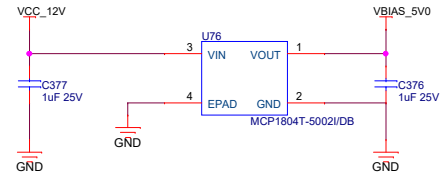
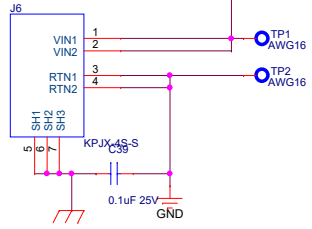
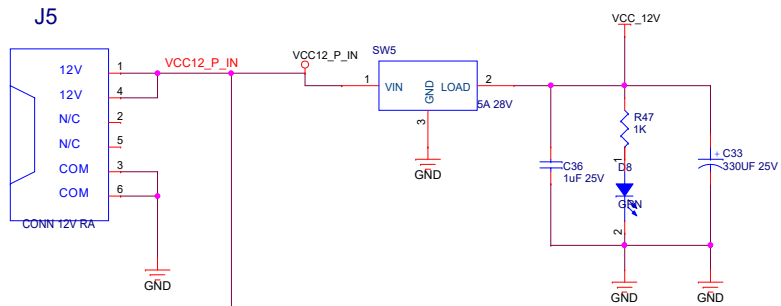


Serial Flash X4

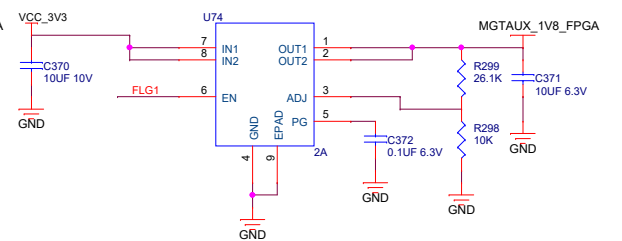
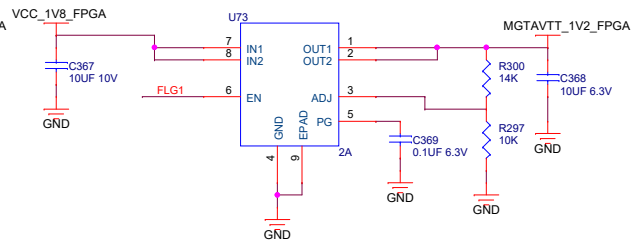
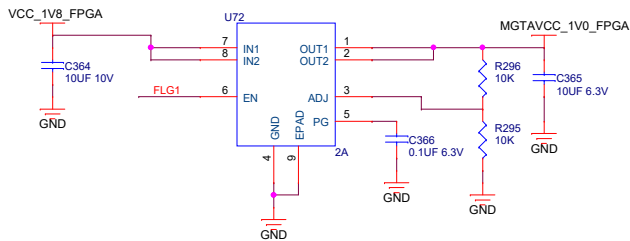
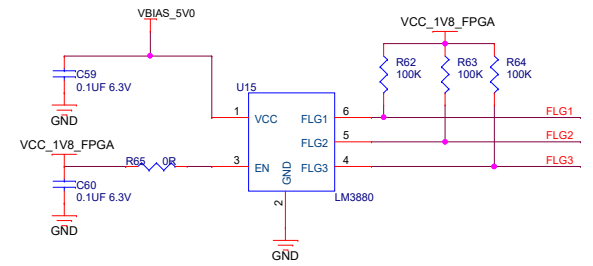
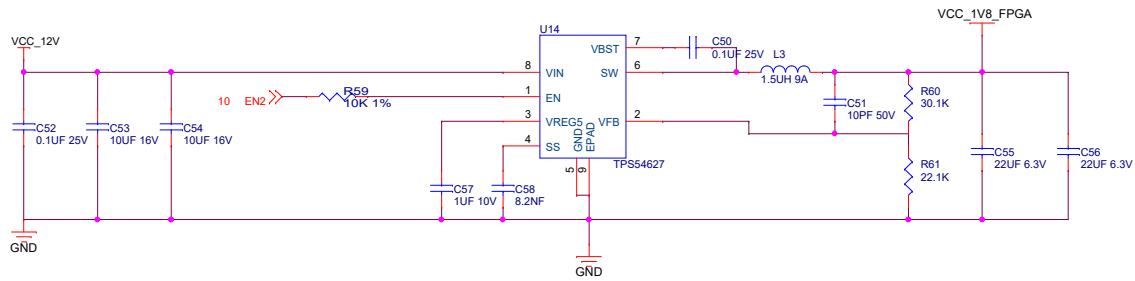


FPGA JTAG, Clock, Flash, Buttons

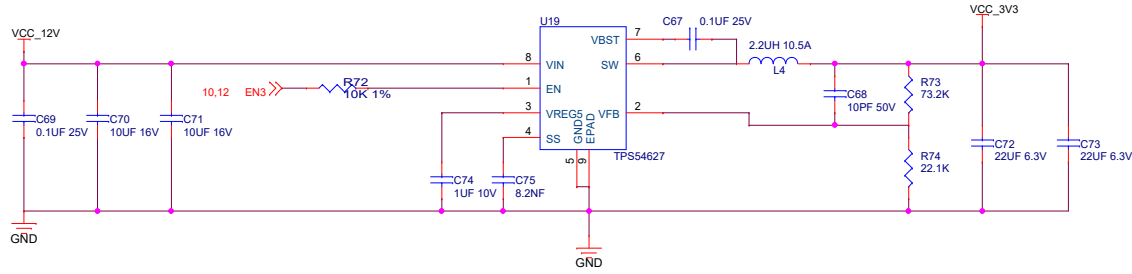
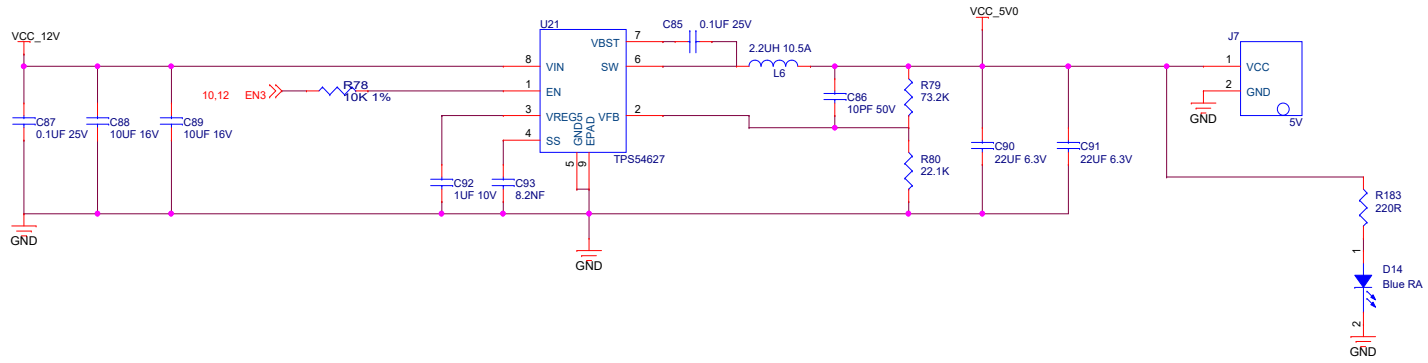
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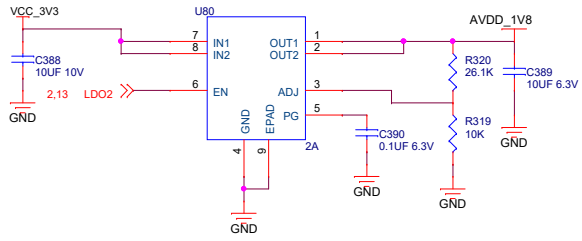
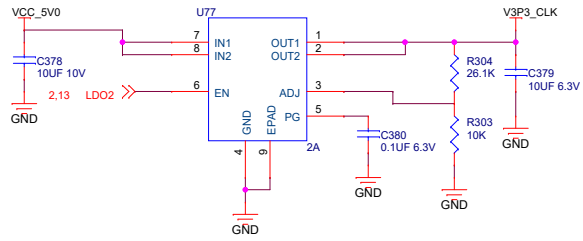
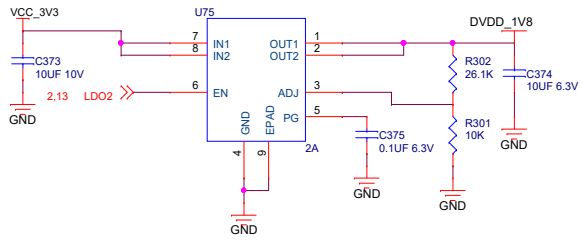
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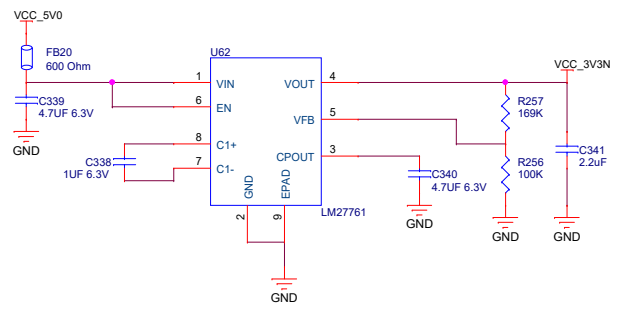
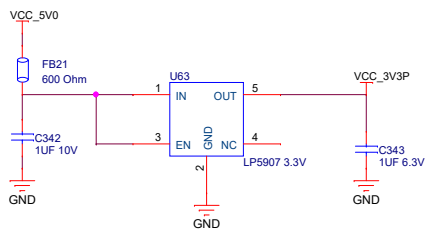
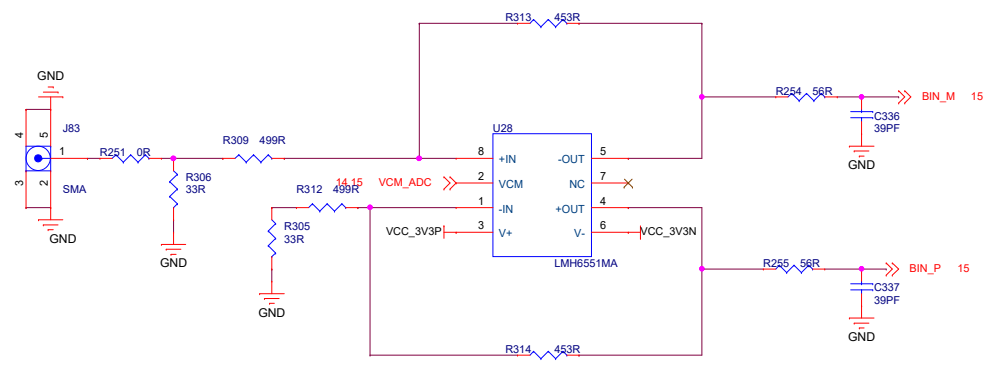
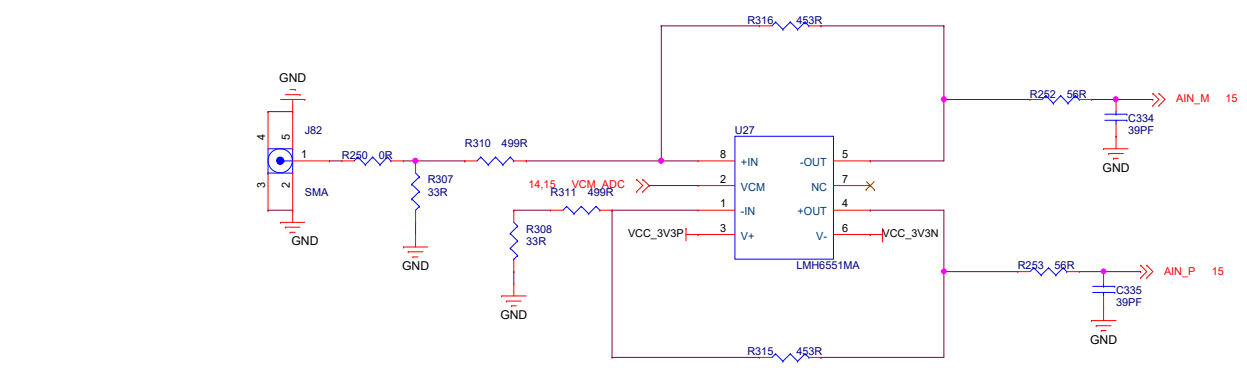
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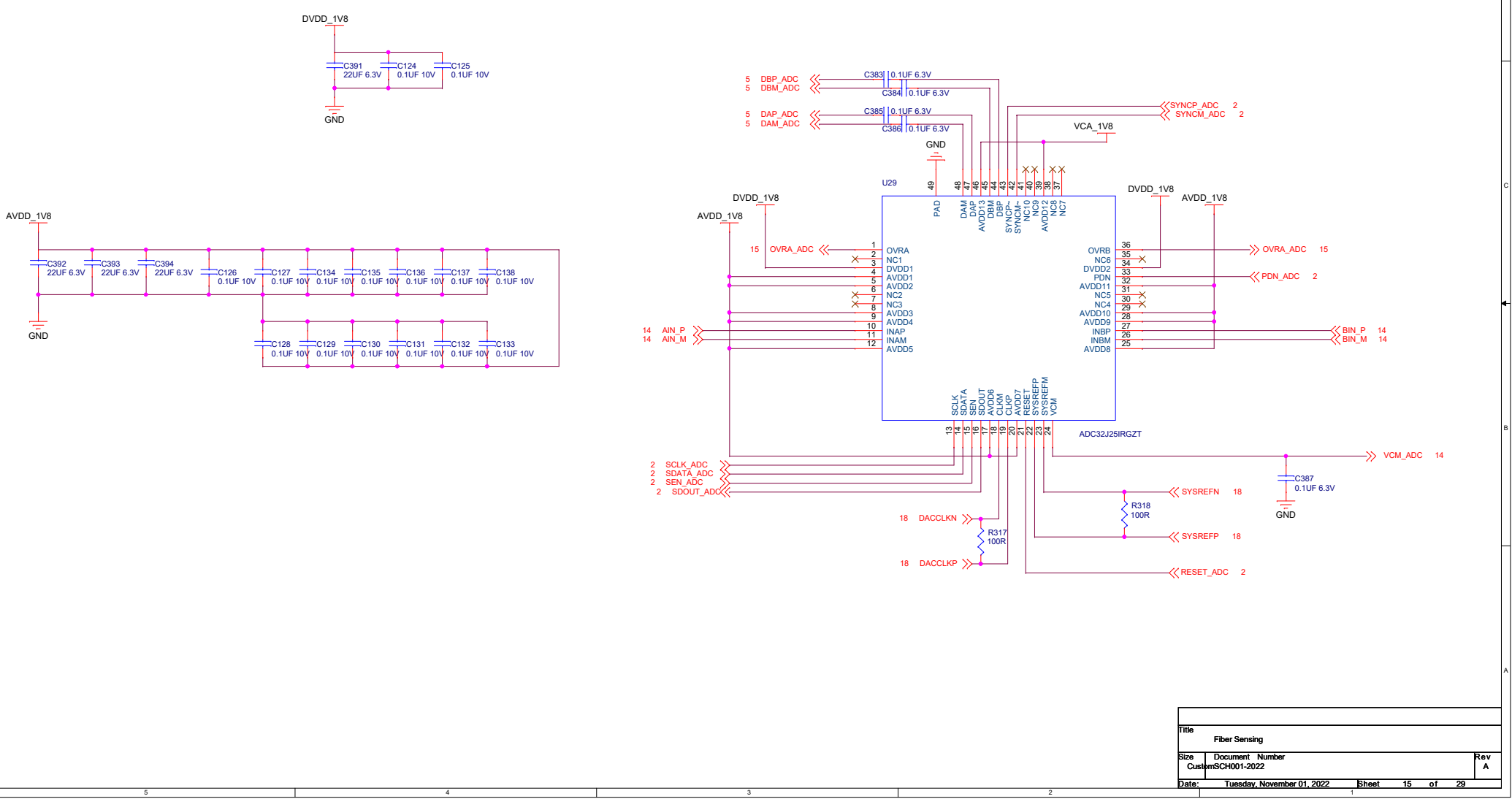
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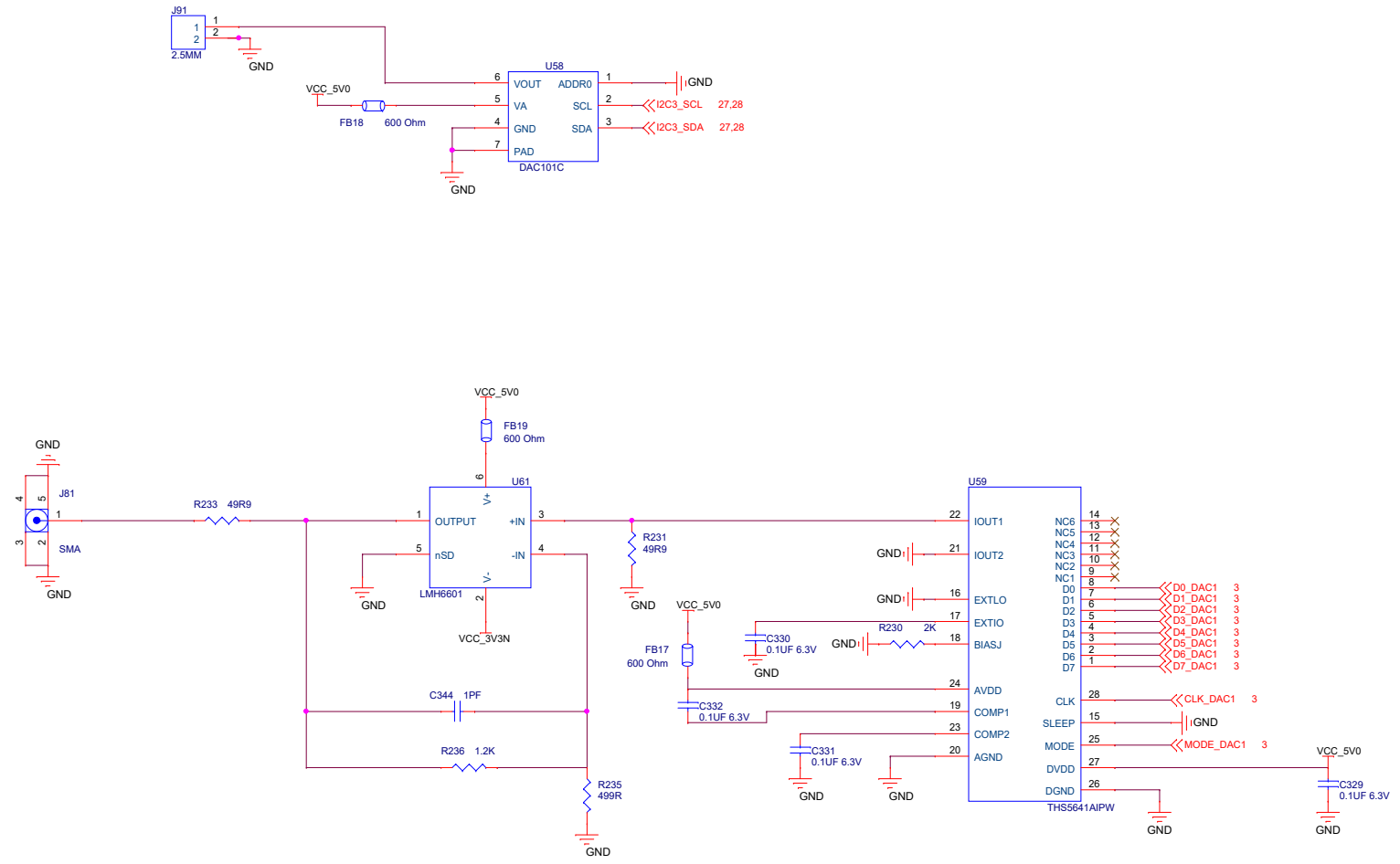
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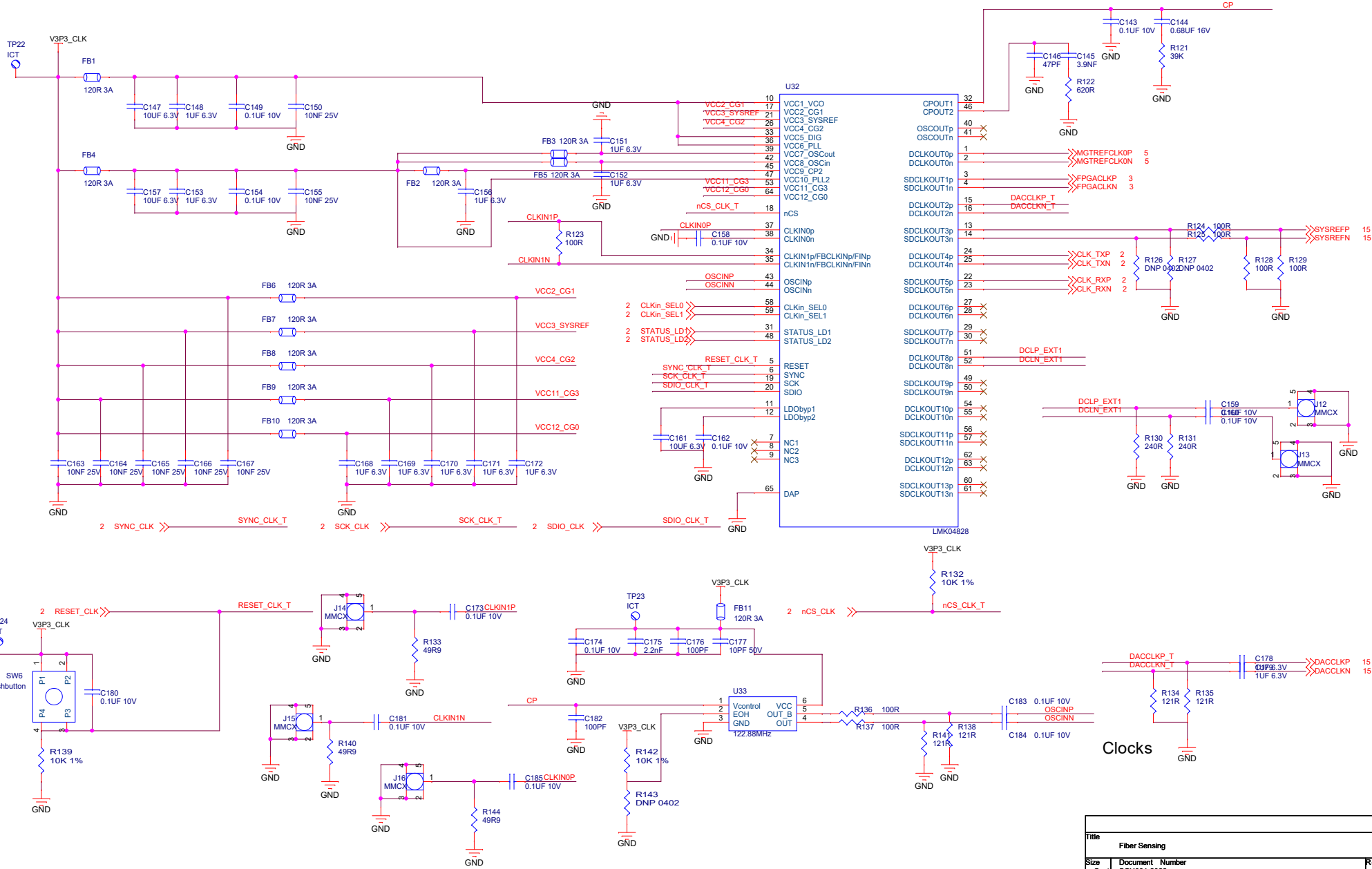
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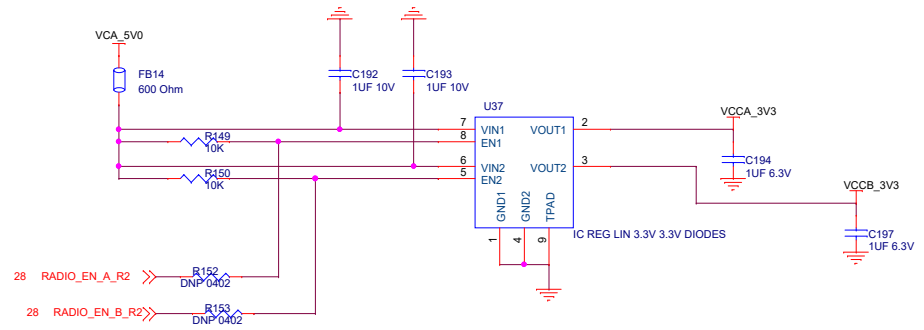
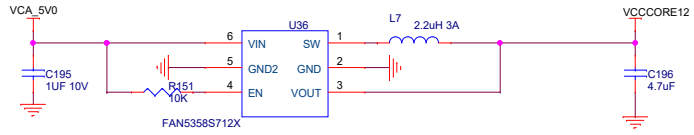
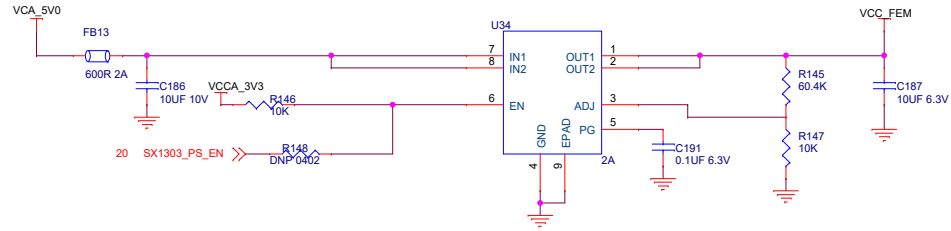
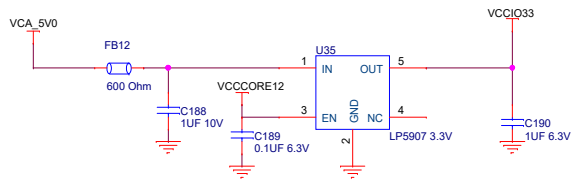


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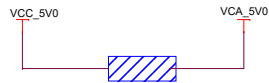


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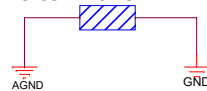
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**HOW TO CONNECT gnd TO AGND2?
VIA STICING?
CONNECT POWER PLANE?**

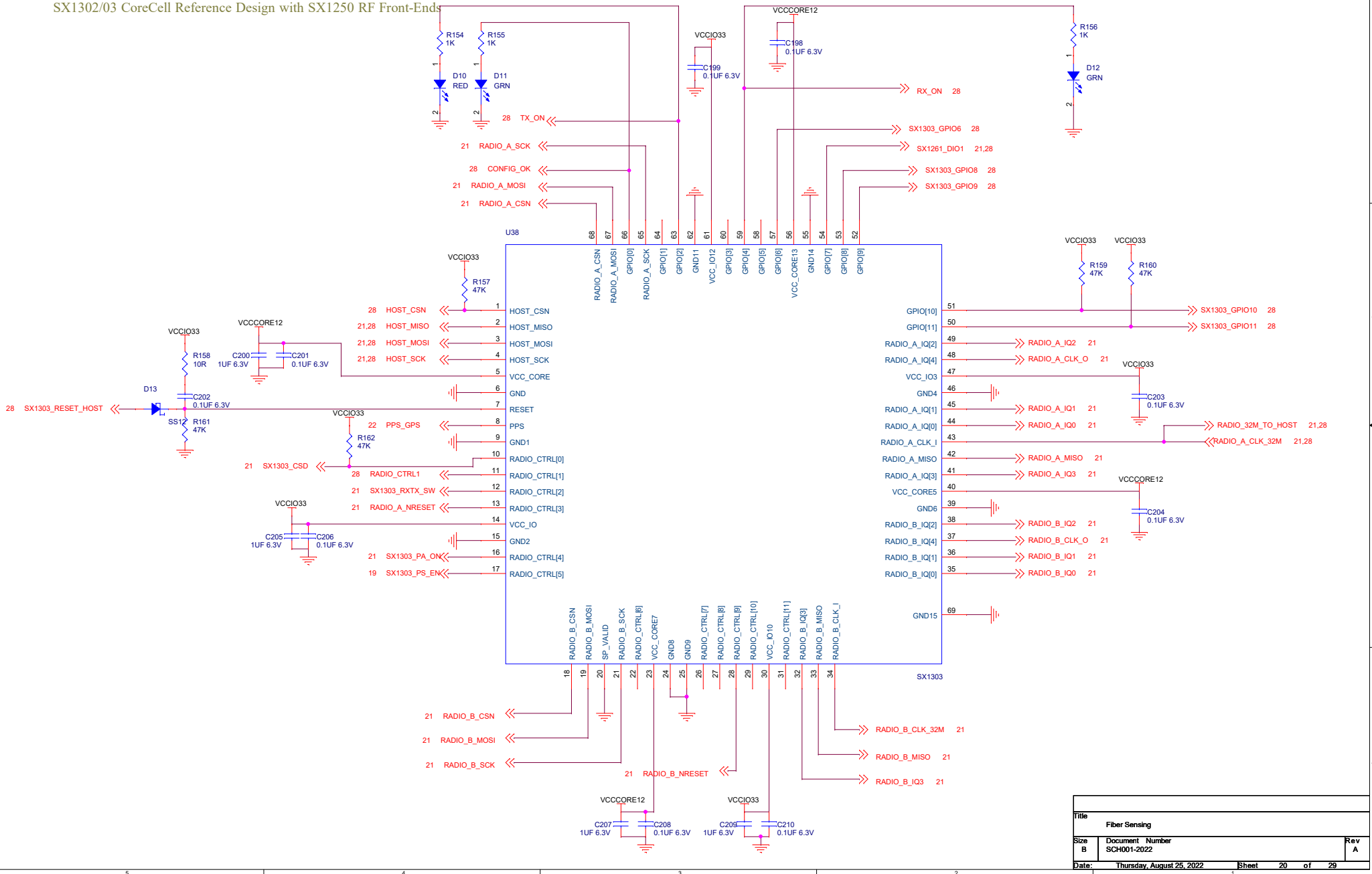


FORCE TO CONNECT GND AND AGND2



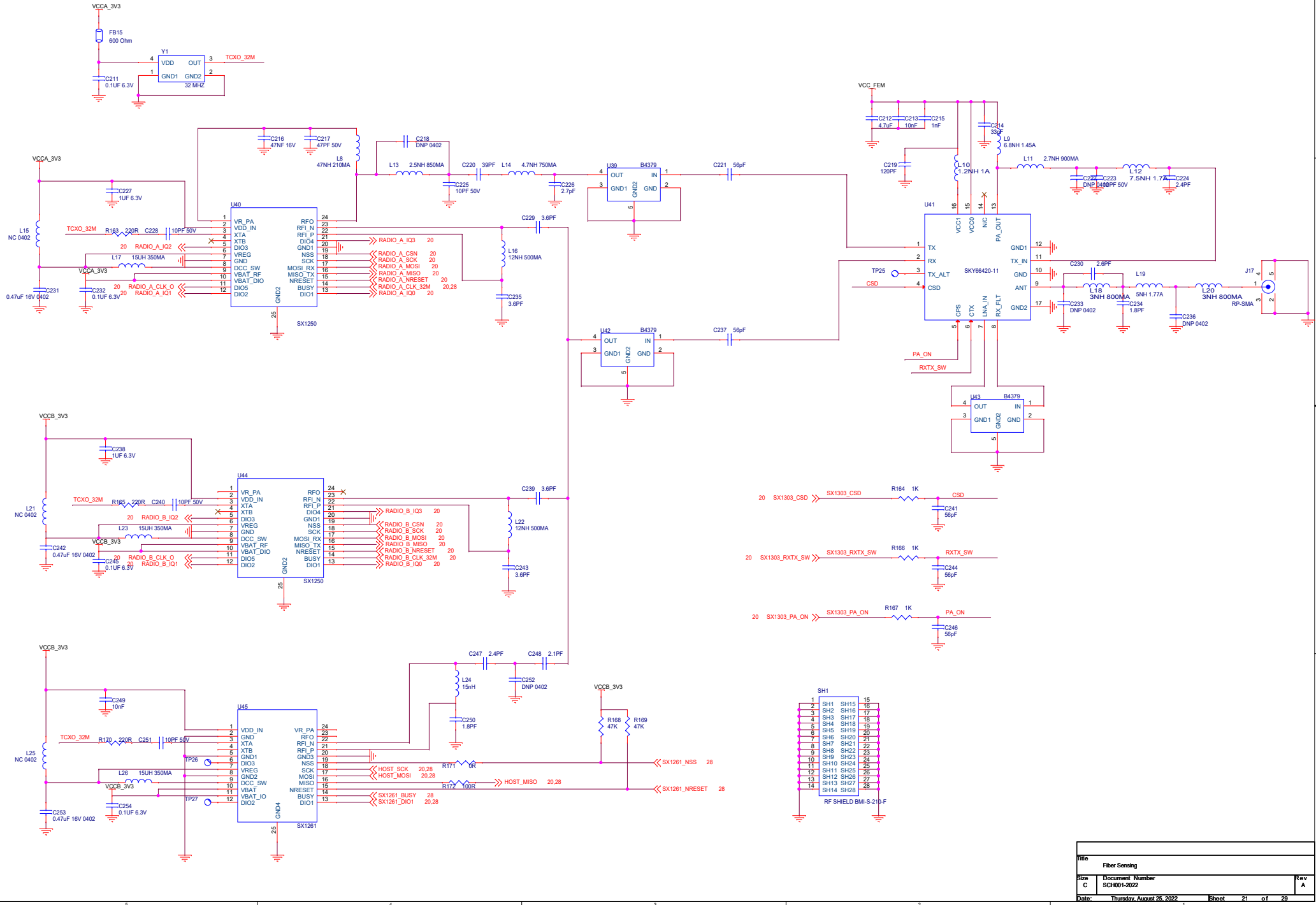
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SX1302/03 CoreCell Reference Design with SX1250 RF Front-Ends

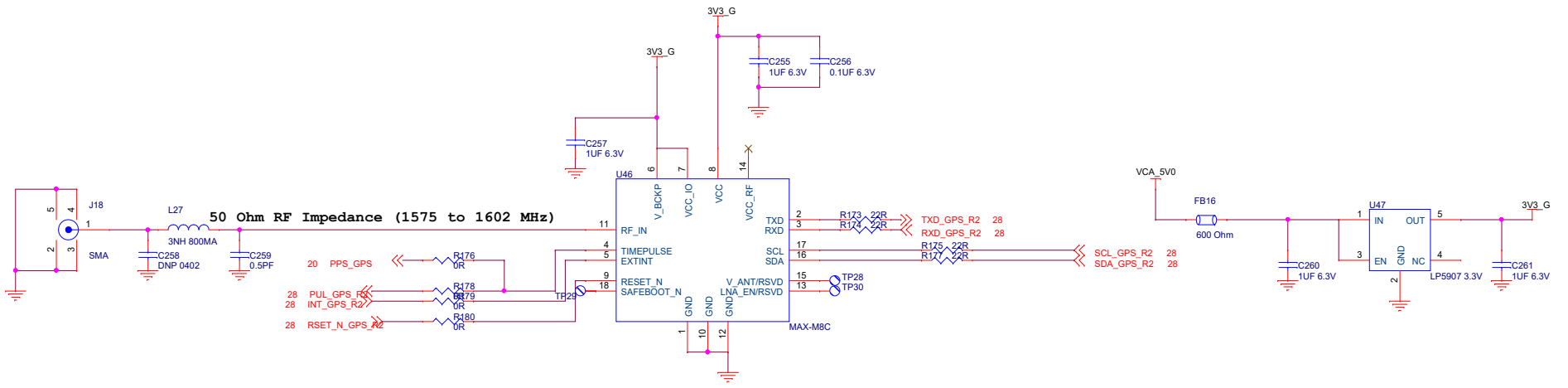


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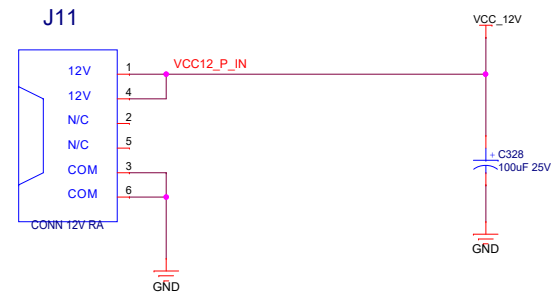
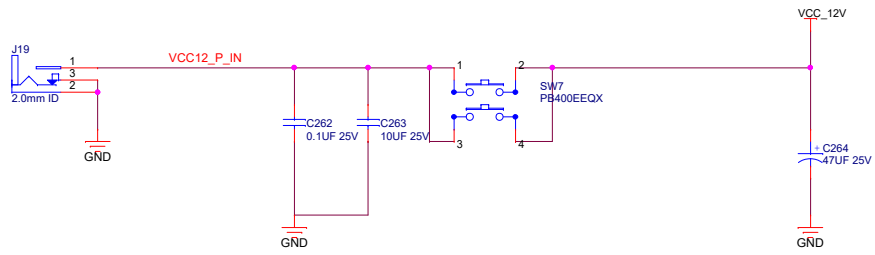
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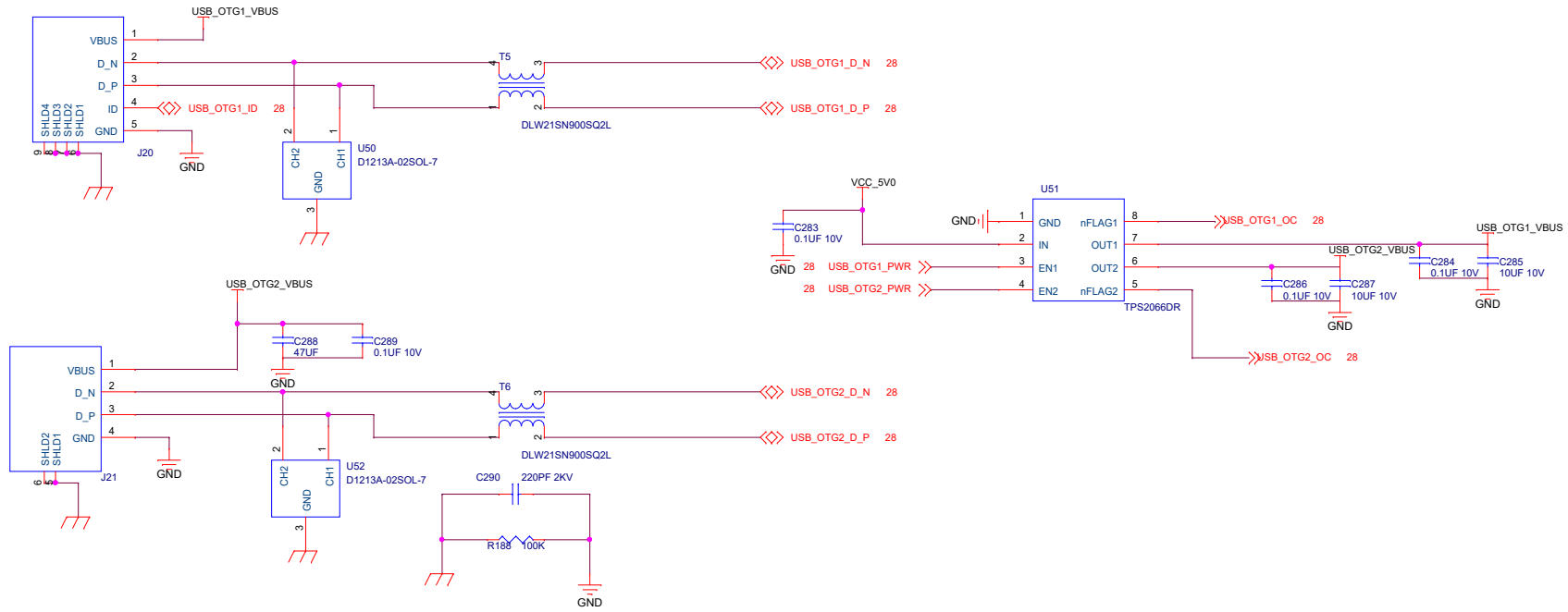
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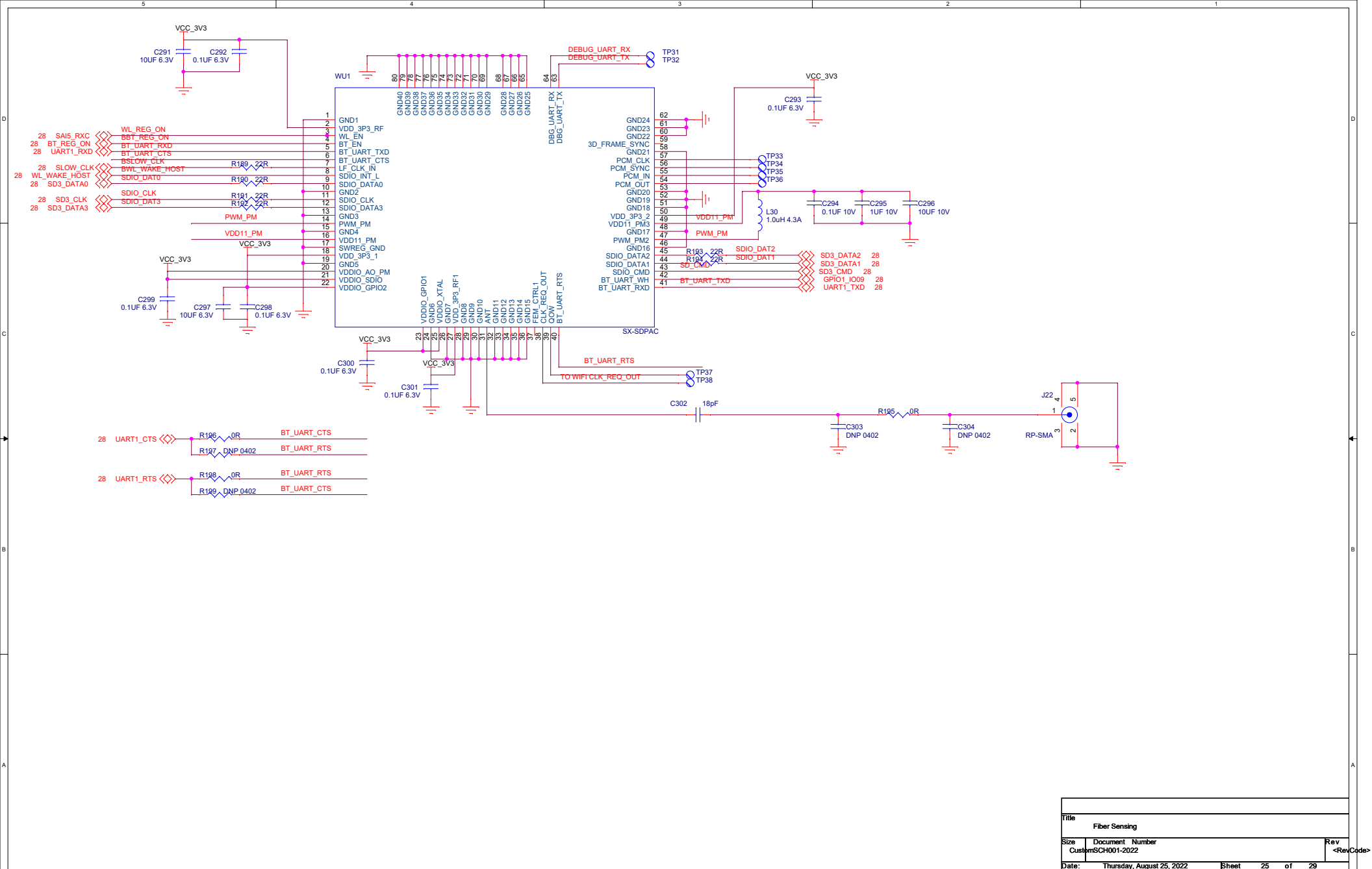
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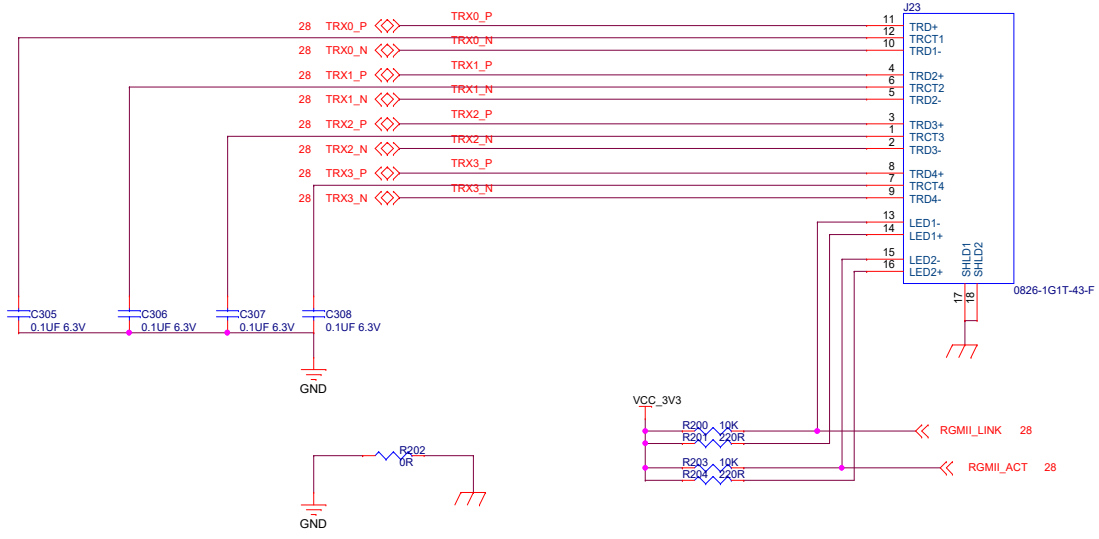
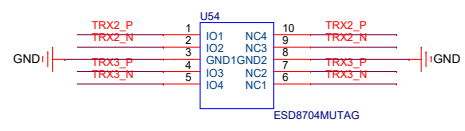
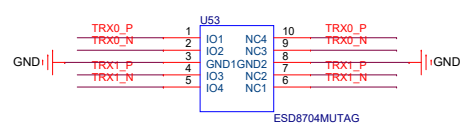
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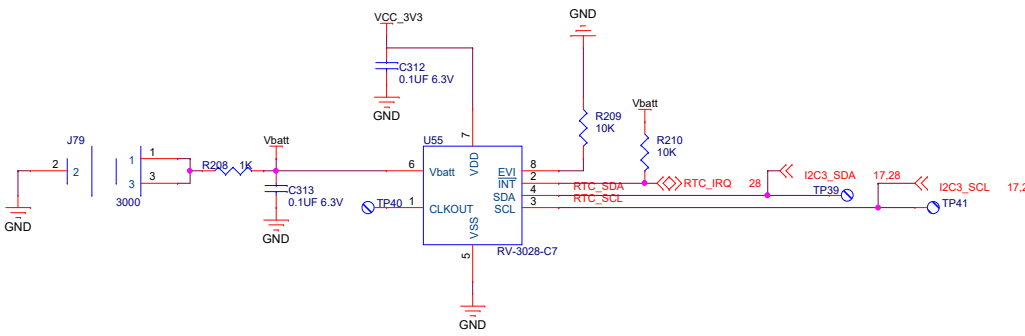
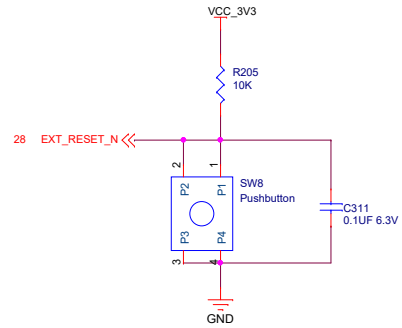
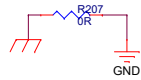
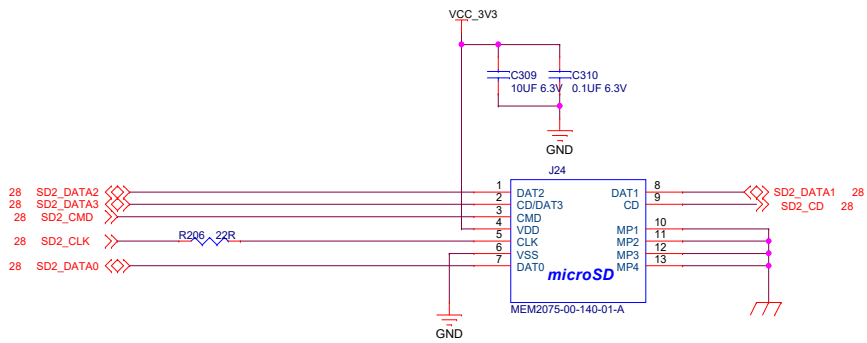
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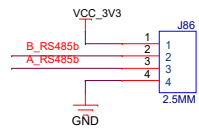
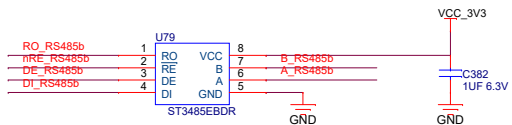
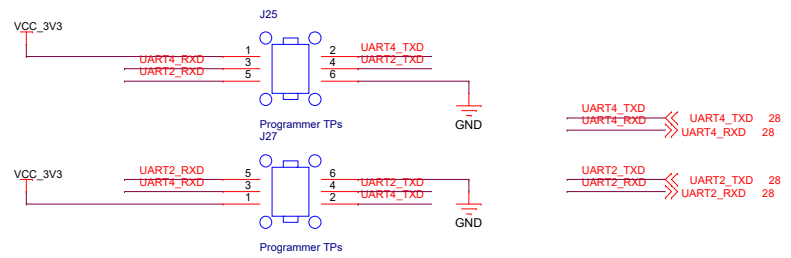
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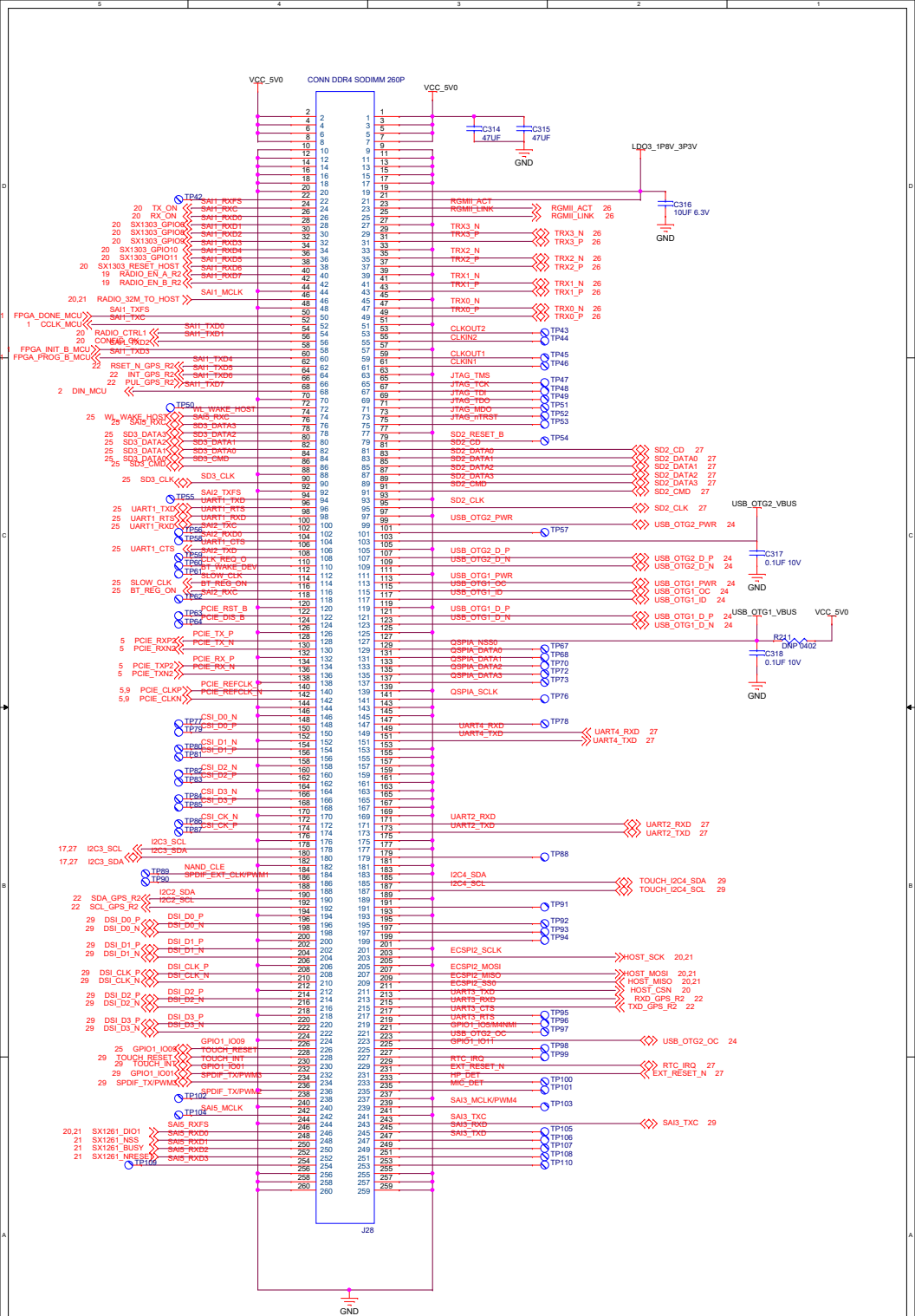
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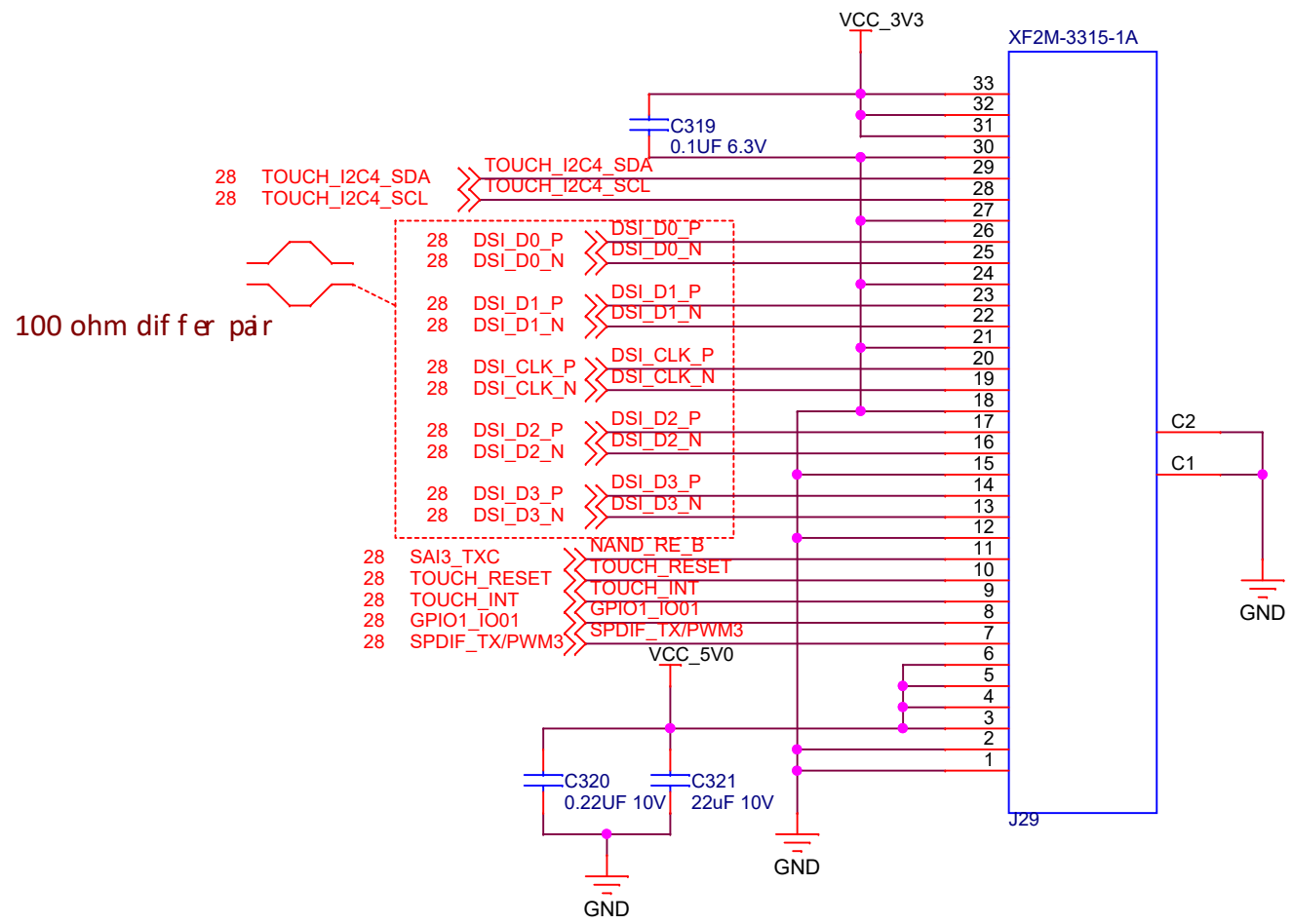


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