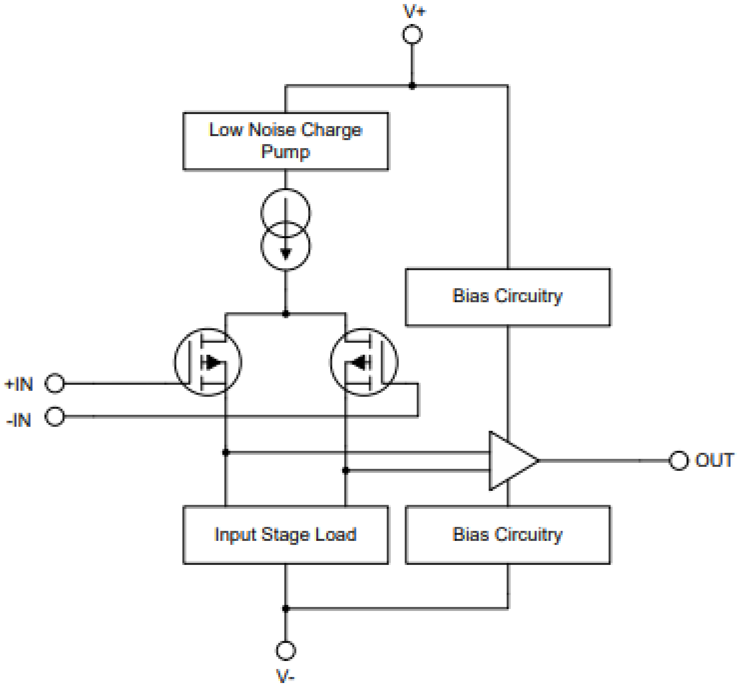
FIT Rate, Failure Mode Distribution
OPA2322AQDGKRQ1

20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier



Failure Rate Mission Profile (1)	Per 10^9 Hours (FIT)
Total FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

FIT Siemens Norm SN29500 (2)

Table	Category	Ref FIT λ_{ref}	Ref Virtual Tj $\theta_{vj,1}$
4	CMOS Operational Amp, Comparators and Voltage monitors	12 FIT	55 C

Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	15%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification	30%
Short circuit any two pins	5%

(1)Failure Rate, Mission Profile and Failure Mode Distribution

The failure rate and mission profile information comes from the Reliability data handbook IEC TR 62380 using reliability modeling for Integrated circuits.
Mission Profile Automotive Control IEC TR 62380
Power dissipation 20mW
Climate type: World-wide Table 8 IEC TR 62380
Package factor lambda 3 Table 17b IEC TR 62380
Substrate Material: FR4
EOS FIT rate assumed = 0

(2) Reference failure rate, Virtual (equivalent) junction temperature

The reference failure rate and virtual junction temperature come from Siemens Norm SN29500-2 tables 1-5. Failure rate under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN29500-2 section 4.

The failure mode distribution estimation comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment. The failure rates listed reflect random failure events and do not include failures due to misuse or over stress.

OPA2322-Q1 was developed using a quality-managed development process but was not developed in accordance with the ISO 26262 standards.

(3) Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the OPA2322-Q1 (VSSOP-8 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

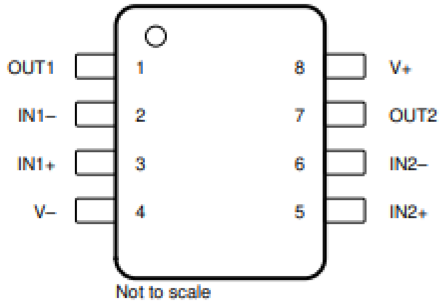
- Pin short-circuited to (V-)
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to (V+)

Tables below indicate how the pin conditions can affect the device as per the following classification of failure effects

Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

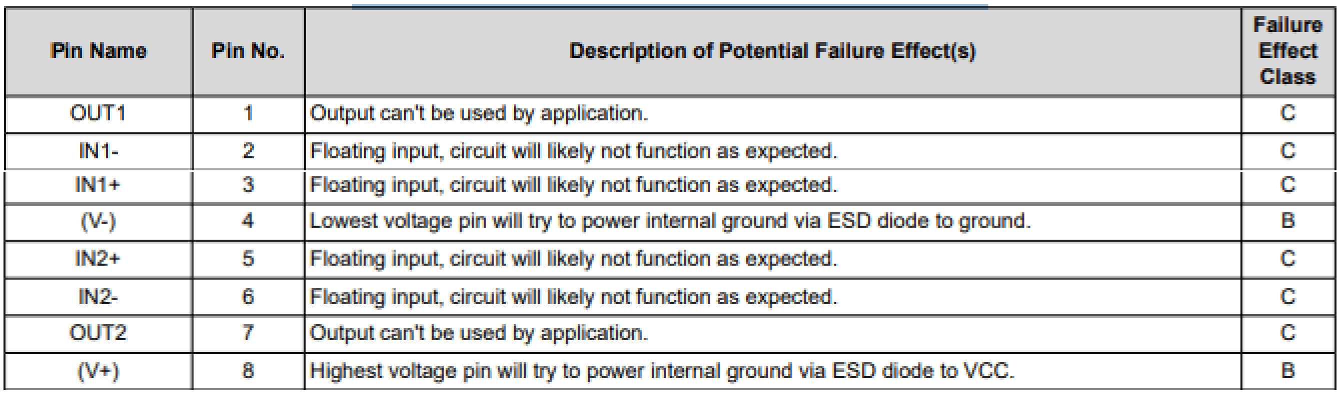
Figure below shows the OPA2322-Q1 pin diagram for the VSSOP (8) package. For a detailed description of the device pins, please refer to the 'Pin Configuration and Functions' section in the OPA2322-Q1 data sheet.



Pin FMA for Device Pins Short-Circuited to (V-) Pin

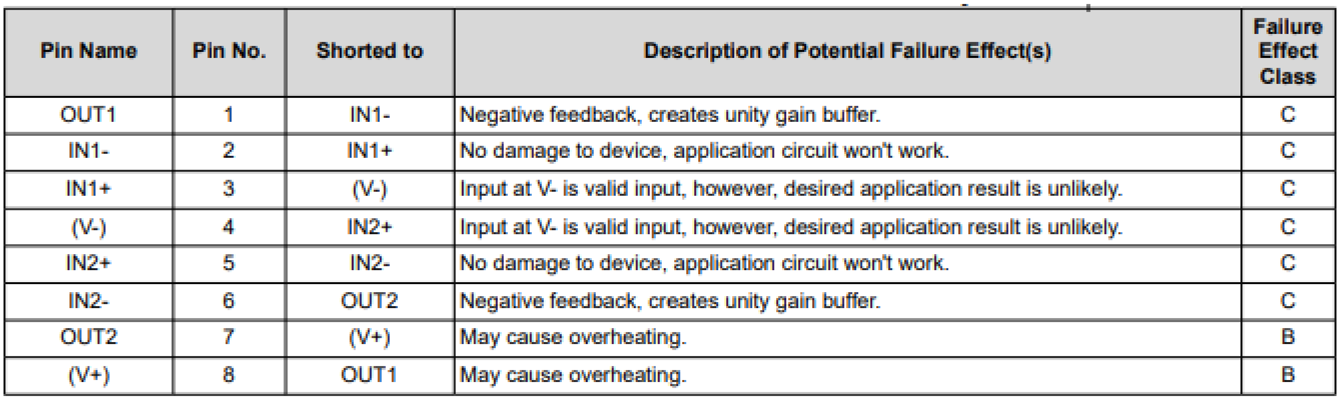
Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V- is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V- is valid input, however, desired application result is unlikely.	C
(V-)	4	Normal operation.	D
IN2+	5	Input at V- is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V- is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating due to output short circuit current.	B
(V+)	8	Diodes from input to V+ may turn due to input signal and cause EOS.	B

Pin FMA for Device Pins Open-Circuited



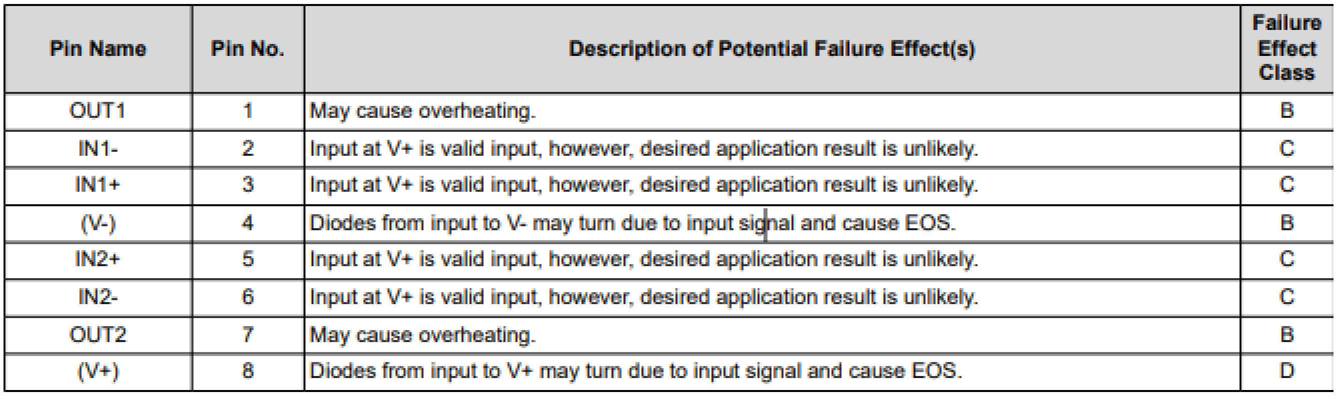
Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can't be used by application.	C
IN1-	2	Floating input, circuit will likely not function as expected.	C
IN1+	3	Floating input, circuit will likely not function as expected.	C
(V-)	4	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
IN2+	5	Floating input, circuit will likely not function as expected.	C
IN2-	6	Floating input, circuit will likely not function as expected.	C
OUT2	7	Output can't be used by application.	C
(V+)	8	Highest voltage pin will try to power internal ground via ESD diode to VCC.	B

Pin FMA for Device Pins Short-Circuited to Adjacent Pin



Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Negative feedback, creates unity gain buffer.	C
IN1-	2	IN1+	No damage to device, application circuit won't work.	C
IN1+	3	(V-)	Input at V- is valid input, however, desired application result is unlikely.	C
(V-)	4	IN2+	Input at V- is valid input, however, desired application result is unlikely.	C
IN2+	5	IN2-	No damage to device, application circuit won't work.	C
IN2-	6	OUT2	Negative feedback, creates unity gain buffer.	C
OUT2	7	(V+)	May cause overheating.	B
(V+)	8	OUT1	May cause overheating.	B

Pin FMA for Device Pins Short-Circuited to (V+)



Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause overheating.	B
IN1-	2	Input at V+ is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V+ is valid input, however, desired application result is unlikely.	C
(V-)	4	Diodes from input to V- may turn due to input signal and cause EOS.	B
IN2+	5	Input at V+ is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V+ is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause overheating.	B
(V+)	8	Diodes from input to V+ may turn due to input signal and cause EOS.	D

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