Functional Safety Information

TAS6754-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TAS6754-Q1 (56-pin DKQ package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

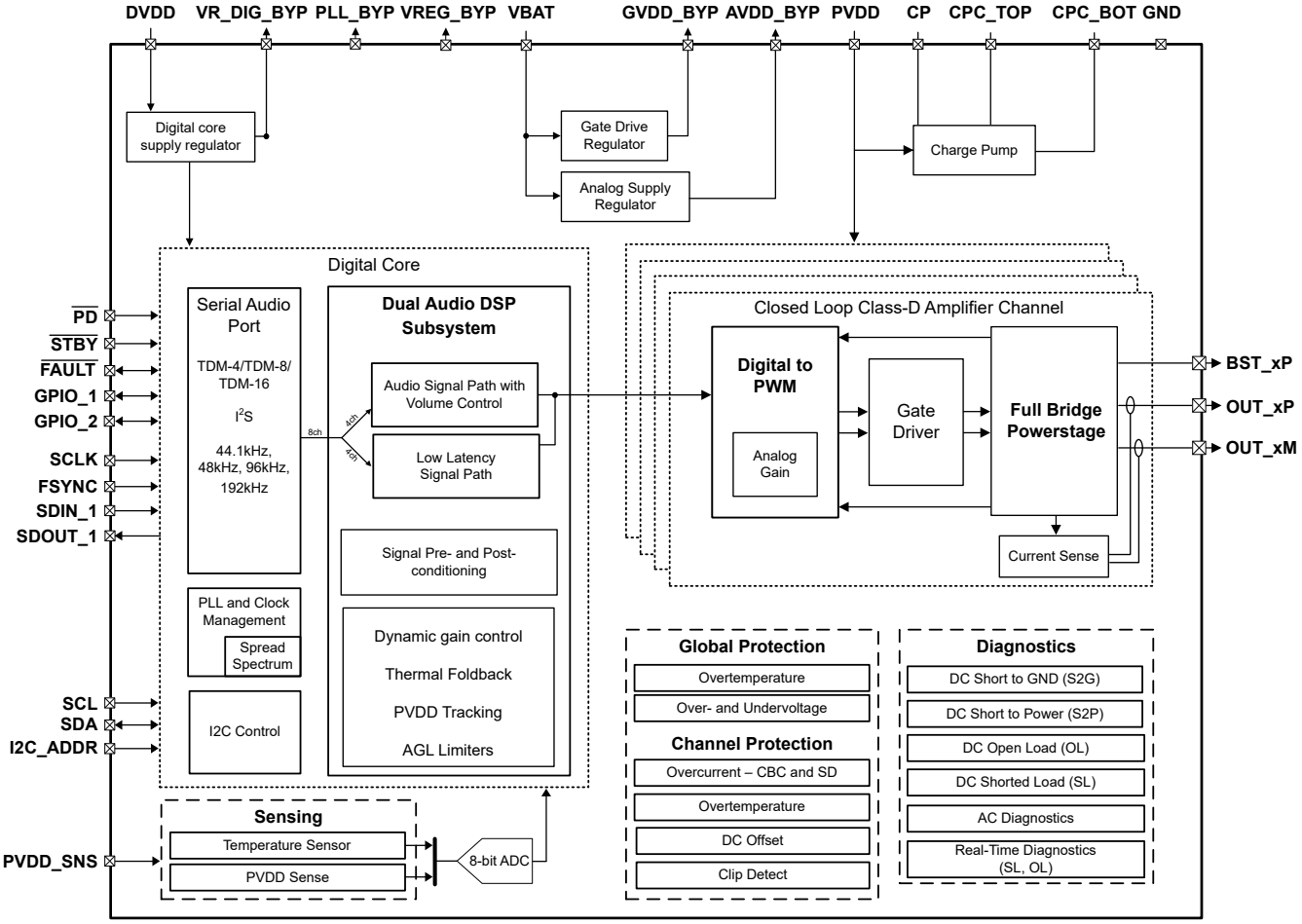

Figure 1-1. Functional Block Diagram

The TAS6754-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TAS6754-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	55
Die FIT rate	3
Package FIT rate	52

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 4550mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed ≤50V supply	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TAS6754-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Safe failure modes	50
Unsafe failure modes	50

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TAS6754-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to PVDD (see Table 4-5)
- Pin short-circuited to VBAT (see Table 4-6)
- Pin short-circuited to DVDD (see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TAS6754-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TAS6754-Q1 data sheet.

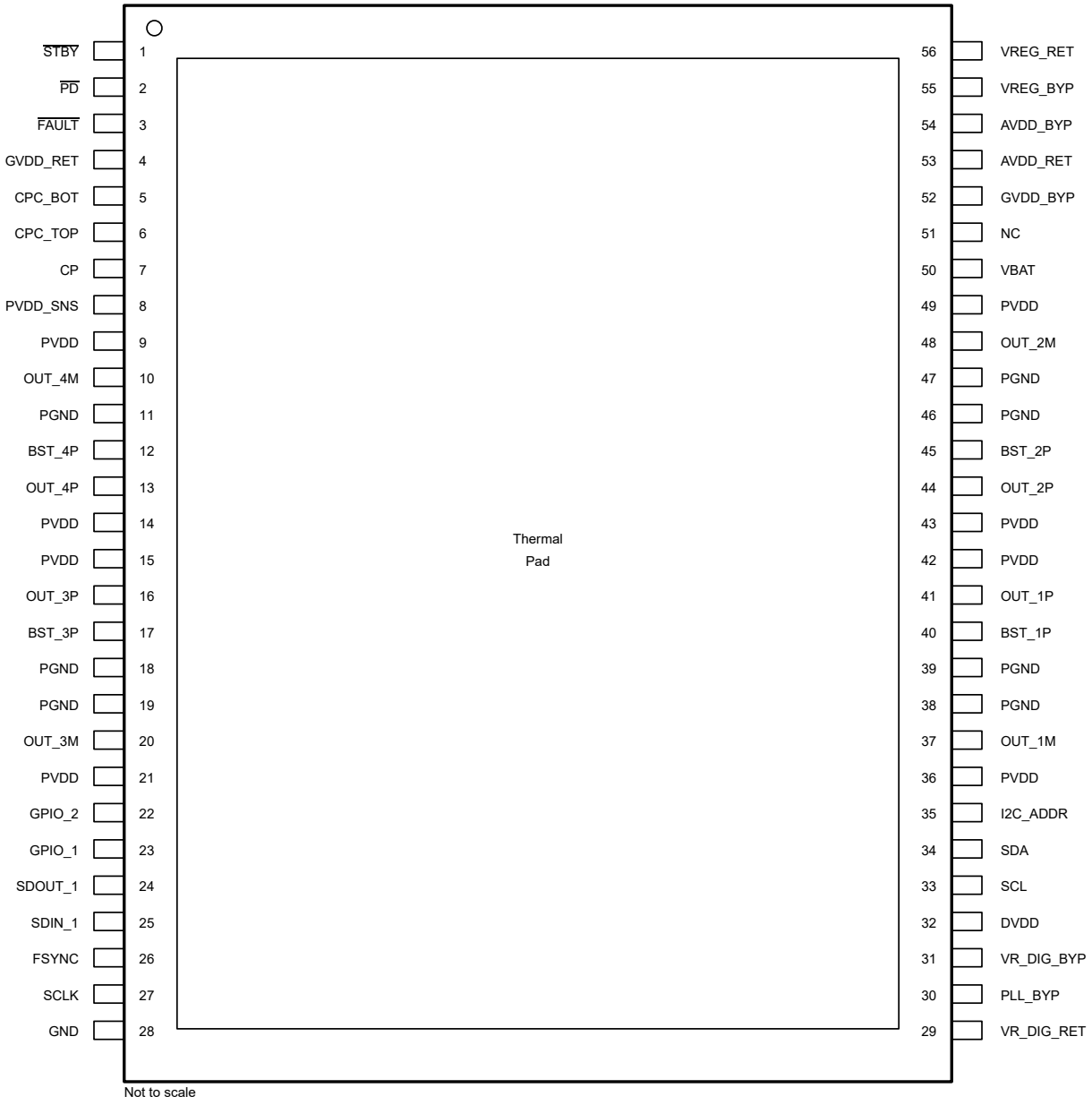

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_C = 25°C
- PVDD = 4.5V - 19V
- VBAT = 14.4V
- DVDD = 1.8V - 3.3V
- R_L = 4Ω
- P_{OUT} = 1W, *f* = 1kHz
- f_{SW} = 2.048MHz
- AES17 filter, default I2C settings
- Output channels in PLAY mode

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	Device shuts down.	B
/PD	2	Device shuts down.	B
/FAULT	3	FAULT cannot assert correctly, can affect system MCU.	B
GVDD_RET	4	No impact.	D
CPC_BOT	5	Reports a charge pump fault.	B
CPC_TOP	6	Device can be damaged.	A
CP	7	Device can be damaged.	A
PVDD_SNS	8	Undervoltage protection enables. Device shuts down.	B
PVDD	9	Undervoltage protection enables. Device shuts down.	B
OUT_4M	10	Output overcurrent protection. Device shuts down. Fault latches.	B
PGND	11	No impact.	D
BST_4P	12	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
OUT_4P	13	Output overcurrent protection. Device shuts down. Fault latches.	B
PVDD	14	Undervoltage protection enables. Device shuts down.	B
PVDD	15	Undervoltage protection enables. Device shuts down.	B
OUT_3P	16	Output overcurrent protection. Device shuts down. Fault latches.	B
BST_3P	17	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
PGND	18	No impact.	D
PGND	19	No impact.	D
OUT_3M	20	Output overcurrent protection. Device shuts down. Fault latches.	B
PVDD	21	Undervoltage protection enables. Device shuts down.	B
GPIO_2	22	Device can be damaged when GPIO is high.	A
GPIO_1	23	Device can be damaged when GPIO is high.	A
SDOUT_1	24	Device can be damaged when SDOUT is high.	A
SDIN_1	25	Input audio is wrong. Under certain configurations, device can heat up.	B
FSYNC	26	Reports a clock error.	B
SCLK	27	Reports a clock error.	B
GND	28	No impact.	D
VR_DIG_RET	29	No impact.	D
PLL_BYP	30	Clock error, device shuts down.	B
VR_DIG_BYP	31	Undervoltage protection enables.	B
DVDD	32	Undervoltage protection enables.	B
SCL	33	I2C interface does not work.	B
SDA	34	I2C interface does not work.	B
I2C_ADDR	35	I2C address can be affected. Device can lose I2C connection.	B
PVDD	36	Undervoltage protection enables. Device shuts down.	B
OUT_1M	37	Output overcurrent protection. Device shuts down. Fault latches.	B
PGND	38	No impact.	D
PGND	39	No impact.	D
BST_1P	40	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
OUT_1P	41	Output overcurrent protection. Device shuts down. Fault latches.	B
PVDD	42	Undervoltage protection enables. Device shuts down.	B
PVDD	43	Undervoltage protection enables. Device shuts down.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT_2P	44	Output overcurrent protection. Device shuts down. Fault latches.	B
BST_2P	45	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
PGND	46	No impact.	D
PGND	47	No impact.	D
OUT_2M	48	Output overcurrent protection. Device shuts down. Fault latches.	B
PVDD	49	Undervoltage protection enables. Device shuts down.	B
VBAT	50	Undervoltage protection enables. Device shuts down.	B
NC	51	No impact.	D
GVDD_BYP	52	Undervoltage protection enables.	B
AVDD_RET	53	No impact.	D
AVDD_BYP	54	Undervoltage protection enables.	B
VREG_BYP	55	Undervoltage protection enables.	B
VREG_RET	56	No impact.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	Internal pulldown resistor places the device in standby.	B
/PD	2	Internal pulldown resistor powers down the device.	B
/FAULT	3	FAULT cannot be reported to the system.	B
GVDD_RET	4	Performance can degrade due to lack of external decoupling capacitor.	C
CPC_BOT	5	Charge pump cannot work.	B
CPC_TOP	6	Charge pump cannot work.	B
CP	7	Performance can degrade due to lack of external decoupling capacitor.	C
PVDD_SNS	8	No power supply, undervoltage protection.	B
PVDD	9	No power supply, undervoltage protection.	B
OUT_4M	10	Open-load condition.	C
PGND	11	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
BST_4P	12	Output cannot be driven to PVDD.	B
OUT_4P	13	Open-load condition.	C
PVDD	14	No power supply, undervoltage protection.	B
PVDD	15	No power supply, undervoltage protection.	B
OUT_3P	16	Open-load condition.	C
BST_3P	17	Output cannot be driven to PVDD.	B
PGND	18	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
PGND	19	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
OUT_3M	20	Open-load condition.	C
PVDD	21	No power supply, undervoltage protection.	B
GPIO_2	22	No output.	B
GPIO_1	23	No output.	B
SDOUT_1	24	No output.	B
SDIN_1	25	No input audio signal.	B
FSYNC	26	Reports clock error.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SCLK	27	Reports a clock error.	B
GND	28	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
VR_DIG_RET	29	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
PLL_BYP	30	Clock error, device shuts down.	C
VR_DIG_BYP	31	Performance can degrade due to a lack of external decoupling capacitor.	C
DVDD	32	No power supply, device does not start up.	B
SCL	33	Device does not respond to I2C command.	B
SDA	34	Device does not respond to I2C command.	B
I2C_ADDR	35	Device I2C address can be wrong.	B
PVDD	36	No power supply, device does not start up.	B
OUT_1M	37	Open-load condition.	C
PGND	38	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
PGND	39	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
BST_1P	40	Output cannot be driven to PVDD.	B
OUT_1P	41	Open-load condition.	C
PVDD	42	No power supply, undervoltage protection.	B
PVDD	43	No power supply, undervoltage protection.	B
OUT_2P	44	Open-load condition.	C
BST_2P	45	Output cannot be driven to PVDD.	B
PGND	46	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
PGND	47	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
OUT_2M	48	Open-load condition.	B
PVDD	49	No power supply, undervoltage protection.	B
VBAT	50	No power supply, undervoltage protection.	B
NC	51	No effect.	D
GVDD_BYP	52	Performance can degrade due to a lack of external decoupling capacitor.	C
AVDD_RET	53	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A
AVDD_BYP	54	Performance can degrade due to a lack of external decoupling capacitor.	C
VREG_BYP	55	Performance can degrade due to a lack of external decoupling capacitor.	B
VREG_RET	56	If all GNDs are not connected, the device can be damaged. If only one GND is disconnected, the device is functional but performance can degrade.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	2	Device control signal can conflict.	B
/PD	2	3	Device control signal can conflict.	B
/FAULT	3	4	FAULT cannot assert correctly, can affect the system MCU.	B
GVDD_RET	4	5	Reports a charge pump fault.	B
CPC_BOT	5	6	Reports a charge pump fault.	B
CPC_TOP	6	7	Reports a charge pump fault.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
CP	7	8	Reports a charge pump fault.	B
PVDD_SNS	8	9	No impact.	D
PVDD	9	10	Overcurrent protection triggers.	B
OUT_4M	10	11	Overcurrent protection triggers.	B
PGND	11	12	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
BST_4P	12	13	Overcurrent protection triggers.	B
OUT_4P	13	14	Overcurrent protection triggers.	B
PVDD	14	15	No impact.	D
PVDD	15	16	Overcurrent protection triggers.	B
OUT_3P	16	17	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
BST_3P	17	18	Overcurrent protection triggers.	B
PGND	18	19	No impact.	D
PGND	19	20	Overcurrent protection triggers.	B
OUT_3M	20	21	Overcurrent protection triggers.	B
PVDD	21	22	Device can be damaged.	A
GPIO_2	22	23	Large current occurs if pin voltage is different with adjacent pin.	A
GPIO_1	23	24	Large current occurs if pin voltage is different with adjacent pin.	A
SDOUT_1	24	25	Reports a clock error.	B
SDIN_1	25	26	Reports a clock error.	B
FSYNC	26	27	Reports a clock error.	B
SCLK	27	28	Reports a clock error.	B
GND	28	29	No impact.	D
VR_DIG_RET	29	30	Clock error, device shuts down.	B
PLL_BYP	30	31	No impact.	D
VR_DIG_BYP	31	32	Device can be damaged.	A
DVDD	32	33	Device can be damaged.	A
SCL	33	34	Device does not respond to I2C command.	B
SDA	34	35	Device I2C address can be wrong.	B
I2C_ADDR	35	36	Device can be damaged.	A
PVDD	36	37	Overcurrent protection triggers.	B
OUT_1M	37	38	Overcurrent protection triggers.	B
PGND	38	39	No impact.	D
PGND	39	40	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
BST_1P	40	41	Overcurrent protection triggers.	B
OUT_1P	41	42	Overcurrent protection triggers.	B
PVDD	42	43	No impact.	D
PVDD	43	44	Overcurrent protection triggers.	B
OUT_2P	44	45	Output cannot be driven to logic-1 (PVDD). LDO can heat up and overcurrent protection can trigger.	B
BST_2P	45	46	Overcurrent protection triggers.	B
PGND	46	47	No impact.	D
PGND	47	48	Overcurrent protection triggers.	B
OUT_2M	48	49	Overcurrent protection triggers.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
PVDD	49	50	Undervoltage protection enables. Device shuts down.	B
VBAT	50	51	No impact.	D
NC	51	52	No impact.	D
GVDD_BYP	52	53	No impact.	D
AVDD_RET	53	54	No impact.	D
AVDD_BYP	54	55	No impact.	D
VREG_BYP	55	56	No impact.	D
VREG_RET	56	1	Device shuts down.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	Device can be damaged.	A
/PD	2	Device can be damaged.	A
/FAULT	3	Device can be damaged.	A
GVDD_RET	4	System-level fault. Power short-to-ground.	B
CPC_BOT	5	Device can be damaged.	A
CPC_TOP	6	Device can be damaged.	A
CP	7	Reports a charge pump UVLO fault.	B
PVDD_SNS	8	No impact.	D
PVDD	9	No impact.	D
OUT_4M	10	Overcurrent protection triggers.	B
PGND	11	System-level fault. Power short-to-ground.	B
BST_4P	12	Device can be damaged.	A
OUT_4P	13	Overcurrent protection triggers.	B
PVDD	14	No impact.	D
PVDD	15	No impact.	D
OUT_3P	16	Overcurrent protection triggers.	B
BST_3P	17	Device can be damaged.	A
PGND	18	System-level fault. Power short-to-ground.	B
PGND	19	System-level fault. Power short-to-ground.	B
OUT_3M	20	Overcurrent protection triggers.	B
PVDD	21	No impact.	D
GPIO_2	22	Device can be damaged.	A
GPIO_1	23	Device can be damaged.	A
SDOUT_1	24	Device can be damaged.	A
SDIN_1	25	Device can be damaged.	A
FSYNC	26	Device can be damaged.	A
SCLK	27	Device can be damaged.	A
GND	28	System-level fault. Power short-to-ground.	B
VR_DIG_RET	29	System-level fault. Power short-to-ground.	B
PLL_BYP	30	Device can be damaged.	A
VR_DIG_BYP	31	Device can be damaged.	A
DVDD	32	Device can be damaged.	A
SCL	33	Device can be damaged.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SDA	34	Device can be damaged.	A
I2C_ADDR	35	Device can be damaged.	A
PVDD	36	No impact.	D
OUT_1M	37	Overcurrent protection triggers.	B
PGND	38	System-level fault. Power short-to-ground.	B
PGND	39	System-level fault. Power short-to-ground.	B
BST_1P	40	Device can be damaged.	A
OUT_1P	41	Overcurrent protection triggers.	B
PVDD	42	No impact.	D
PVDD	43	No impact.	D
OUT_2P	44	Overcurrent protection triggers.	B
BST_2P	45	Device can be damaged.	A
PGND	46	System-level fault. Power short-to-ground.	B
PGND	47	System-level fault. Power short-to-ground.	B
OUT_2M	48	Overcurrent protection triggers.	B
PVDD	49	No impact.	D
VBAT	50	No impact.	D
NC	51	No impact.	D
GVDD_BYP	52	Device can be damaged.	A
AVDD_RET	53	System-level fault. Power short-to-ground.	B
AVDD_BYP	54	Device can be damaged.	A
VREG_BYP	55	Device can be damaged.	A
VREG_RET	56	System-level fault. Power short-to-ground.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	Device can be damaged.	A
/PD	2	Device can be damaged.	A
/FAULT	3	Device can be damaged.	A
GVDD_RET	4	System-level fault. Power short-to-ground.	B
CPC_BOT	5	Device can be damaged.	A
CPC_TOP	6	Device can be damaged.	A
CP	7	Device can be damaged.	A
PVDD_SNS	8	No impact.	D
PVDD	9	No impact.	D
OUT_4M	10	Overcurrent protection triggers.	B
PGND	11	System-level fault. Power short-to-ground.	B
BST_4P	12	Device can be damaged.	A
OUT_4P	13	Overcurrent protection triggers.	B
PVDD	14	No impact.	D
PVDD	15	No impact.	D
OUT_3P	16	Overcurrent protection triggers.	B
BST_3P	17	Device can be damaged.	A
PGND	18	System-level fault. Power short-to-ground.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VBAT (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PGND	19	System-level fault. Power short-to-ground.	B
OUT_3M	20	Overcurrent protection triggers.	B
PVDD	21	No impact.	D
GPIO_2	22	Device can be damaged.	A
GPIO_1	23	Device can be damaged.	A
SDOUT_1	24	Device can be damaged.	A
SDIN_1	25	Device can be damaged.	A
FSYNC	26	Device can be damaged.	A
SCLK	27	Device can be damaged.	A
GND	28	System-level fault. Power short-to-ground.	B
VR_DIG_RET	29	System-level fault. Power short-to-ground.	B
PLL_BYP	30	Device can be damaged.	A
VR_DIG_BYP	31	Device can be damaged.	A
DVDD	32	Device can be damaged.	A
SCL	33	Device can be damaged.	A
SDA	34	Device can be damaged.	A
I2C_ADDR	35	Device can be damaged.	A
PVDD	36	No impact.	D
OUT_1M	37	Overcurrent protection triggers.	B
PGND	38	System-level fault. Power short-to-ground.	B
PGND	39	System-level fault. Power short-to-ground.	B
BST_1P	40	Device can be damaged.	A
OUT_1P	41	Overcurrent protection triggers.	B
PVDD	42	No impact.	D
PVDD	43	No impact.	D
OUT_2P	44	Overcurrent protection triggers.	B
BST_2P	45	Device can be damaged.	A
PGND	46	System-level fault. Power short-to-ground.	B
PGND	47	System-level fault. Power short-to-ground.	B
OUT_2M	48	Overcurrent protection triggers.	B
PVDD	49	No impact.	D
VBAT	50	No impact.	D
NC	51	No impact.	D
GVDD_BYP	52	Device can be damaged.	A
AVDD_RET	53	System-level fault. Power short-to-ground.	B
AVDD_BYP	54	Device can be damaged.	A
VREG_BYP	55	Device can be damaged.	A
VREG_RET	56	System-level fault. Power short-to-ground.	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to DVDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
/STBY	1	Device is not able to shut down.	B
/PD	2	Device is not able to shut down.	B
/FAULT	3	FAULTs cannot be reported correctly.	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to DVDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GVDD_RET	4	System-level fault. Power short-to-ground.	B
CPC_BOT	5	Device can be damaged.	A
CPC_TOP	6	Device can be damaged.	A
CP	7	Device can be damaged.	A
PVDD_SNS	8	Undervoltage protection triggers.	B
PVDD	9	Undervoltage protection triggers.	B
OUT_4M	10	Overcurrent protection triggers.	B
PGND	11	System-level fault. Power short-to-ground.	B
BST_4P	12	Overcurrent protection triggers.	B
OUT_4P	13	Overcurrent protection triggers.	B
PVDD	14	Undervoltage protection triggers.	B
PVDD	15	Undervoltage protection triggers.	B
OUT_3P	16	Overcurrent protection triggers.	B
BST_3P	17	Overcurrent protection triggers.	B
PGND	18	System-level fault. Power short-to-ground.	B
PGND	19	System-level fault. Power short-to-ground.	B
OUT_3M	20	Overcurrent protection triggers.	B
PVDD	21	Undervoltage protection triggers.	B
GPIO_2	22	Large current occurs if pin voltage is different with DVDD.	A
GPIO_1	23	Large current occurs if pin voltage is different with DVDD.	A
SDOUT_1	24	Large current occurs if pin voltage is different with DVDD.	A
SDIN_1	25	Reports a clock error.	B
FSYNC	26	Reports a clock error.	B
SCLK	27	Reports a clock error.	B
GND	28	System-level fault. Power short-to-ground.	B
VR_DIG_RET	29	System-level fault. Power short-to-ground.	B
PLL_BYP	30	Device can be damaged.	A
VR_DIG_BYP	31	Device can be damaged.	A
DVDD	32	No impact.	D
SCL	33	I2C interface cannot work.	B
SDA	34	I2C interface cannot work.	B
I2C_ADDR	35	I2C address can be affected. Device can lose I2C connection.	B
PVDD	36	Undervoltage protection triggers.	B
OUT_1M	37	Overcurrent protection triggers.	B
PGND	38	System-level fault. Power short-to-ground.	B
PGND	39	System-level fault. Power short-to-ground.	B
BST_1P	40	Overcurrent protection triggers.	B
OUT_1P	41	Overcurrent protection triggers.	B
PVDD	42	Undervoltage protection triggers.	B
PVDD	43	Undervoltage protection triggers.	B
OUT_2P	44	Overcurrent protection triggers.	B
BST_2P	45	Overcurrent protection triggers.	B
PGND	46	System-level fault. Power short-to-ground.	B
PGND	47	System-level fault. Power short-to-ground.	B
OUT_2M	48	Overcurrent protection triggers.	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to DVDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
PVDD	49	Undervoltage protection triggers.	B
VBAT	50	Undervoltage protection triggers.	B
NC	51	No impact.	D
GVDD_BYP	52	Performance can degrade.	C
AVDD_RET	53	System-level fault. Power short-to-ground.	B
AVDD_BYP	54	Performance can degrade.	C
VREG_BYP	55	Performance can degrade.	C
VREG_RET	56	System-level fault. Power short-to-ground.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265