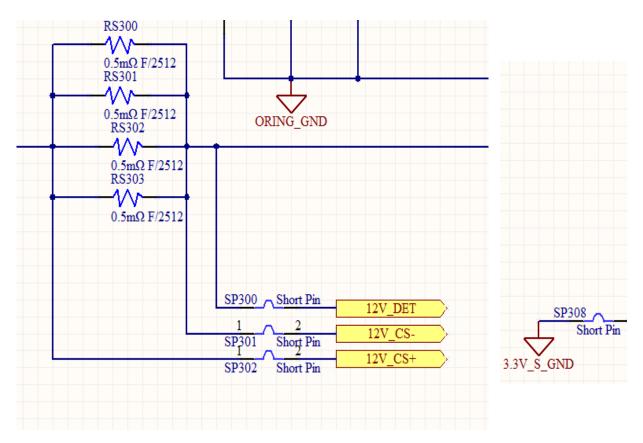
## 1, Question

CFF800V5TT project is using IC INA214AIDCKR as CS, the output delay is different under different inp

## 2、 schematic



# 3、Scope

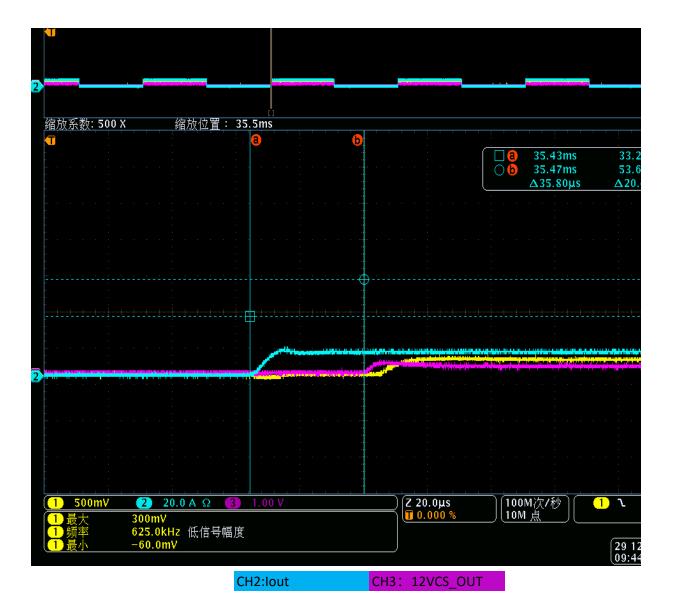
						<del>,</del>
1 500mV	<b>2</b> 20.0 A	Ω (3) 1.00	· · · · · · · · · · · · · · · · · · ·	10.0µs 0.000 %	100M次/秒 10M 点	<u>ן</u> ג
<ul> <li>↓ 最大</li> <li>1 频率</li> <li>1 最小</li> </ul>	980mV Hz	€发现周期 		<b>0.000 10</b> j		29 12 09:10

CH2:lout CH3: 12VCS\_OUT

(b)12V output, 0-32.8A(100% Load) dynamic load , the delay between output cu



<mark>(c)12V output, 0-13.12A(100% Load) dynamic load, the delay between output c Tek预选 M 10.0ms</mark>



#### (2)Removed C304, the wavefrom under different test set-up Removed INA214AIDCKR input filter cap C304

a)12V	output, 0-6	65.6A(10	0% Load	dyna	mic load,	the delay	between ou	itput c
ek 预 <u></u> 5				•	M	10.0ms		•
缩放系数	: 1kX	缩放位置:	60.9ms	· · · · · · · · · · · · · · · · · · ·	· • •			
							<b>a</b> 60.90ms	33
						· · · · · · ·	60.89ms     Δ8.300μs	53 ∆2
							2301300,00	
					· · · · · · · · · · · · · · · · · · ·	tea and a state of the second s		
				φ	7			

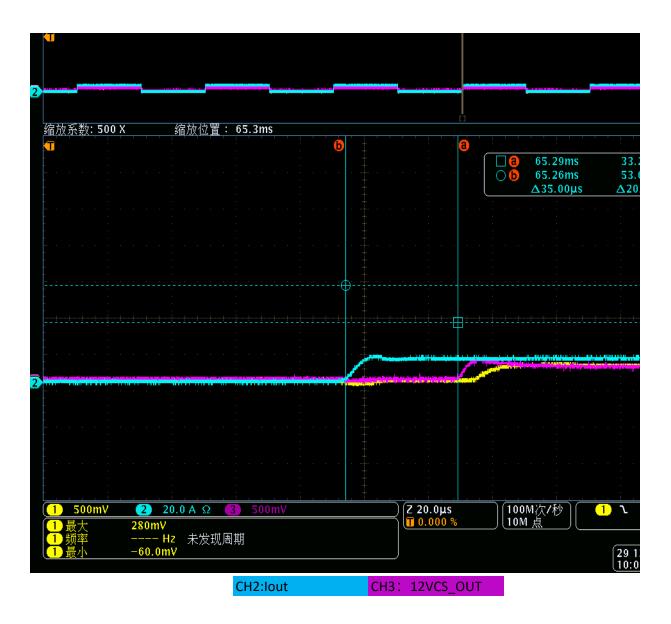
1.02 V	0.0 A Ω <u>3</u> 500mV z 未发现周期 /	Z 10.0μs 0.000 %	(100M次/秒) 10M 点 29 12 10:08

CH2:lout CH3: 12VCS\_OUT



CH2:lout CH3: 12VCS\_OUT

<mark>(c)12V output, 0-13.12A(100% Load) dynamic load, the delay between output c Tek 预选 M 10.0ms</mark>



Conclusion: C304 will not impact the delay. The delay under different dynamic

### 4, Question

why the dealy of INA214AIDCKR is defferent under different dynamic load.

