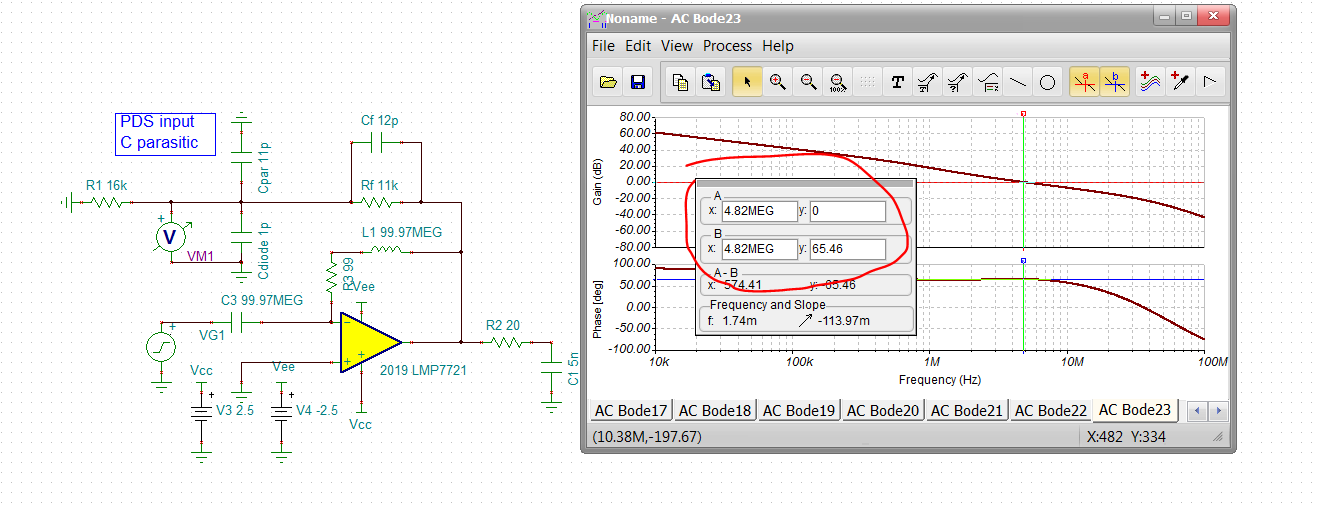
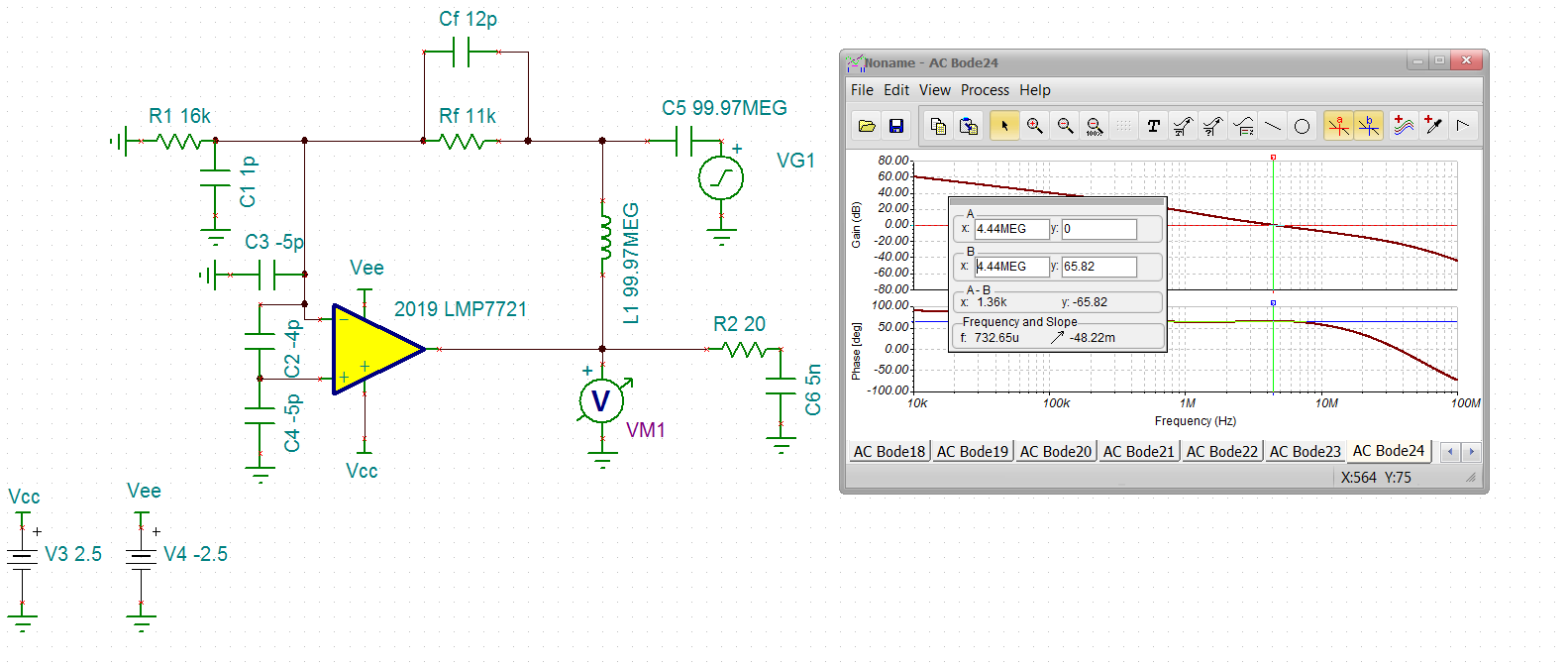
LG phase margin testing with updated LMP7721 model with correct 11pF input C

Here we get about 65.5deg with 11pF for a device parasitic and 1pF for the detector



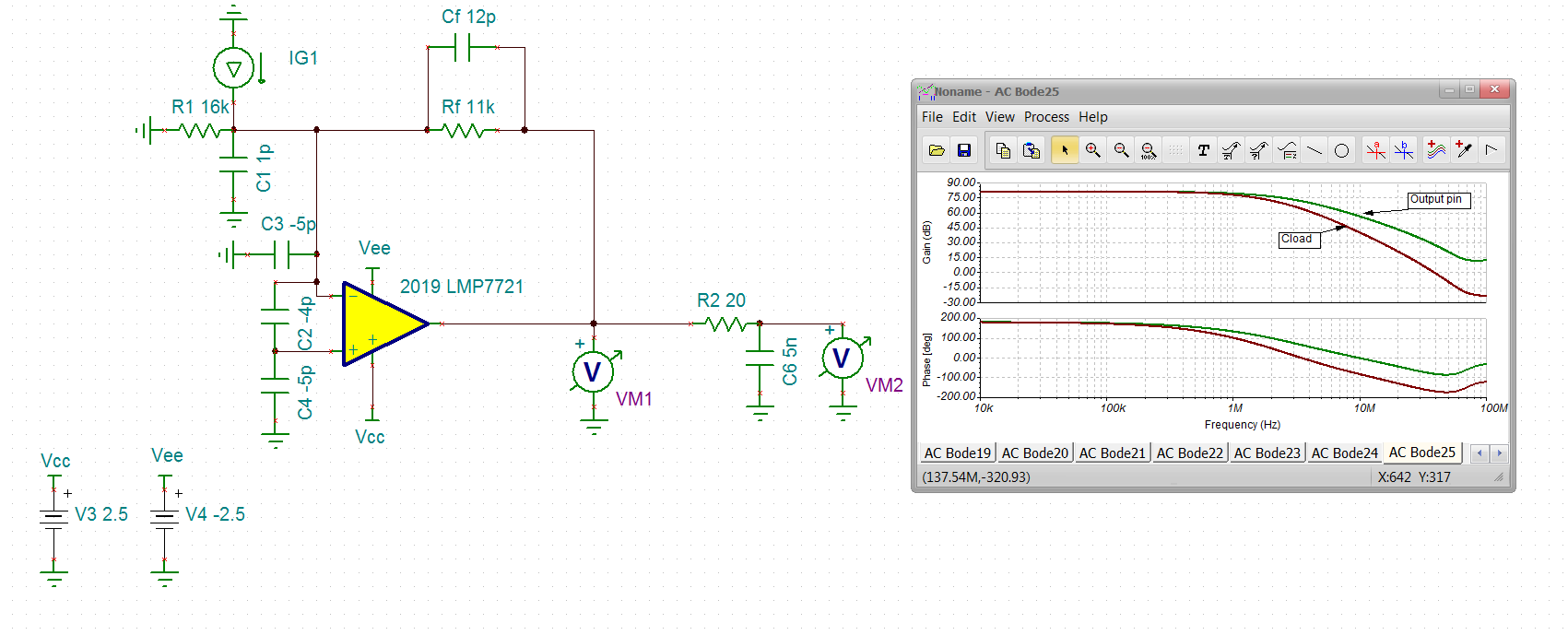
Now use the adjusted subckt in the older LG test circuit shown at the bottom above,

Ok, so now this is making sense, the older method that is missing the feedback load interacting with the Zol is showing 65.8deg with the input C adjust subckt – and going to the new method drops that to 65.5deg. So yes, not much difference here – normally, it is a little lower phase margin including a feedback network in the LG that has a C across the feedback R. If I were to use a device with a higher frequency resonance in the Zol, the difference would be a lot more.



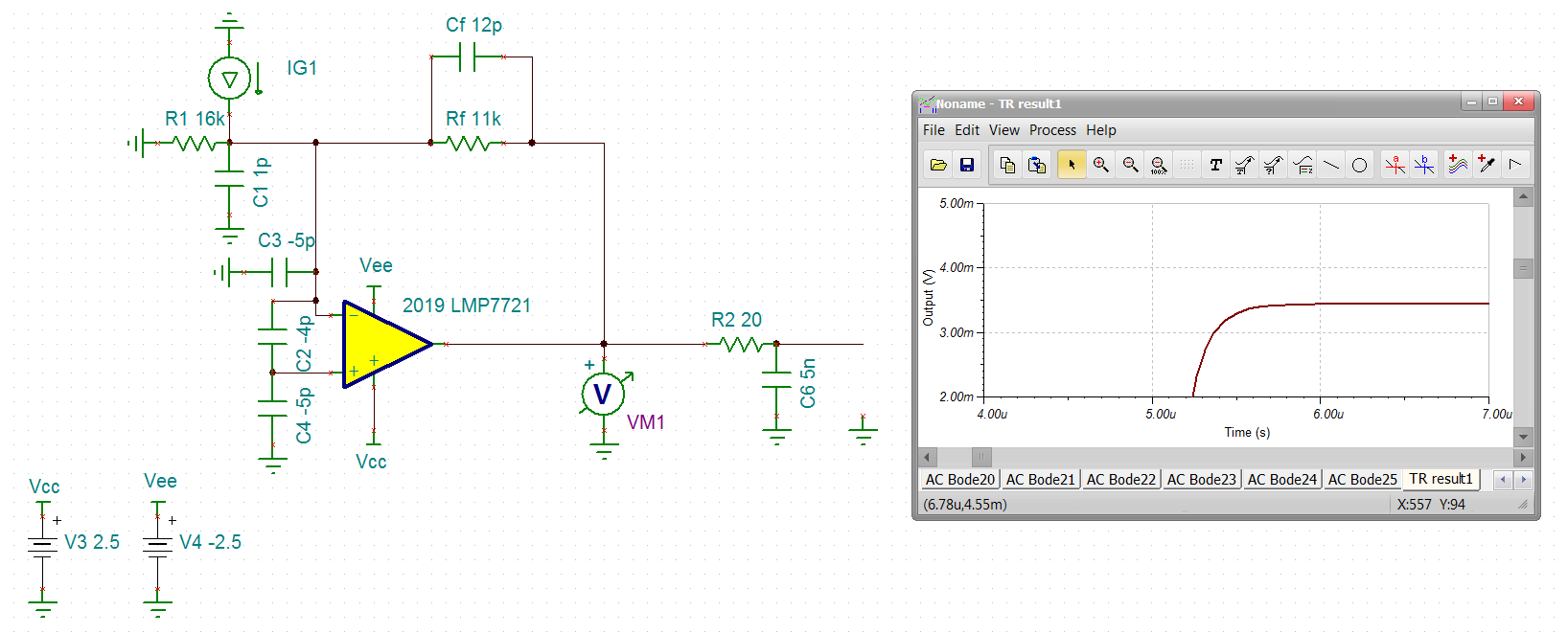
So going closed loop with the updated subckt model and a current source input gives this.

Yes, this looks very Butterworth at the output pin,



A butterworth (65.5deg phase margin) is 4.3% overshoot, try a +/-5mVoutput step (+/-4.4545e-7A input)

Getting no overshoot actually, this is really clean,



Has a little bit of output offset voltage in this,

