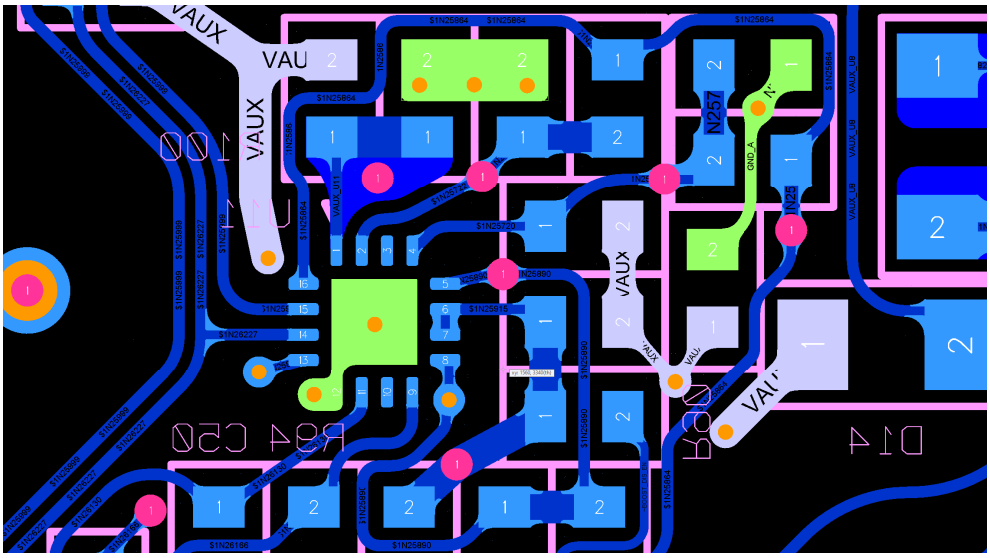
Thank you both for your responses.

Clemens: I disagree somewhat about the decoupling capacitor. This is not a digital IC. As the transistor model you posted shows, VCC feeds multiple constant current sources. VCC current is a constant DC even during output switching since the output is open collector (the load current doesn't flow through VCC pin). This bears out in the high supply rejection ratio of 100 dB typ. For this type of part the purpose of the decoupling cap is mainly filtering noise coming from the power source, not to provide a low impedance to the IC. To that end R108/C58 is a low pass filter for filtering any noise from the power source.

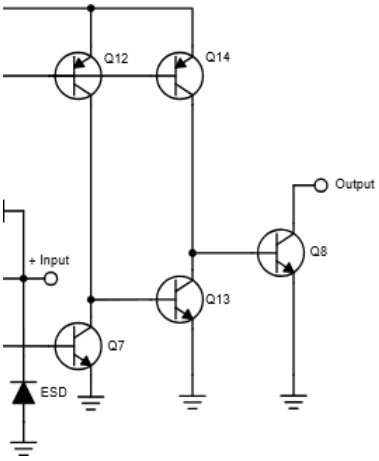
On the same IC these glitches occur on any output pin with a high resistance pullup. You can swap pullups around. If a output pin has a high resistance pullup you get negative glitches on that pin. Lower the pullup resistance and the negative glitch disappears. Having the glitch on some output pins but not others on the same IC and the fact you can move the glitches around to different output pins should eliminate VCC as the issue.

Also, the width of the negative glitch is proportional to pullup resistance. As you increase the pullup current the width of the glitch gets smaller and smaller.

Further, these glitches occur on devices with a traditional low impedance VCC decoupling path as shown here.



<u>Open drain devices CAN generate voltages below GND.</u> Per your image:



Assume output Q8 is low and has a high resistance pullup. The collector of Q8 will be close to GND since the Q8 collector current is low. Q8 base is one Vbe above GND. So Vbc is also one Vbe above GND.

When Q13 turns on the base of Q8 is driven to GND (or VCEsat). However, the collector- base capacitance of Q8 was previously charged to Vbe. Turning on Q13 drops Q8 base voltage by one Vbe. Because the collector-base capacitance of Q8 can't change voltage instantaneously the collector of Q8 also drops by one Vbe. Since the collector of Q8 was initially at GND the output pin goes negative by one Vbe until the collector-base capacitance of Q8 is discharged.

Paul Grohe:

Layout is correct. Pin 11 and 12 are tied together. Tying Pin 11 to 5 would require another via and jumper trace. Decided the layout was cleaner and less susceptible to noise without the added via.

LED resistors weren't intended or need to be precise. I wanted the highest LED current within the transient thermal impedance of the LEDs at the highest ambient temperature of this product. Value turned out to be around 500 Ω. Didn't have a 499 Ω on the BOM but have a 2k and 681. 681 by itself is about 30% less light. Using two existing $0.001 resistors in parallel helps the production floor by not needing to pull another reel from the warehouse, load it on the chip shooters, add it to ICT, AOI, etc. If it was more than one or two places I would have picked a single resistor.

"The output can only pull to GND, so there is no way the comparator output can pull below the GND pin." Yes, it can. See explanation above using Clemens schematic.

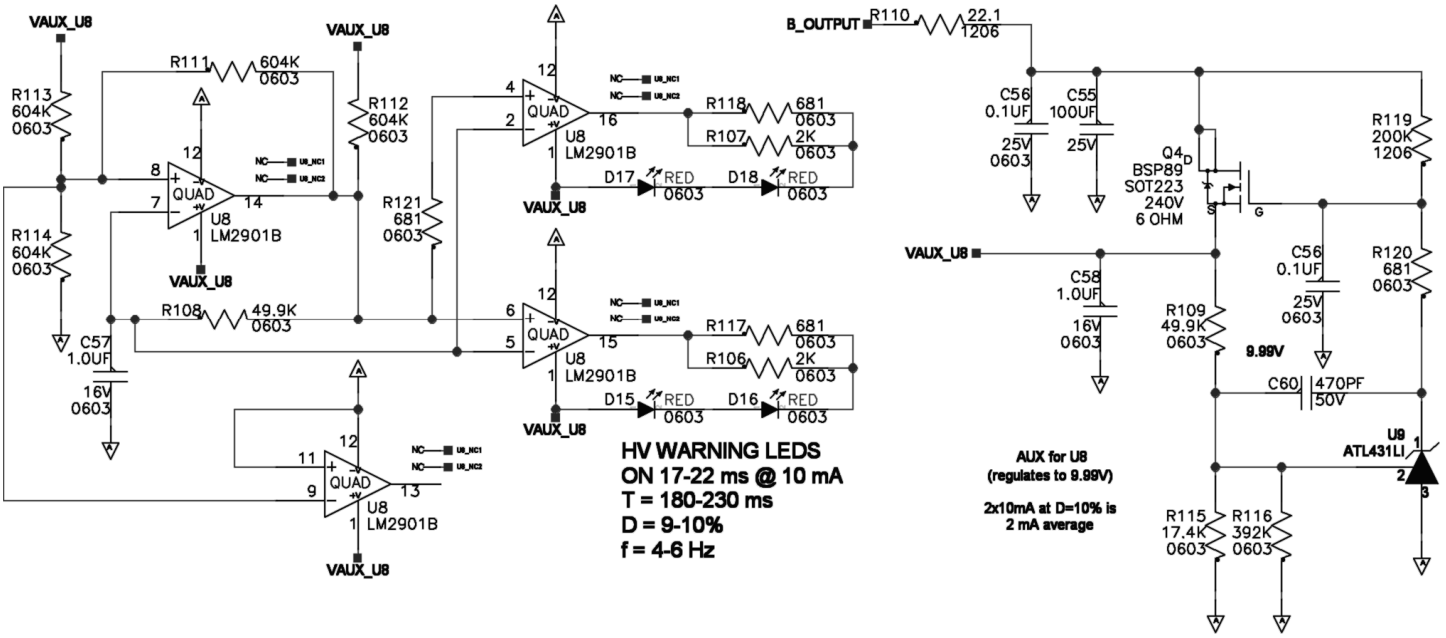
Glitches do not coincide with other system switching. This board has no digital, no SMPS, no RF, pure analog. For the scope traces the comparator was fed with a linear lab supply. Rest of the board is unpowered.

I've observed this on at least 8 different LM2901B circuits on 3 different board designs. Each circuit has a different schematic and layout. The only thing that is common is if the pullup is high impedance the output is driven negative when the output transitions from low to high.

I'm beginning to think there were changes to Q8 and Q13 vs older LM324 types. Changes in collector/base drive, c-b capacitance, and switching speed combine to drive the output negative when pullup current is low.

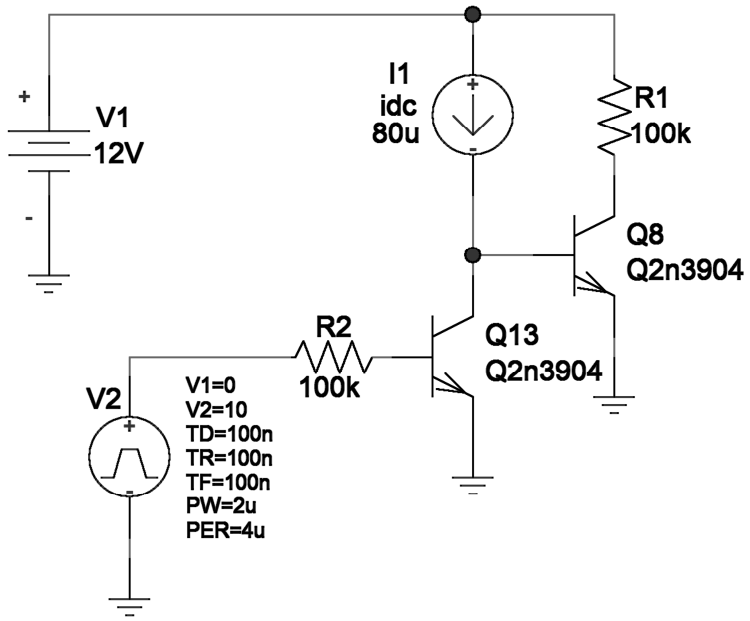
"Both the comparator, references and LED's are powered off the same "soft" supply, and the LED's turning on could cause a dip in the supply, causing feedback."

Negative dips occur on other LM2901B circuits including this identical circuit but with a linear regulator for VCC. Again negative dips on pin 14 and pin 13. None on pin 15 or 16. Can change R112 to 10k and negative dips disappear. Can increase R107/R118 or R117/R106 to 499k and now negative dips appear on those pins.



No channels are being abused. All inputs are within common-mode range. The only pins dipping below GND are the output pins and the only output pins that have high resistance or no resistance pullups.

A simple simulation of the output stage as a sanity check gives similar behavior to the LM2901B. With a high pullup resistance you get negative glitches on the output (collector of Q8). See my explanation of collector-base capacitance above. A faster Q13 or larger Q8 capacitance makes the negative glitch worse which seems to have happened on these 'next generation' devices.



Simulation results show negative output pin: