LMH6517

Problem: SPI reading and writing not working

Transformer shorting out the function generator for changing values for the gain

Set up:

Pin 2: Clk **CUST: SW**

Pin 1: SDI **CUST: SW**

Pin 32: CS **CUST: DDS\_RF\_VGA\_CS? Maybe SW**

Pin 31: SDO **CUST: SW**

Pin 3,4,6,7,8,9,10,16,20,21,25 Connect to GND **CUST: 3, 7, 8, 9, 10, 25 - Unconnected**

Pin 30, 11: IPA+ and IPB+ **CUST: Transformer**

Pin 29, 12: IPA- and IPB- **CUST: Transformer**

Pin 24, 17: OPA+ and OPB+ **CUST: UNK**

Pin 23, 18: OPA-, and OPB- **CUST: UNK**

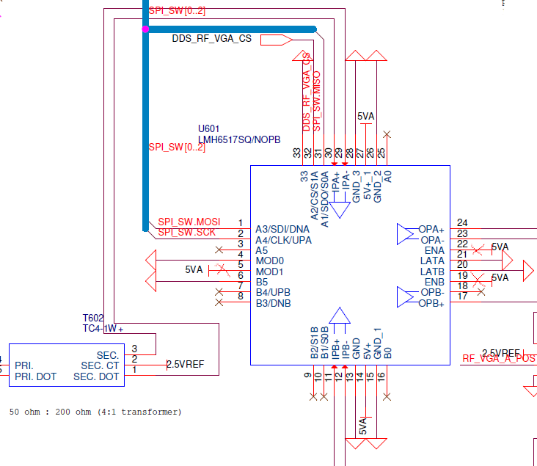
Pin 13, 15, 26, 28: GND **CUST: GND**

Pin 14, 27: +5V **CUST: 5V**

Pin 4, 5: MOD0 and MOD1: float high if unconnected **MOD0: low, MOD1: High 🡪 Serial**

Pin 22, 19: ENA and ENB: **CUST: 5V**

SPI Mode (MOD0 connected to ground and MOD1 floating)



Question:

1. Pin 1 with marking? **Yes**
2. SDO pin (1.8k pull down to ground and pull up to 3.3V): **Ok**
3. Issues a read command in mode 0 with 1MHz clock and lowers CS. Then send 0x80 and sends to 0x80 a dummy byte while reading. Then raises CS. SDO stays high either way.
   1. Stuck in a gain of approx. 10, no change to gain or shut of the output
   2. Transformer 0.2Vpp 3MHz signal on the primary, one side at DC while other side is excited. Secondary 0.2Vpp on each single ended side so 0.4Vpp

**Timing: Sclk: CLK signal at certain pulse width: 40-60 percent duty cycle: 10.5MHz**

**SDI pin on rising edge, SDO pin on falling edge**

**CS: assertion new register action**

**Needs to be de-asserted after the 16th clock**

**SDI: Write CHA Max Gain (16dB step at max gain of 10): 0000000010000000 binary or 0x80 in Hex. Seems correct, it should be giving a gain of 10**

**1st bit R/WB, 3 bits Reserved (0), Address 4 bits (0 Serial), Last 8 bits are Data for Gain Setting as shown in Table 4 page 24 in datasheet**

**Try SDI Write CHA Min Gain of 0xFE and see if you get min gain of around 0.335**

**SDI: Read CHA 1000000010000000 or Hex 0x8080**

1. Default at power up for gain and enable and disable? **ENA and ENB pins are active in the serial mode. For fast disable capability these pins can be used and the serial register will hold the last active gain state. These pins will float high and can be left disconnected for serial mode. SDO upon power-up the default register address is 00h.**
2. Inter-Access gap: Minimum time serial chip select pin must be asserted between accesses
   1. **3 Cycles of SCLK (gap between asserts can assert with CS after 3 cycles of CLK signal)**