LMH6517

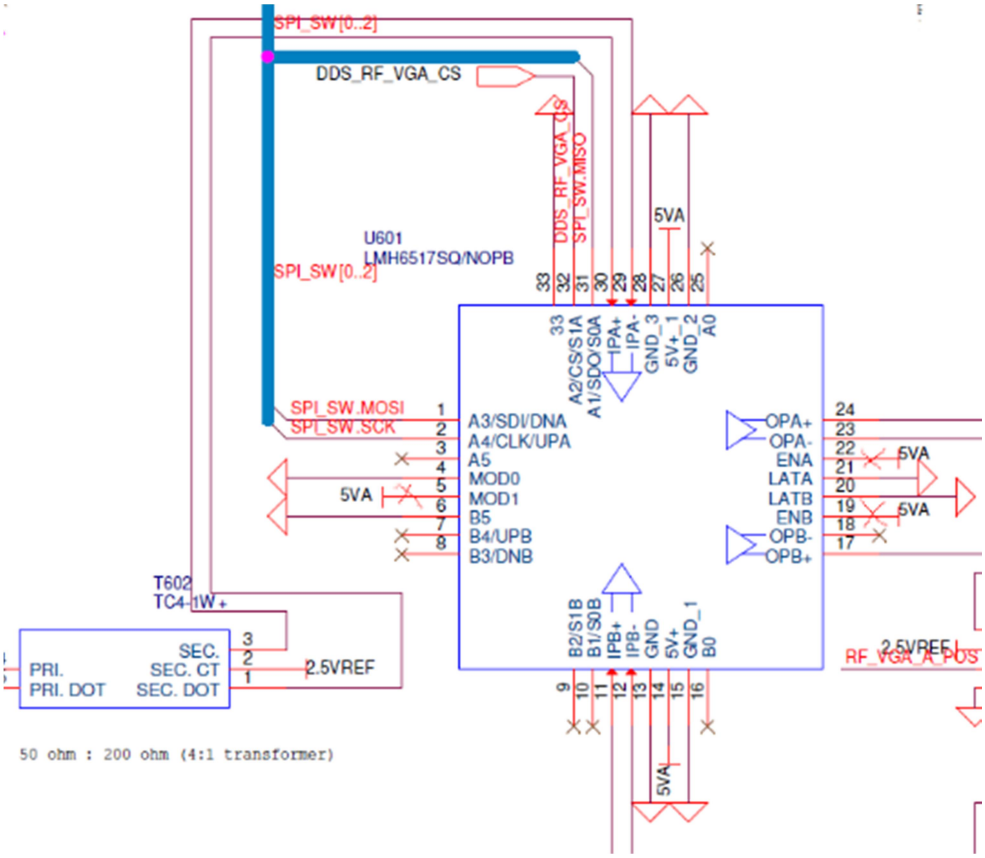
Problem: SPI reading and writing not working

Transformer shorting out the function generator for changing values for the gain

Set up:

Pin 2: Clk	**CUST: SW**
Pin 1: SDI	**CUST: SW**
Pin 32: CS	**CUST: DDS_RF_VGA_CS? Maybe SW**
Pin 31: SDO	**CUST: SW**
Pin 3,4,6,7,8,9,10,16,20,21,25 Connect to GND	**CUST: 3, 7, 8, 9, 10, 25 - Unconnected**
Pin 30, 11: IPA+ and IPB+	**CUST: Transformer**
Pin 29, 12: IPA- and IPB-	**CUST: Transformer**
Pin 24, 17: OPA+ and OPB+	**CUST: UNK**
Pin 23, 18: OPA-, and OPB-	**CUST: UNK**
Pin 13, 15, 26, 28: GND	**CUST: GND**
Pin 14, 27: +5V	**CUST: 5V**
Pin 4, 5: MOD0 and MOD1: float high if unconnected	**MOD0: low, MOD1: High → Serial**
Pin 22, 19: ENA and ENB:	**CUST: 5V**

SPI Mode (MOD0 connected to ground and MOD1 floating)



Question:

1- Pin 1 with marking? **Yes**
2- SDO pin (1.8k pull down to ground and pull up to 3.3V): **Ok**
3- Issues a read command in mode 0 with 1MHz clock and lowers CS. Then send 0x80 and sends to 0x80 a dummy byte while reading. Then raises CS. SDO stays high either way.
    a. Stuck in a gain of approx. 10, no change to gain or shut of the output
    b. Transformer 0.2Vpp 3MHz signal on the primary, one side at DC while other side is excited. Secondary 0.2Vpp on each single ended side so 0.4Vpp

Timing: Sclk: CLK signal at certain pulse width: 40-60 percent duty cycle: 10.5MHz

SDI pin on rising edge, SDO pin on falling edge

CS: assertion new register action

Needs to be de-asserted after the 16th clock

SDI: Write CHA Max Gain (16dB step at max gain of 10): 0000000010000000 binary or 0x80 in Hex. Seems correct, it should be giving a gain of 10

1st bit R/WB, 3 bits Reserved (0), Address 4 bits (0 Serial), Last 8 bits are Data for Gain Setting as shown in Table 4 page 24 in datasheet

Try SDI Write CHA Min Gain of 0xFE and see if you get min gain of around 0.335

SDI: Read CHA 1000000010000000 or Hex 0x8080

4- Default at power up for gain and enable and disable? **ENA and ENB pins are active in the serial mode. For fast disable capability these pins can be used and the serial register will hold the last active gain state. These pins will float high and can be left disconnected for serial mode. SDO upon power-up the default register address is 00h.**

5- Inter-Access gap: Minimum time serial chip select pin must be asserted between accesses
   a. **3 Cycles of SCLK (gap between asserts can assert with CS after 3 cycles of CLK signal)**

Questions-2 (12/4):

Gain steps of 0.5dB over a 31.5dB range (16+8+4+2+1+0.5 = 31.5dB)

From 21.85dB gain to -9.5dB gain typical

Gain Parameters						
	Maximum Gain	Gain Code 000000, DC Voltage Gain	21.7 **21.65**	21.85	22 **22.05**	dB
	Minimum Gain	Gain Code 111111, DC Voltage Gain	−9.25 **−9.1**	−9.5	−9.78 **−9.8**	dB
	Gain Adjust Range			31.5		dB
	Gain Step Size			0.5		dB

Gain bit zero = 0.5dB step. Gain steps down from maximum gain (000000 = Maximum Gain)
Gain bit one = 1dB step
Gain bit two = 2dB step
Gain bit three = 4dB step
Gain bit four = 8dB step
Gain bit five = 16dB step

1- Made work with:
   a. 0x30: 0000000000110000**: Write, Reserved + Address, CHA, Not enabled? 8+4 step down from Maximum Gain**
   b. 0x50: 0000000001010000**: Write, Reserved + Address, CHA, Not enabled? 16+4 step down from Maximum Gain**
   c. 0x70: 0000000001110000**: Write, Reserved + Address, CHA, Not Enabled? 16+8+4 step down from Maximum Gain**

2- Not Working:
   a. 0x00**: Write, Reserved + Address, CHA, Not Enabled, Maximum Gain**

3- Try These Hex Codes to write from Datasheet:
   a. Max Gain to ChA: 0000000010000000 **equal to Hex: 80 Enabled at Max Gain**
   b. Min Gain to CHA: 0000000011111110 **equal to Hex: FE Enabled at Min Gain**

c. 21.85dB gain – 16dB step down CHA: 0000000011000000: **equal to Hex: C0 Enabled at gain of 5.85dB**
d. 21.85dB gain – 20dB step down (16+4dB) CHA: 0000000011010000: **equal to Hex: D0 Enabled at gain of 1.85dB**

4- Write works without sending clock cycles?
   a. That is weird, it needs clock cycles for data to send on rising edge of the clock and data to be read at falling edge of the clock
   b. Thanks for sending explanation of the CLK and comments on the code (I can now see what you mean in reference to your code).
   c. **Can you continually generate CLK signals of around 10.5MHz (duty cycle of 50 percent low to high state)? I believe you would need to use PWM pins on the Arduino. You are sending bits rather than using these dedicated pins. From what I remember from using Arduinos, it would be Timer 2 with TCCR2A and TCCR2B registers as well as OCR2A and OCR2B counters.**

5- Read Command:
   a. Device reads at falling edge of the CLK, in your first image of the post you are actually not sending a read command at 49us. You are sending a write command of max gain to CH0 which would be around 21.85dB gain or 10V/V. To send a read command:

Read	Reserved	Reserved	Reserved	Address	Address	Address	CHA
1	0	0	0	0	0	0	0
Enable	GB5	GB4	GB3	GB2	GB1	GB0	Reserved
1 (Maybe X)	X	X	X	X	X	X	0 (maybe X)

X is Don't Care, in datasheet it states it disregards Data if first bit is 1 indicating read command. So in binary: 1000000010000000, in **Hex: 8080 or 8000 if it disregards all of data including enable bit.**

6- Assertion:
   a. This only comes into play when you are sending two commands, like in the first image Between ~20us and ~49us, CS needs to be de-asserted for 3 CLK cycles before being asserted for the next command.
   b. Example:
      i. CS HIGH
      ii. CS LOW before the 1st CLK (first data command either Read or Write)
      iii. CS HIGH after the 16th CLK (first data command either Read or Write registered in Device)
      iv. CS HIGH for atleast 3 CLK cycles
      v. CS can now be LOW for second data command either Read or Write