Functional Safety Information

LMV3xx-N-Q1 Functional Safety FIT Rate, FMD, and Pin FMA

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for the following devices to aid in a functional safety system design:

LMV321-N-Q1
SOT-23 (5)

Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

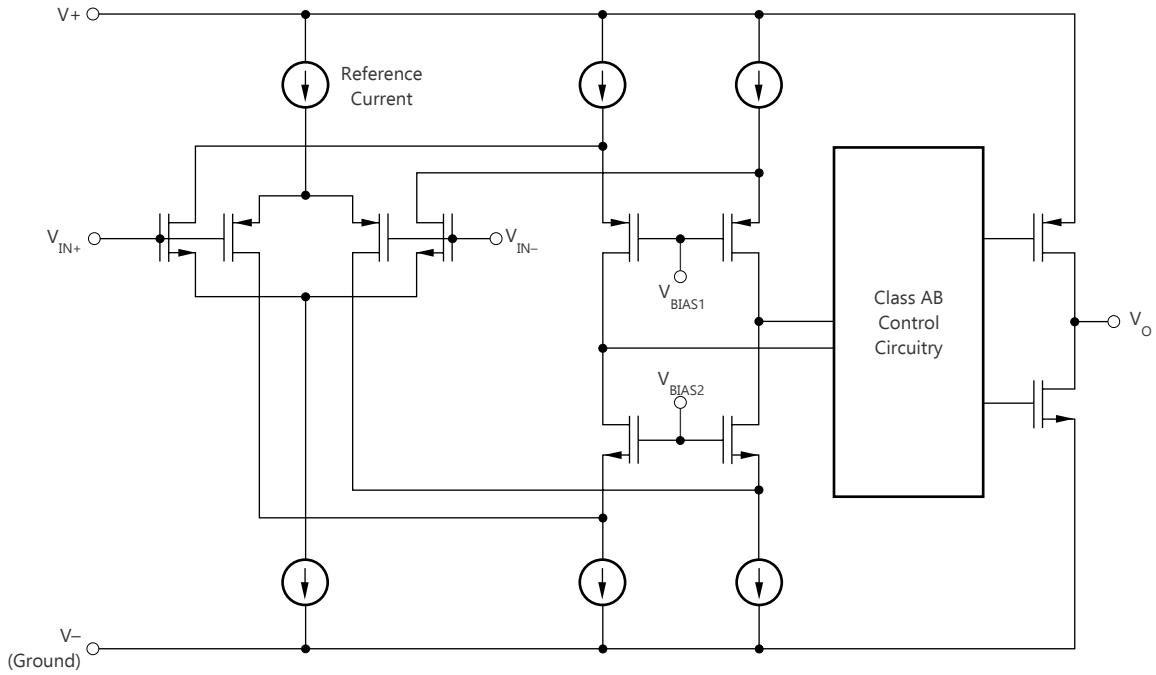

Figure 1-1. Functional Block Diagram

The LMV3xx-N-Q1 family was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 (5) Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 (5) package of the LMV321-N-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 10 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar Op Amp, Comparators, Voltage Monitors	6 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMV3xx-N-Q1 family in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the LMV3xx-N-Q1 device family. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to (V-)
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to (V+)

Table 4-1 includes context for what failure modes these pin conditions induce.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 LMV321-N-Q1 Packages

4.1.1 5-Pin Packages with OUT on Pin 4 ("Southeast" Pinout)

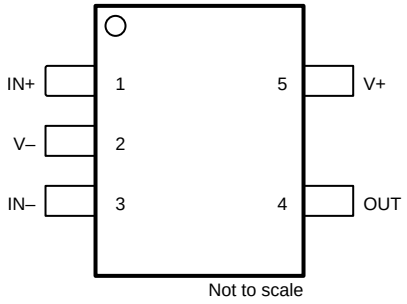

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Negative Supply (V-) Pin

Pin Analysis for Pin Short-Circuit to Negative Supply (V-)					
Pin Name	**Pin No.**	**Device Damage**	**Device Funtionality Affected**	**Description of Potential Failure Effect(s)/Comments**	**Failure Effect Class**
IN+	1	No	No	Input at V- potential is valid input, however, desired application result is unlikely	C
(V-)	2	No	No	Normal operation	D
IN-	3	No	No	Input at V- potential is valid input, however, desired application result is unlikely	C
OUT	4	Potentially	Yes	May cause overheating	B
(V+)	5	Potentially	Yes	Diodes from input to V+ may turn due to input signal and cause EOS	B

Table 4-3. Pin FMA for Device Pins Short-Circuited to Positive Supply (V+) Pin

Pin Analysis for Pin Short-Circuit to Positive Supply (V+)					
Pin Name	**Pin No.**	**Device Damage**	**Device Funtionality Affected**	**Description of Potential Failure Effect(s)/Comments**	**Failure Effect Class**
IN+	1	No	No	Input at V+ potential is valid input, however, desired application result is unlikely	C
(V-)	2	Potentially	Yes	Diodes from input to V- may turn due to input signal and cause EOS	B
IN-	3	No	No	Input at V+ potential is valid input, however, desired application result is unlikely	C
OUT	4	Potentially	Yes	May cause overheating	B
(V+)	5	No	No	Normal operation	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Analysis for Pin Short-Circuit to next higher pin number					
Pin Name	**Pin No.**	**Device Damage**	**Device Funtionality Affected**	**Description of Potential Failure Effect(s)/Comments**	**Failure Effect Class**
IN+ to (V-)	1 → 2	No	No	Input at V- is valid input, however, desired application result is unlikely	C
(V-) to IN-	2 → 3	No	No	Input at V- is valid input, however, desired application result is unlikely	C
IN- to OUT	3 → 4	No	No	Connection is allowed. However, amplifier will function as buffer and any feedback network will be short-circuited.	C
OUT to (V+)	4 → 5	Potentially	Yes	May cause overheating	B
(V+) to IN+	5 → 1	No	No	Input at V- is valid input, however, desired application result is unlikely	C

Table 4-5. Pin FMA for Device Pins Open-Circuited

Pin Analysis for Pin Open-Circuit					
Pin Name	**Pin No.**	**Device Damage**	**Device Functionality Affected**	**Description of Potential Failure Effect(s)/Comments**	**Failure Effect Class**
IN+	1	No	No	Floating input, circuit will likely not function as expected.	C
(V-)	2	Potentially	Yes	Lowest voltage pin will try to power internal supply via ESD diode to V-	B
IN-	3	No	No	Floating input, circuit will likely not function as expected.	C
OUT	4	No	Yes	Output can't be used by application.	C
(V+)	5	Potentially	Yes	Highest voltage pin will try to power internal supply via ESD diode to V+	B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265