LMV772QMMX/NOPB Automotive Low Offset, Low Noise, RRO Dual Operational Amplifier

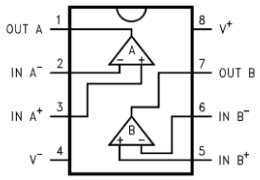

Table 1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Table 2. Pin FMA Analysis for Device Pins Short-Circuited to V-

Pin No.	Short to V- Name	Description of Potential Failure Effects	Class
1	OUT A	Short to V- may cause device to overheat.	B
2	IN A-	Input at V- is valid input, however, desired application result is unlikely.	C
3	IN A+	Input at V- is valid input, however, desired application result is unlikely.	C
4	V-	Normal Operation if single supply configuration is used.	D
5	IN B+	Input at V- is valid input, however, desired application result is unlikely.	D
6	IN B-	Input at V- is valid input, however, desired application result is unlikely.	D
7	OUT B	Short to V- may cause device to overheat.	B
8	V+	Diodes from input to V+ may turn due to input signal and cause EOS.	A

Table 3. Pin FMA Analysis for Device Pins Open-Circuited

Pin No.	Open pin Name	Comments	Class
1	OUT A	Output can't be used by application.	C
2	IN A-	Floating input, circuit will likely not function as expected.	C
3	IN A+	Floating input, circuit will likely not function as expected.	C
4	V-	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
5	IN B+	Floating input, circuit will likely not function as expected.	C
6	IN B-	Floating input, circuit will likely not function as expected.	C
7	OUT B	Output can't be used by application.	C
8	V+	Highest voltage pin will try to power internal ground via ESD diode to VCC.	B

Table 4. Pin FMA Analysis for Device Pins Short-Circuit to V+

Pin No.	Short to V+ Name	Comments	Class
1	OUT A	Short to V+ may cause device to overheat.	B
2	IN A-	Input at V+ is valid input, however, desired application result is unlikely.	C
3	IN A+	Input at V+ is valid input, however, desired application result is unlikely.	C
4	V-	Diodes from input to V+ may turn due to input signal and cause EOS.	A
5	IN B+	Input at V+ is valid input, however, desired application result is unlikely.	C
6	IN B-	Input at V+ is valid input, however, desired application result is unlikely.	C
7	OUT B	Short to V+ may cause device to overheat.	B
8	V+	No change if same node as V+	D

Table 5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin No.	Short to next pin Name	Comments	Class
1 to 2	OUT A to IN A-	Channel 1 configured in unity gain.	C
2 to 3	IN A- to IN A+	No damage to device. Application circuit will not work.	C
3 to 4	IN A+ to V-	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
4 to 5	V- to IN B+	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
5 to 6	IN B+ to IN B-	No damage to device. Application circuit will not work.	C
6 to 7	IN B- to OUT B	Channel 2 configured in unity gain.	C